# NBSG16VS

# 2.5V/3.3V SiGe Differential Receiver/Driver with Variable Output Swing

**ON Semiconductor®**

**http://onsemi.com**

### Description

The NBSG16VS is a differential receiver/driver targeted for high frequency applications that require variable output swing. The device is functionally equivalent to the EP16VS device with much higher bandwidth and lower EMI capabilities. This device may be used for applications driving VCSEL lasers.

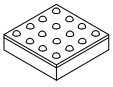
Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. The output amplitude is varied by applying a voltage to the $V_{CTRL}$ input pin. Outputs are variable swing ECL from 100 mV to 750 mV amplitude, optimized for operation from $V_{CC} - V_{EE}$ = 3.0 V to 3.465 V.

The $V_{BB}$ and $V_{MM}$ pins are internally generated voltage supplies available to this device only. The $V_{BB}$ is used as a reference voltage for single−ended NECL or PECL inputs and the $V_{MM}$ pin is used as a reference voltage for LVCMOS inputs. For single−ended input operation, the unused complementary differential input is connected to $V_{BB}$ or $V_{MM}$ as a switching reference voltage. $V_{BB}$ or $V_{MM}$ may also rebias AC−coupled inputs. When used, decouple $V_{BB}$ and $V_{MM}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ and $V_{MM}$ outputs should be left open.

### Features

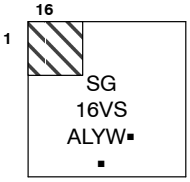
- Maximum Input Clock Frequency up to 12 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- 40 ps Typical Rise and Fall Times ($V_{CTRL} = V_{CC} - 1$ V)
- 120 ps Typical Propagation Delay ($V_{CTRL} = V_{CC} - 1$ V)
- Variable Swing PECL Output with Operating Range: $V_{CC}$ = 2.375 V to 3.465 V with $V_{EE}$ = 0 V
- Variable Swing NECL Output with NECL Inputs with Operating Range: $V_{CC}$ = 0 V with $V_{EE}$ = −2.375 V to −3.465 V
- Output Level (100 mV to 750 mV Peak−to−Peak Output; $V_{CC} - V_{EE}$ = 3.0 V to 3.465 V), Differential Output Only
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V EP Devices
- $V_{BB}$ and $V_{MM}$ Reference Voltage Output
- Pb−Free Packages are Available

**MARKING DIAGRAMS***



**FCBGA−16**
**BA SUFFIX**
**CASE 489**


**QFN−16**
**MN SUFFIX**
**CASE 485G**




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

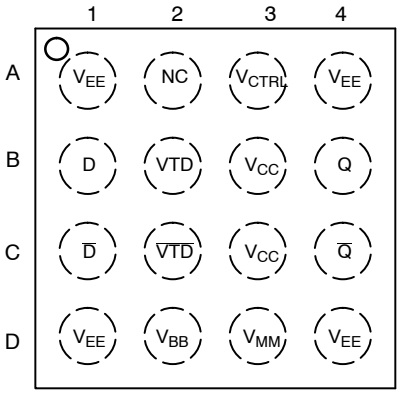



**Figure 1. BGA−16 Pinout** (Top View)

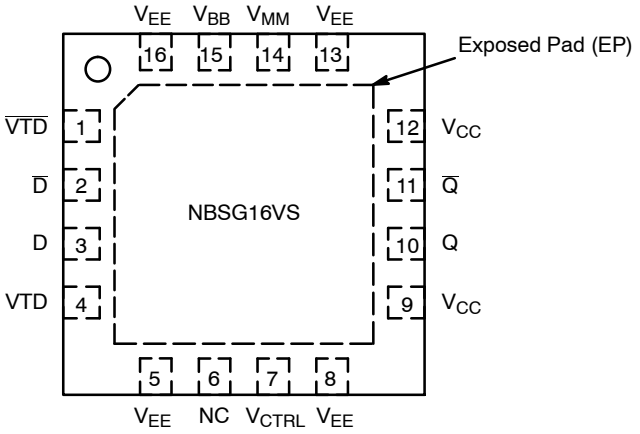



**Figure 2. QFN−16 Pinout** (Top View)

**Table 1. PIN DESCRIPTION**

| Pin | | Name | I/O | Description |
|---|---|---|---|---|
| BGA | QFN | | | |
| C2 | 1 | $\overline{VTD}$ | − | Internal 50 Ω Termination Pin. See Table 2. |
| C1 | 2 | $\overline{D}$ | ECL, CML, LVCMOS, LVDS, LVTTL Input | Inverted Differential Input. Internal 75 kΩ to $V_{EE}$ and 36.5 kΩ to $V_{CC}$. |
| B1 | 3 | D | ECL, CML, LVCMOS, LVDS, LVTTL Input | Noninverted Differential Input. Internal 75 kΩ to $V_{EE}$. |
| B2 | 4 | VTD | − | Internal 50 Ω Termination Pin. See Table 2. |
| A1,D1,A4, D4 | 5,8,13,16 | $V_{EE}$ | − | Negative Supply Voltage |
| A2 | 6 | NC | − | No Connect |
| A3 | 7 | $V_{CTRL}$ | | Output Amplitude Swing Control. Bypass Pin to $V_{CC}$ through 0.1 μF Capacitor. |
| B3,C3 | 9,12 | $V_{CC}$ | − | Positive Supply Voltage |
| B4 | 10 | Q | RSECL Output | Noninverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V |
| C4 | 11 | $\overline{Q}$ | RSECL Output | Inverted Differential Output. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V |
| D3 | 14 | $V_{MM}$ | − | LVCMOS Reference Voltage Output. $(V_{CC} - V_{EE})/2$ |
| D2 | 15 | $V_{BB}$ | − | ECL Reference Voltage Output |
| N/A | − | EP | − | The Exposed Pad (EP) and the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is not electrically connected to the die but may be electrically and thermally connected to $V_{EE}$ on the PC board. |

1. The NC pin is electrically connected to the die and must be left open.
2. All $V_{CC}$ and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat−sinking conduit.
3. In the differential configuration when the input termination pins (VTD, $\overline{VTD}$) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self−oscillation.

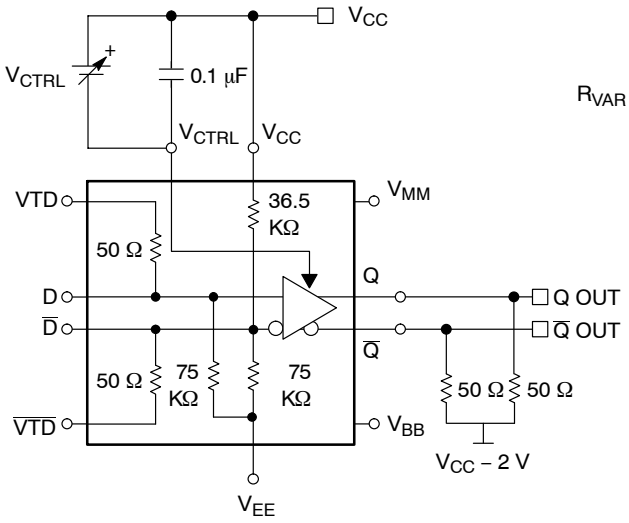



**Figure 3. Logic Diagram/ Voltage Source Implementation**

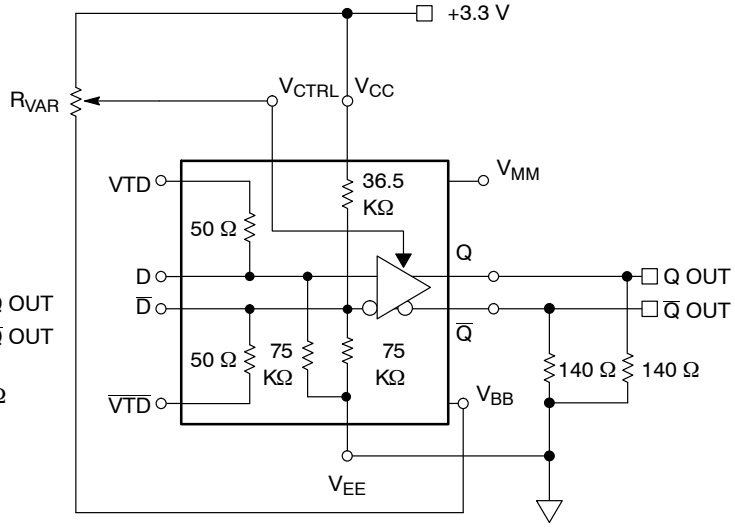



**Figure 4. Alternative Voltage Source Implementation**

**Table 2. INTERFACING OPTIONS**

| INTERFACING OPTIONS | CONNECTIONS |
|---|---|
| CML | Connect VTD and $\overline{VTD}$ to $V_{CC}$ |
| LVDS | Connect VTD and $\overline{VTD}$ Together |
| AC−COUPLED | Bias VTD and $\overline{VTD}$ Inputs within Common Mode Range ($V_{IHCMR}$) |
| RSECL, PECL, NECL | Standard ECL Termination Techniques |
| LVTTL | An external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTL. |
| LVCMOS | $V_{MM}$ should be connected to the unused complementary differential input. |

**Table 3. ATTRIBUTES**

| Characteristics | | Value | |
|---|---|---|---|
| Internal Input Pulldown Resistor (D, $\overline{D}$) | | 75 kΩ | |
| Internal Input Pullup Resistor ($\overline{D}$) | | 36.5 kΩ | |
| ESD Protection | Human Body Model<br>Machine Model | > 2 kV<br>> 100 V | |
| Moisture Sensitivity (Note 4) | | Pb Pkg | Pb−Free Pkg |
| | FCBGA−16<br>QFN−16 | Level 3<br>Level 1 | Level 3<br>Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| Transistor Count | | 192 | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

4. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Power Supply | $V_{EE}$ = 0 V | | 3.6 | V |
| $V_{EE}$ | Negative Power Supply | $V_{CC}$ = 0 V | | −3.6 | V |
| $V_I$ | Positive Input<br>Negative Input | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \le V_{CC}$<br>$V_I \ge V_{EE}$ | 3.6<br>−3.6 | V<br>V |
| $V_{INPP}$ | Differential Input Voltage $\lvert D - \overline{D} \rvert$ | $V_{CC} - V_{EE} \ge 2.8$ V<br>$V_{CC} - V_{EE} < 2.8$ V | | 2.8<br>$\lvert V_{CC} - V_{EE} \rvert$ | V<br>V |
| $I_{OUT}$ | Output Current | Continuous<br>Surge | | 25<br>50 | mA<br>mA |
| $I_{IN}$ | Input Current Through $R_T$ (50 Ω Resistor) | Static<br>Surge | | 45<br>80 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | 1 | mA |
| $I_{MM}$ | $V_{MM}$ Sink/Source | | | 1 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) (Note 5) | 0 lfpm<br>500 lfpm<br>0 lfpm<br>500 lfpm | FCBGA−16<br>FCBGA−16<br>QFN−16<br>QFN−16 | 108<br>86<br>41.6<br>35.2 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | 2S2P (Note 5)<br>2S2P (Note 6) | FCBGA−16<br>QFN−16 | 5.0<br>4.0 | °C/W<br>°C/W |
| $T_{sol}$ | Wave Solder Pb<br>Pb−Free | | | 225<br>265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

5. JEDEC standard 51−6 multilayer board − 2S2P (2 signal, 2 power).
6. JEDEC standards multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

**Table 5. DC CHARACTERISTICS, INPUT WITH VARIABLE PECL OUTPUT** $V_{CC}$ = 2.5 V; $V_{EE}$ = 0 V (Note 7)

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Negative Power Supply Current | 18 | 25 | 32 | 18 | 25 | 32 | 18 | 25 | 32 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 8) | 1315 | 1440 | 1565 | 1305 | 1430 | 1555 | 1305 | 1430 | 1555 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 8)<br>(Max Swing)<br>($V_{CTRL}$ = $V_{CC}$ − 600 mV) | <br>645<br>1090 | <br>765<br>1210 | <br>885<br>1330 | <br>605<br>1035 | <br>725<br>1155 | <br>845<br>1275 | <br>600<br>1010 | <br>720<br>1130 | <br>840<br>1250 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) (Notes 10 and 11) | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Notes 10 and 12) | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | mV |
| $V_{BB}$ | PECL Output Voltage Reference | 1080 | 1140 | 1200 | 1080 | 1140 | 1200 | 1080 | 1140 | 1200 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Note 9) (Differential Configuration) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| $V_{MM}$ | CMOS Output Voltage Reference<br>($V_{CC}$ − $V_{EE}$)/2 | <br>1100 | <br>1250 | <br>1400 | <br>1100 | <br>1250 | <br>1400 | <br>1100 | <br>1250 | <br>1400 | mV |
| $R_{TIN}$ | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | 30 | 100 | | 30 | 100 | | 30 | 100 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$) | | 25 | 50 | | 25 | 50 | | 25 | 50 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*Typicals used for testing purposes.

7. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.125 V to −0.965 V.
8. All loading with 50 Ω to $V_{CC}$ − 2.0 V. $V_{OH}$/$V_{OL}$ measured at $V_{IH}$/$V_{IL}$.
9. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
10. $V_{THR}$ is the voltage applied to the complementary input, typically $V_{BB}$ or $V_{MM}$. $V_{THR(MIN)}$ = $V_{IHCMR}$ + 75 mV. $V_{THR(MAX)}$ = $V_{IHCMR}$ − 75 mV.
11. $V_{IH}$ cannot exceed $V_{CC}$.
12. $V_{IL}$ always ≥ $V_{EE}$.

**Table 6. DC CHARACTERISTICS, INPUT WITH VARIABLE PECL OUTPUT** $V_{CC}$ = 3.3 V; $V_{EE}$ = 0 V (Note 18)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Negative Power Supply Current | 20 | 27 | 34 | 20 | 27 | 34 | 20 | 27 | 34 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 13) | 2095 | 2220 | 2345 | 2085 | 2210 | 2335 | 2075 | 2200 | 2325 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 13)<br>(Max Swing)<br>($V_{CTRL}$ = $V_{CC}$ − 600 mV) | <br>1275<br>1750 | <br>1395<br>1870 | <br>1515<br>1990 | <br>1285<br>1730 | <br>1405<br>1850 | <br>1525<br>1970 | <br>1295<br>1715 | <br>1415<br>1835 | <br>1535<br>1955 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) (Notes 15 and 16) | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Notes 15 and 17) | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | mV |
| $V_{BB}$ | PECL Output Voltage Reference | 1880 | 1940 | 2000 | 1880 | 1940 | 2000 | 1880 | 1940 | 2000 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Note 14) (Differential Configuration) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| $V_{MM}$ | CMOS Output Voltage Reference ($V_{CC}$ − $V_{EE}$)/2 | 1500 | 1650 | 1800 | 1500 | 1650 | 1800 | 1500 | 1650 | 1800 | mV |
| $R_{TIN}$ | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | 30 | 100 | | 30 | 100 | | 30 | 100 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$) | | 25 | 50 | | 25 | 50 | | 25 | 50 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*Typicals used for testing purposes.

13. All loading with 50 Ω to $V_{CC}$ − 2.0 V. $V_{OH}$/$V_{OL}$ measured at $V_{IH}$/$V_{IL}$.
14. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
15. $V_{THR}$ is the voltage applied to the complementary input, typically $V_{BB}$ or $V_{MM}$. $V_{THR(MIN)}$ = $V_{IHCMR}$ + 75 mV. $V_{THR(MAX)}$ = $V_{IHCMR}$ − 75 mV.
16. $V_{IH}$ cannot exceed $V_{CC}$.
17. $V_{IL}$ always ≥ $V_{EE}$.
18. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.925 V to −0.165 V.

**Table 7. DC CHARACTERISTICS, NECL INPUT WITH VARIABLE NECL OUTPUT**

$V_{CC}$ = 0 V; $V_{EE}$ = −3.465 V to −2.375 V (Note 19)

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Negative Power Supply Current | 20 | 27 | 34 | 20 | 27 | 34 | 20 | 27 | 34 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 20)<br>−3.465 V ≤ $V_{EE}$ ≤ −3.0 V<br>−3.0 V < $V_{EE}$ ≤ −2.375 V | <br>−1205<br>−1185 | <br>−1080<br>−1060 | <br>−955<br>−935 | <br>−1215<br>−1195 | <br>−1090<br>−1070 | <br>−965<br>−945 | <br>−1225<br>−1195 | <br>−1100<br>−1070 | <br>−975<br>−945 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 20)<br>−3.465 V ≤ $V_{EE}$ ≤ −3.0 V<br>(Max Swing)<br>($V_{CTRL}$ = $V_{CC}$ − 600 mV)<br>−3.0 V < $V_{EE}$ ≤ −2.375 V<br>(Max Swing)<br>($V_{CTRL}$ = $V_{CC}$ − 600 mV) | <br><br>−2000<br>−1560<br><br>−1855<br>−1410 | <br><br>−1910<br>−1440<br><br>−1620<br>−1215 | <br><br>−1820<br>−1320<br><br>−1290<br>−1000 | <br><br>−1990<br>−1580<br><br>−1895<br>−1460 | <br><br>−1900<br>−1460<br><br>−1705<br>−1290 | <br><br>−1810<br>−1340<br><br>−1425<br>−1100 | <br><br>−1980<br>−1595<br><br>−1900<br>−1490 | <br><br>−1890<br>−1475<br><br>−1730<br>−1330 | <br><br>−1800<br>−1355<br><br>−1470<br>−1150 | mV<br><br>mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) (Notes 22 and 23) | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{THR}$ + 75 | $V_{CC}$ − 1000* | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Notes 22 and 24) | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | $V_{IH}$ − 2500 | $V_{CC}$ − 1400* | $V_{THR}$ − 75 | mV |
| $V_{BB}$ | NECL Output Voltage Reference | −1420 | −1360 | −1300 | −1420 | −1360 | −1300 | −1420 | −1360 | −1300 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Note 21) (Differential Configuration) | $V_{EE}$+1.2 | | 0.0 | $V_{EE}$+1.2 | | 0.0 | $V_{EE}$+1.2 | | 0.0 | V |
| $V_{MM}$ | CMOS Output Voltage Reference (Note 25) | $V_{MMT}$ − 150 | $V_{MMT}$ | $V_{MMT}$ + 150 | $V_{MMT}$ − 150 | $V_{MMT}$ | $V_{MMT}$ + 150 | $V_{MMT}$ − 150 | $V_{MMT}$ | $V_{MMT}$ + 150 | mV |
| $R_{TIN}$ | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | 30 | 100 | | 30 | 100 | | 30 | 100 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$) | | 25 | 50 | | 25 | 50 | | 25 | 50 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*Typicals used for testing purposes.

19. Input and output parameters vary 1:1 with $V_{CC}$.
20. All loading with 50 Ω to $V_{CC}$ − 2.0 V. $V_{OH}$/$V_{OL}$ measured at $V_{IH}$/$V_{IL}$.
21. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
22. $V_{THR}$ is the voltage applied to the complementary input, typically $V_{BB}$ or $V_{MM}$. $V_{THR(MIN)}$ = $V_{IHCMR}$ + 75 mV. $V_{THR(MAX)}$ = $V_{IHCMR}$ − 75 mV.
23. $V_{IH}$ cannot exceed $V_{CC}$.
24. $V_{IL}$ always ≥ $V_{EE}$.
25. $V_{MM}$ typical = $|V_{CC}-V_{EE}|$ / 2 + $V_{EE}$ = $V_{MMT}$.

**Table 8. AC CHARACTERISTICS for FCBGA−16** $V_{CC}$ = 0 V; $V_{EE}$ = −3.465 V to −3.0 V or $V_{CC}$ = 3.0 V to 3.465 V; $V_{EE}$ = 0 V

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $f_{max}$ | Maximum Frequency (See Figure 8) (Note 26) | 10.7 (Note 29) | 12 | | 10.7 (Note 29) | 12 | | 10.7 (Note 29) | 12 | | GHz |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output Differential ($V_{CTRL}$ = $V_{CC}$ − 2 V) D → Q, $\overline{Q}$ ($V_{CTRL}$ = $V_{CC}$ − 1 V) D → Q, $\overline{Q}$ | 100 100 | 125 120 | 145 140 | 100 100 | 125 120 | 145 140 | 100 100 | 125 120 | 145 140 | ps |
| $t_{SKEW}$ | Duty Cycle Skew (Note 27) | | 3 | 10 | | 3 | 10 | | 3 | 10 | ps |
| $t_{JITTER}$ | RMS Random Clock Jitter $f_{in}$ < 10 GHz Peak−to−Peak Data Dependent Jitter $f_{in}$ < 10 Gb/s | | 0.8 TBD | 2 | | 0.8 TBD | 2 | | 0.8 TBD | 2 | ps |
| $V_{INPP}$ | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 28) | 75 | | 2600 | 75 | | 2600 | 75 | | 2600 | mV |
| $t_r$ $t_f$ | Output Rise/Fall Times (20% − 80%) @ 1 GHz ($V_{CTRL}$ = $V_{CC}$ − 2 V) Q, $\overline{Q}$ ($V_{CTRL}$ = $V_{CC}$ − 1 V) Q, $\overline{Q}$ | 30 30 | 45 40 | 55 50 | 30 30 | 45 40 | 55 50 | 30 30 | 45 40 | 55 50 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

26. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC}$−2.0 V. Input edge rates 40 ps (20% − 80%).
27. $t_{SKEW}$ = $|t_{PLH}-t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 10.
28. $V_{INPP(MAX)}$ cannot exceed $V_{CC}$ − $V_{EE}$ (applicable only when $V_{CC}$ − $V_{EE}$ < 2600 mV).
29. Conditions include input amplitude of 500 mV and $V_{CTRL}$ = $V_{CC}$ − 2 V. Minimum output amplitude guarantee of 100 mV (see Output P−P Spec in Figure 8).

**Table 9. AC CHARACTERISTICS for FCBGA−16** $V_{CC}$ = 0 V; −3.0 V < $V_{EE}$ ≤ −2.375 V or 2.375 V ≤ $V_{CC}$ < 3.0 V; $V_{EE}$ = 0 V

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $f_{max}$ | Maximum Frequency (See Figure 9) (Note 30) | 10.7 (Note 33) | 12 | | 10.7 (Note 33) | 12 | | 10.7 (Note 33) | 12 | | GHz |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output Differential ($V_{CTRL}$ = $V_{CC}$ − 2 V) D → Q, $\overline{Q}$ ($V_{CTRL}$ = $V_{CC}$ − 1 V) D → Q, $\overline{Q}$ | 100 100 | 125 120 | 145 140 | 100 100 | 125 120 | 145 140 | 100 100 | 125 120 | 145 140 | ps |
| $t_{SKEW}$ | Duty Cycle Skew (Note 31) | | 3 | 10 | | 3 | 10 | | 3 | 10 | ps |
| $t_{JITTER}$ | RMS Random Clock Jitter $f_{in}$ < 10 GHz Peak−to−Peak Data Dependent Jitter $f_{in}$ < 10 Gb/s | | 0.9 TBD | 3 | | 0.9 TBD | 3 | | 0.9 TBD | 3 | ps |
| $V_{INPP}$ | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 32) | 75 | | 2600 | 75 | | 2600 | 75 | | 2600 | mV |
| $t_r$ $t_f$ | Output Rise/Fall Times (20% − 80%) @ 1 GHz ($V_{CTRL}$ = $V_{CC}$ − 2 V) Q, $\overline{Q}$ ($V_{CTRL}$ = $V_{CC}$ − 1 V) Q, $\overline{Q}$ | 25 22 | 50 45 | 70 60 | 25 22 | 50 45 | 70 60 | 25 22 | 50 45 | 70 60 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

30. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC}$−2.0 V. Input edge rates 40 ps (20% − 80%).
31. $t_{SKEW}$ = $|t_{PLH}-t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 10.
32. $V_{INPP(MAX)}$ cannot exceed $V_{CC}$ − $V_{EE}$ (applicable only when $V_{CC}$ − $V_{EE}$ < 2600 mV).
33. Conditions include input amplitude of 500 mV and $V_{CTRL}$ = $V_{CC}$ − 2 V. Minimum output amplitude guarantee of 100 mV (see Output P−P Spec in Figure 9).

**Table 10. AC CHARACTERISTICS for QFN−16** $V_{CC}$ = 0 V; $V_{EE}$ = −3.465 V to −3.0 V or $V_{CC}$ = 3.0 V to 3.465 V; $V_{EE}$ = 0 V

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $f_{max}$ | Maximum Frequency (See Figure 8) (Note 34) | 10 (Note 37) | 12 | | 10 (Note 37) | 12 | | 10 (Note 37) | 12 | | GHz |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output Differential | | | | | | | | | | ps |
| | ($V_{CTRL}$ = $V_{CC}$ − 2 V) D → Q, $\overline{Q}$ | 100 | 140 | 180 | 100 | 140 | 180 | 100 | 140 | 180 | |
| | ($V_{CTRL}$ = $V_{CC}$ − 1 V) D → Q, $\overline{Q}$ | 100 | 135 | 180 | 100 | 135 | 180 | 80 | 135 | 220 | |
| $t_{SKEW}$ | Duty Cycle Skew (Note 35) | | 3 | 20 | | 3 | 15 | | 3 | 10 | ps |
| $t_{JITTER}$ | RMS Random Clock Jitter | | | | | | | | | | ps |
| | $f_{in}$ < 10 GHz | | 0.5 | 2 | | 0.5 | 2 | | 0.5 | 2 | |
| | Peak−to−Peak Data Dependent Jitter | | | | | | | | | | |
| | $f_{in}$ < 10 Gb/s | | TBD | | | TBD | | | TBD | | |
| $V_{INPP}$ | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 36) | 75 | | 2600 | 75 | | 2600 | 75 | | 2600 | mV |
| $t_r$ $t_f$ | Output Rise/Fall Times (20% − 80%) @ 1 GHz | | | | | | | | | | ps |
| | ($V_{CTRL}$ = $V_{CC}$ − 2 V) Q, $\overline{Q}$ | 30 | 45 | 55 | 30 | 45 | 55 | 30 | 45 | 55 | |
| | ($V_{CTRL}$ = $V_{CC}$ − 1 V) Q, $\overline{Q}$ | 30 | 40 | 50 | 30 | 40 | 50 | 30 | 40 | 50 | |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

34. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC}$−2.0 V. Input edge rates 40 ps (20% − 80%).
35. $t_{SKEW}$ = $|t_{PLH}-t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 10.
36. $V_{INPP(MAX)}$ cannot exceed $V_{CC}$ − $V_{EE}$ (applicable only when $V_{CC}$ − $V_{EE}$ < 2600 mV).
37. Conditions include input amplitude of 500 mV and $V_{CTRL}$ = $V_{CC}$ − 2 V. Minimum output amplitude guarantee of 100 mV (see Output P−P Spec in Figure 8).

**Table 11. AC CHARACTERISTICS for QFN−16** $V_{CC}$ = 0 V; −3.0 V < $V_{EE}$ ≤ −2.375 V or 2.375 V ≤ $V_{CC}$ < 3.0 V; $V_{EE}$ = 0 V

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $f_{max}$ | Maximum Frequency (See Figure 9) (Note 38) | 10 (Note 41) | 12 | | 10 (Note 41) | 12 | | 10 (Note 41) | 12 | | GHz |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output Differential | | | | | | | | | | ps |
| | ($V_{CTRL}$ = $V_{CC}$ − 2 V) D → Q, $\overline{Q}$ | 100 | 140 | 180 | 100 | 140 | 180 | 80 | 140 | 180 | |
| | ($V_{CTRL}$ = $V_{CC}$ − 1 V) D → Q, $\overline{Q}$ | 100 | 135 | 180 | 100 | 135 | 180 | 100 | 135 | 220 | |
| $t_{SKEW}$ | Duty Cycle Skew (Note 39) | | 3 | 20 | | 3 | 15 | | 3 | 10 | ps |
| $t_{JITTER}$ | RMS Random Clock Jitter | | | | | | | | | | ps |
| | $f_{in}$ < 10 GHz | | 0.5 | 3 | | 0.5 | 3 | | 0.5 | 3 | |
| | Peak−to−Peak Data Dependent Jitter | | | | | | | | | | |
| | $f_{in}$ < 10 Gb/s | | TBD | | | TBD | | | TBD | | |
| $V_{INPP}$ | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 40) | 75 | | 2600 | 75 | | 2600 | 75 | | 2600 | mV |
| $t_r$ $t_f$ | Output Rise/Fall Times (20% − 80%) @ 1 GHz | | | | | | | | | | ps |
| | ($V_{CTRL}$ = $V_{CC}$ − 2 V) Q, $\overline{Q}$ | 25 | 50 | 70 | 25 | 50 | 70 | 25 | 50 | 70 | |
| | ($V_{CTRL}$ = $V_{CC}$ − 1 V) Q, $\overline{Q}$ | 22 | 45 | 60 | 22 | 45 | 60 | 22 | 45 | 60 | |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

38. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC}$−2.0 V. Input edge rates 40 ps (20% − 80%).
39. $t_{SKEW}$ = $|t_{PLH}-t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 10.
40. $V_{INPP(MAX)}$ cannot exceed $V_{CC}$ − $V_{EE}$ (applicable only when $V_{CC}$ − $V_{EE}$ < 2600 mV).
41. Conditions include input amplitude of 500 mV and $V_{CTRL}$ = $V_{CC}$ − 2 V. Minimum output amplitude guarantee of 100 mV (see Output P−P Spec in Figure 9).

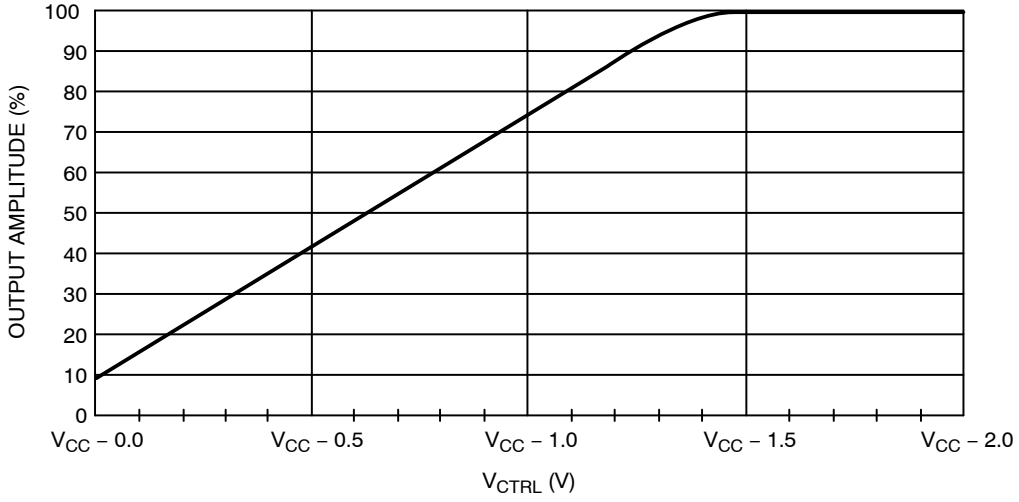



**Figure 5. Output Amplitude % vs. $V_{CTRL}$ (pin #A3)**

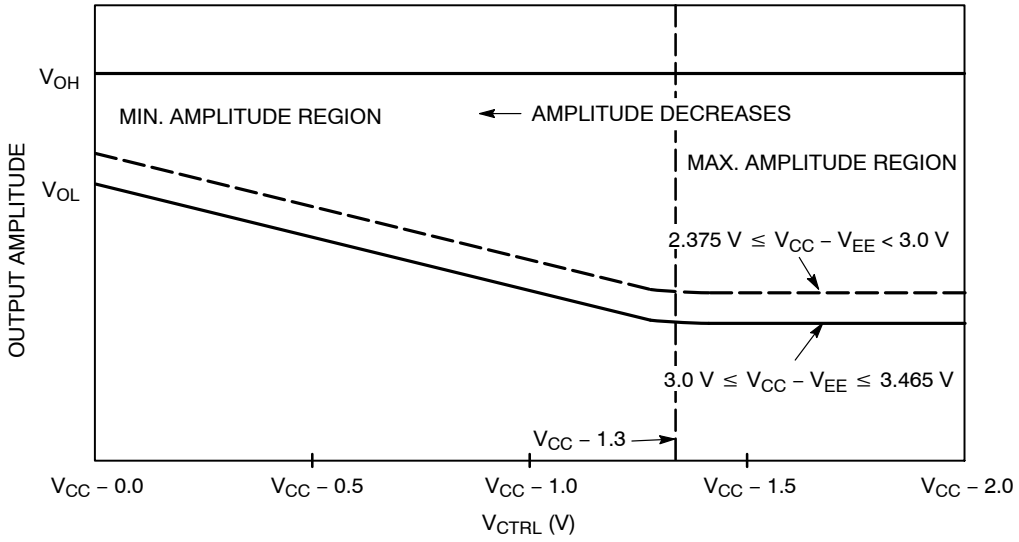



**Figure 6. Output Amplitude vs. $V_{CTRL}$ (pin #A3)**

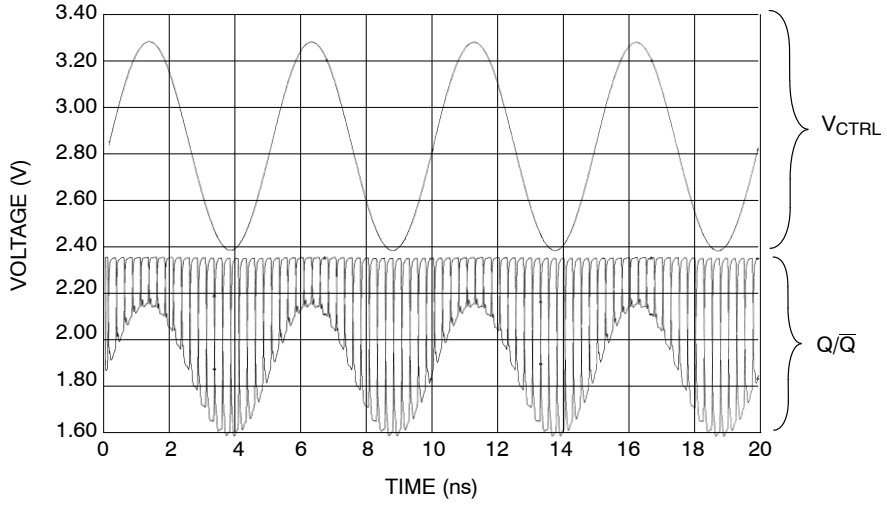



**Figure 7. Output Response Under Amplitude Modulation of $V_{CTRL}$ (Conditions Include $V_{CC} - V_{EE}$ = 3.3 V at 25°C, $f_{IN}$ ($V_{CTRL}$) = 200 MHz, and $f_{IN}$ (D, $\overline{D}$) = 2 GHz)**

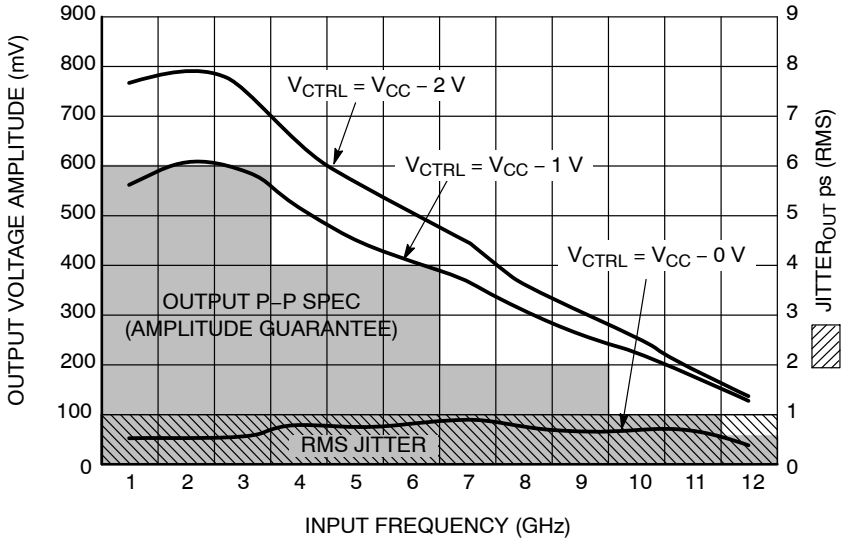



**Figure 8. Output Voltage Amplitude ($V_{OUTPP}$) / RMS Jitter vs. Input Frequency ($f_{in}$) at Ambient Temperature (Typical) See Tables 8 and 10 ($V_{CC}$ = 0 V; $V_{EE}$ = −3.465 V to −3.0 V or $V_{CC}$ = 3.0 V to 3.465 V; $V_{EE}$ = 0 V**

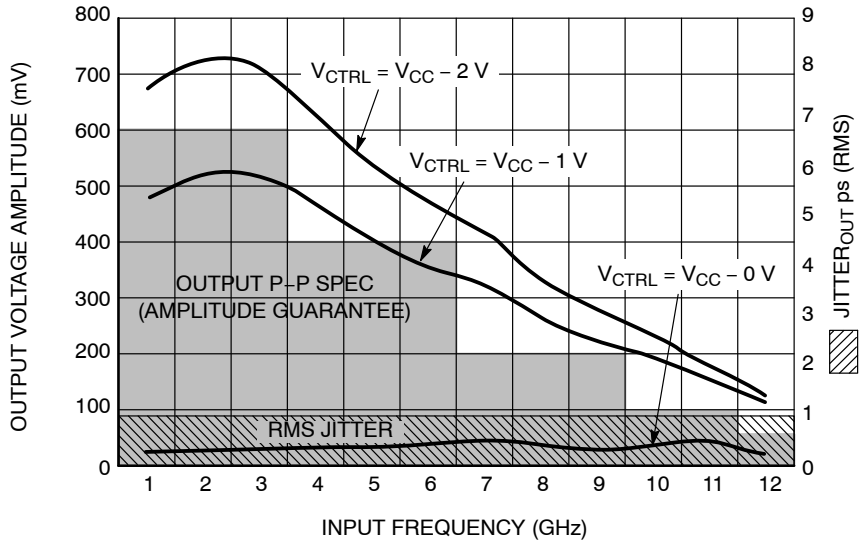



**Figure 9. Output Voltage Amplitude ($V_{OUTPP}$) / RMS Jitter vs. Input Frequency ($f_{in}$) at Ambient Temperature (Typical) See Tables 9 and 11 ($V_{CC}$ = 0 V; −3.0 V $V_{EE}$ −2.375 V or 2.375 V $V_{CC}$ 3.0 V; $V_{EE}$ = 0 V)**

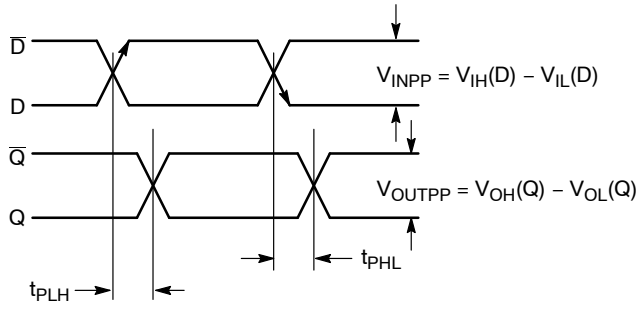



**Figure 10. AC Reference Measurement**

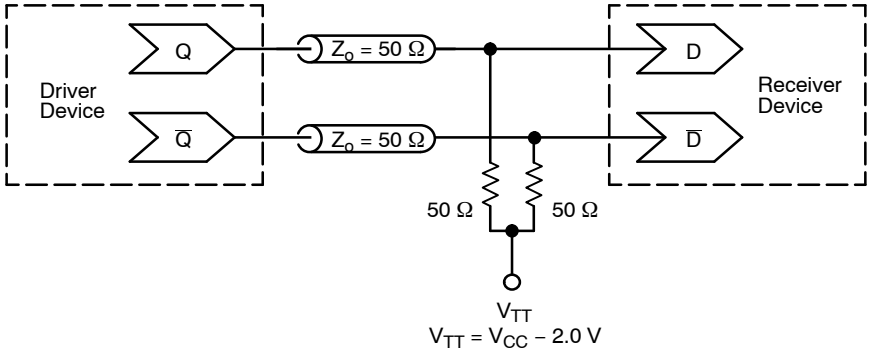



**Figure 11. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

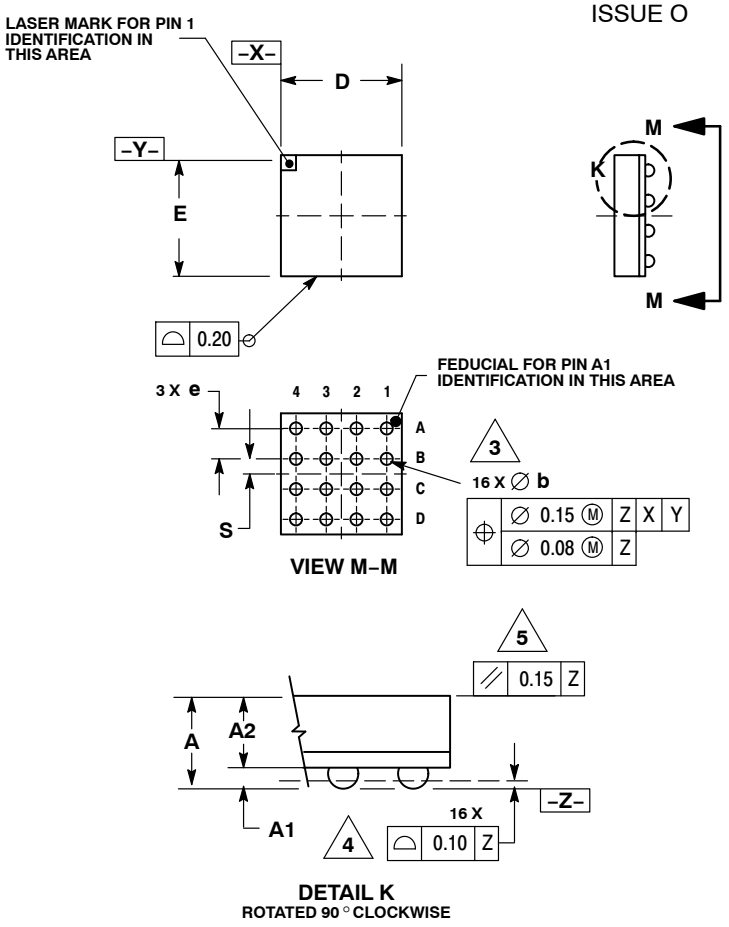
| Device | Package | Shipping† |
|---|---|---|
| NBSG16VSBAHTBG | FCBGA−16 (Pb−Free) | 100 / Tape & Reel |
| NBSG16VSBA | FCBGA−16 | 100 Units / Tray (Contact Sales Representative) |
| NBSG16VSBAR2 | FCBGA−16 | 100 / Tape & Reel (Contact Sales Representative) |
| NBSG16VSMN | QFN−16 | 123 Units / Rail |
| NBSG16VSMNG | QFN−16 (Pb−Free) | 123 Units / Rail |
| NBSG16VSMNR2 | QFN−16 | 3000 / Tape & Reel |
| NBSG16VSMNR2G | QFN−16 (Pb−Free) | 3000 / Tape & Reel |
| NBSG16VSMNHTBG | QFN−16 (Pb−Free) | 100 / Tape & Reel |

| Board | Description |
|---|---|
| NBSG16VSBAEVB | NBSG16VSBA Evaluation Board |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**FCBGA−16**
**BA SUFFIX**
PLASTIC 4X4 (mm) BGA FLIP CHIP PACKAGE
CASE 489−01
ISSUE O

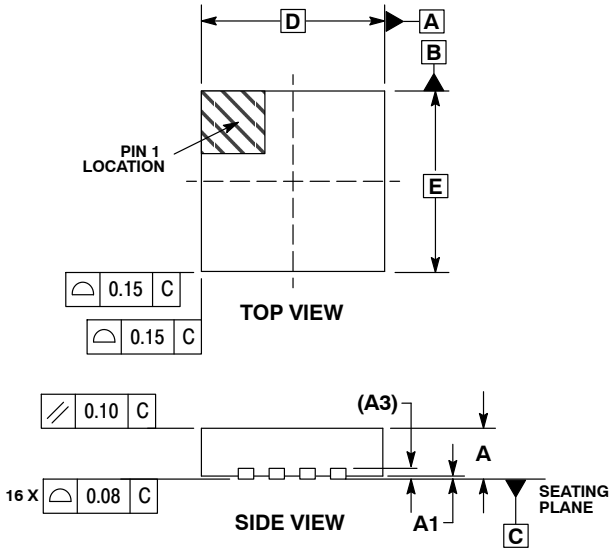


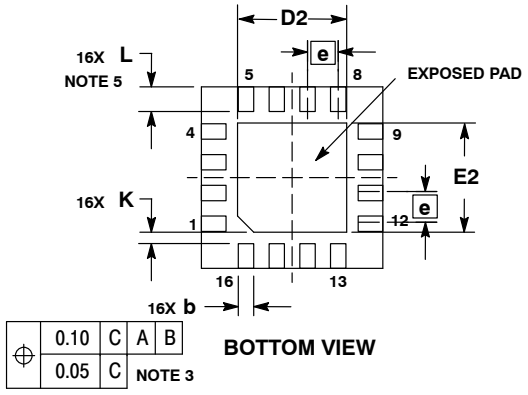

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.40 MAX | |
| A1 | 0.25 | 0.35 |
| A2 | 1.20 REF | |
| b | 0.30 | 0.50 |
| D | 4.00 BSC | |
| E | 4.00 BSC | |
| e | 1.00 BSC | |
| S | 0.50 BSC | |

## PACKAGE DIMENSIONS

**16 PIN QFN**
CASE 485G−01
ISSUE C

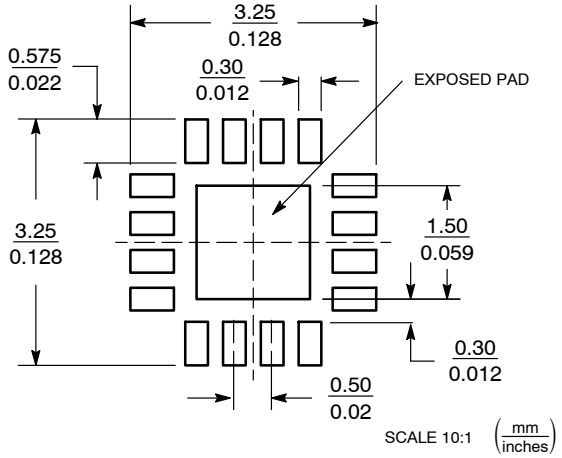



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. $L_{max}$ CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 3.00 BSC | |
| D2 | 1.65 | 1.85 |
| E | 3.00 BSC | |
| E2 | 1.65 | 1.85 |
| e | 0.50 BSC | |
| K | 0.18 TYP | |
| L | 0.30 | 0.50 |

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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