Low Power RTC with Battery Backed SRAM, Integrated ±5ppm Temperature Compensation and Auto Daylight Saving

ISL12022MR5421

The ISL12022MR5421 device is a low power real time clock (RTC) with an embedded temperature sensor and crystal. Device functions include oscillator compensation, clock/calendar, power fail and low battery monitors, brownout indicator, one-time, periodic or polled alarms, intelligent battery backup switching, Battery Reseal™ function and 128 bytes of battery-backed user SRAM. The device is offered in a 20 Ld SOIC module that contains the RTC and an embedded 32.768kHz quartz crystal. The calibrated oscillator provides less than ±5ppm drift over the full -40°C to +85°C temperature range.

The RTC tracks time with separate registers for hours, minutes, and seconds. The calendar registers track date, month, year and day of the week and are accurate through 2099, with automatic leap year correction.

Daylight Savings time adjustment is done automatically, using parameters entered by the user. Power fail and battery monitors offer user-selectable trip levels. The time stamp function records the time and date of switchover from V_{DD} to V_{BAT} power, and also from V_{BAT} to V_{DD} power.

The ISL12022MR5421 has redesign package to increase Contact and Air Discharge ESD performance.

Related Literature

- See AN1549 “Addressing Power Issues in Real Time Clock Applications”

Features

- Embedded 32.768kHz Quartz Crystal in the Package
- 20 Ld SOIC Package (for DFN version, refer to the ISL12020M)
- Calendar
- On-chip Oscillator Temperature Compensation
- 10-bit Digital Temperature Sensor Output
- 15 Selectable Frequency Outputs
- Interrupt for Alarm or 15 Selectable Frequency Outputs
- Automatic Backup to Battery or Supercapacitor
- VDD and Battery Status Monitors
- Battery Reseal™ Function to Extend Battery Shelf Life
- Power Status Brownout Monitor
- Time Stamp for Battery Switchover
- 128 Bytes Battery-Backed User SRAM
- I^2C-Bus™
- RoHS Compliant

Applications

- Utility Meters
- POS Equipment
- Printers and Copiers
- Digital Cameras

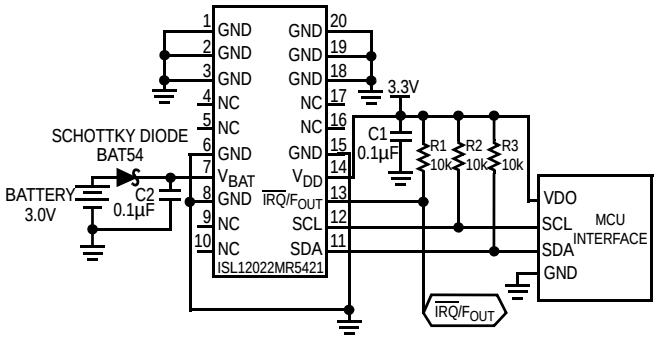


FIGURE 1. TYPICAL APPLICATION CIRCUIT

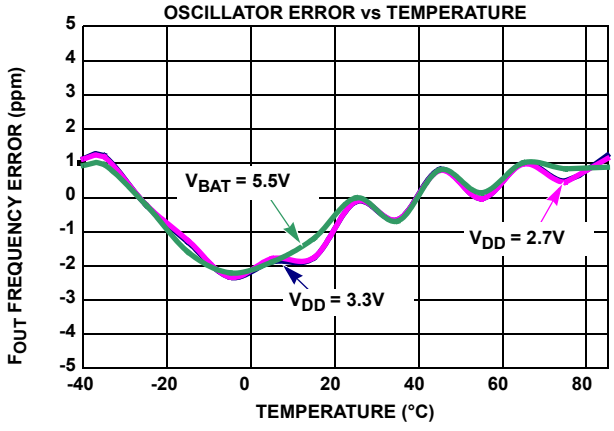
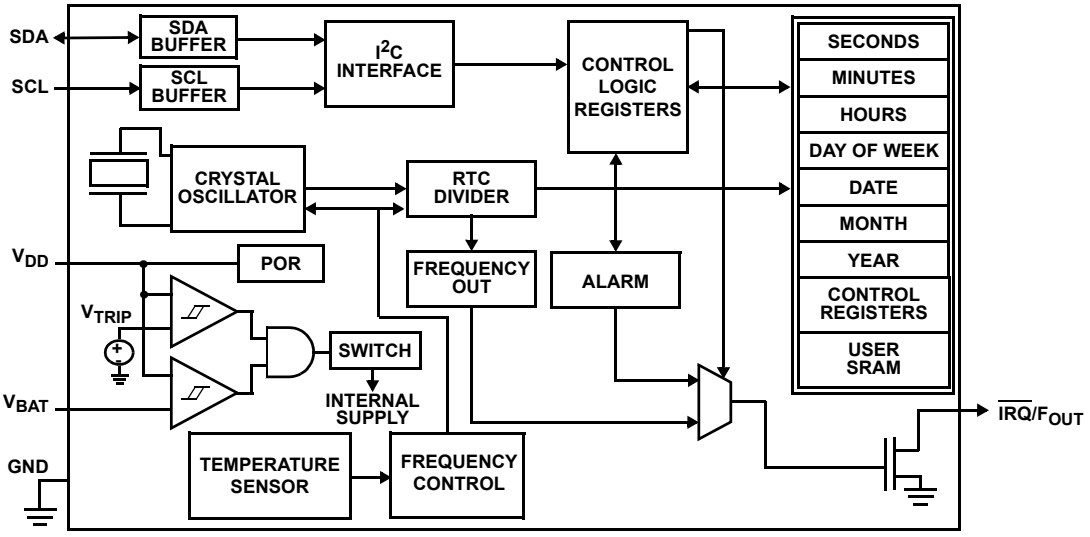


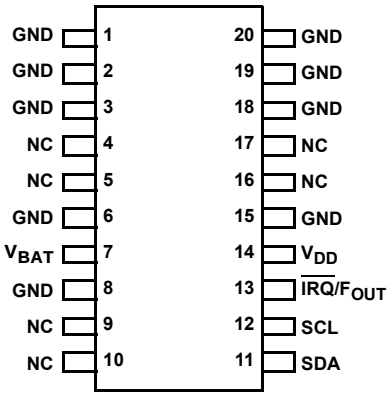
FIGURE 2. PERFORMANCE CURVE

Block Diagram



Pin Configuration

ISL12022MR5421
(20 LD SOIC)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
4, 5, 9, 10, 16, 17	NC	**No Connection**. Do not connect to a signal or supply voltage.
7	V_{BAT}	**Backup Supply**. This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin can be connected to a battery, a supercapacitor or tied to ground if not used. See the Battery Monitor parameter in the “DC Operating Characteristics-RTC” table on page 6. This pin should be tied to ground if not used.
11	SDA	**Serial Data**. SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be OR’ed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode. An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I^2C interface speeds. It is disabled when the backup power supply on the V_{BAT} pin is activated.
12	SCL	**Serial Clock**. The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the backup power supply on the V_{BAT} pin is activated to minimize power consumption.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
13	$\overline{IRQ}/F_{OUT}$	**Interrupt Output/Frequency Output** (Default 32.768kHz frequency output). This dual function pin can be used as an interrupt or frequency output pin. The $\overline{IRQ}/F_{OUT}$ mode is selected via the frequency out control bits of the control/status register. **Interrupt Mode**. The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active low output. **Frequency Output Mode**. The pin outputs a clock signal, which is related to the crystal frequency. The frequency output is user selectable and enabled via the I^2C bus. It is an open drain output. The output is open drain and requires a pull-up resistor.
14	V_{DD}	**Power Supply**. Chip power supply and ground pins. The device will operate with a power supply from V_{DD} = 2.7V to 5.5VDC. A 0.1µF capacitor is recommended on the V_{DD} pin to ground.
1, 2, 3, 6, 8, 15, 18, 19, 20	GND	**Ground Pin**.

Ordering Information

PART NUMBER	PART MARKING	V_{DD} RANGE (V)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL12022MIBZR5421 (Note 2)	ISL12022MIBZ R5421	2.7 to 5.5	-40 to +85	20 Ld SOIC	M20.3
ISL12022MIBZ-TR5421 (Notes 1, 2)	ISL12022MIBZ R5421	2.7 to 5.5	-40 to +85	20 Ld SOIC (Tape and Reel)	M20.3

1. Please refer to TB347 for details on reel specifications.
2. These Intersil plastic packaged products employ special material sets, molding compounds and 100% matte tin plate plus anneal (e3) termination finish. These products do contain Pb but they are RoHS compliant by exemption 7 (lead in high melt temp solder for internal connections) and exemption 5 (lead in piezoelectric elements). These Intersil RoHS compliant products are compatible with both SnPb and Pb free soldering operations. These Intersil RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Table of Contents

Absolute Maximum Ratings

Voltage on V_{DD}, V_{BAT} and $\overline{IRQ}/F_{OUT}$ Pins
(Respect to Ground) . . . . . -0.3V to 6.0V
Voltage on SCL and SDA Pins
(Respect to Ground) . . . . . -0.3V to V_{DD} + 0.3V
ESD Rating
Human Body Model
(Per MIL-STD-883 Method 3014) . . . . . >3kV
Machine Model . . . . . >300V
Charge Discharge Model . . . . . >2200V
Latch-up (Tested per JESD-78B, Class 2, Level A 100mA
Shock Resistance . . . . . 5000g, 0.3ms, 1/2 sine
Vibration (Ultrasound cleaning not advised) 20g/10-2000Hz,

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Lead SOIC (Notes 3, 4)	70	35

Storage Temperature . . . . . -40°C to +85°C
Pb-Free Reflow Profile (Note 5). . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is on top of the package and measured in the center of the package between Pins 6 and 15.
5. The ISL12022MR5421 Oscillator Initial Accuracy can change after solder reflow attachment. The amount of change will depend on the reflow temperature and length of exposure. A general rule is to use only one reflow cycle and keep the temperature and time as short as possible. Changes on the order of ±1ppm to ±3ppm can be expected with typical reflow profiles.

DC Operating Characteristics RTC

Test Conditions: V_{DD} = +2.7 to +5.5V, T_A = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS	NOTES
V_{DD}	Main Power Supply	(Note 14)	**2.7**		**5.5**	V	
V_{BAT}	Battery Supply Voltage	(Note 14)	**1.8**		**5.5**	V	8
I_{DD1}	Supply Current. (I^2C Not Active, Temperature Conversion Not Active, F_{OUT} Not Active)	V_{DD} = 5V		4.1	**15**	µA	9, 10
		V_{DD} = 3V		3.5	**14**	µA	9, 10
I_{DD2}	Supply Current. (I^2C Active, Temperature Conversion Not Active, F_{out} Not Active)	V_{DD} = 5V		200	**500**	µA	9, 10
I_{DD3}	Supply Current. (I^2C Not Active, Temperature Conversion Active, F_{OUT} Not Active)	V_{DD} = 5V		120	**400**	µA	9, 10
I_{BAT}	Battery Supply Current	V_{DD} = 0V, V_{BAT} = 3V, T_A = +25°C		1.0	1.6	µA	9
		V_{DD} = 0V, V_{BAT} = 3V		1.0	**5.0**	µA	9
I_{BATLKG}	Battery Input Leakage	V_{DD} = 5.5V, V_{BAT} = 1.8V			**100**	nA	
I_{LI}	Input Leakage Current on SCL	V_{IL} = 0V, V_{IH} = V_{DD}	**-1.0**	±0.1	**1.0**	µA	
I_{LO}	I/O Leakage Current on SDA	V_{IL} = 0V, V_{IH} = V_{DD}	**-1.0**	±0.1	**1.0**	µA	
V_{BATM}	Battery Level Monitor Threshold		**-100**		**+100**	mV	
V_{PBM}	Brownout Level Monitor Threshold		**-100**		**+100**	mV	
V_{TRIP}	V_{BAT} Mode Threshold	(Note 14)	**2.0**	2.2	**2.4**	V	
$V_{TRIPHYS}$	V_{TRIP} Hysteresis			30		mV	12
V_{BATHYS}	V_{BAT} Hysteresis			50		mV	12

DC Operating Characteristics RTC

Test Conditions: V_{DD} = +2.7 to +5.5V, T_A = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS	NOTES
OSCILLATOR ACCURACY							
$\Delta Fout_I$	Oscillator Initial Accuracy	V_{DD} = 3.3V	**-2**		**+8**	ppm	5, 16
$\Delta Fout_R$	Oscillator Accuracy after Reflow Cycle	V_{DD} = 3.3V		±5		ppm	5, 16
$\Delta Fout_T$	Oscillator Stability vs Temperature	V_{DD} = 3.3V		±2		ppm	5, 17
$\Delta Fout_V$	Oscillator Stability vs Voltage	2.7V ≤ V_{DD} ≤ 5.5V	**-3**		**+3**	ppm	18
Temp	Temperature Sensor Accuracy	V_{DD} = V_{BAT} = 3.3V		±2		°C	12
$\overline{IRQ}/F_{OUT}$ **(OPEN DRAIN OUTPUT)**							
V_{OL}	Output Low Voltage	V_{DD} = 5V, I_{OL} = 3mA			**0.4**	V	
		V_{DD} = 2.7V, I_{OL} = 1mA			**0.4**	V	

Power-Down Timing

Test Conditions: V_{DD} = +2.7 to +5.5V, Temperature = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS	NOTES
V_{DDSR-}	V_{DD} Negative Slew Rate				**10**	V/ms	11
V_{DDSR+}	V_{DD} Positive Slew Rate, Minimum			0.05		V/ms	15

I^2C Interface Specifications

Test Conditions: V_{DD} = +2.7 to +5.5V, Temperature = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS	NOTES
V_{IL}	SDA and SCL Input Buffer LOW Voltage		**-0.3**		**0.3 x V_{DD}**	V	
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		**0.7 x V_{DD}**		**V_{DD} + 0.3**	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis			0.05 x V_{DD}		V	12, 13
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA	V_{DD} = 5V, I_{OL} = 3mA	**0**	0.02	**0.4**	V	
C_{PIN}	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF	12, 13
f_{SCL}	SCL Frequency				**400**	kHz	
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			**50**	ns	
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window.			**900**	ns	
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition.	**1300**			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing.	**1300**			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing.	**600**			ns	

I^2C Interface Specifications

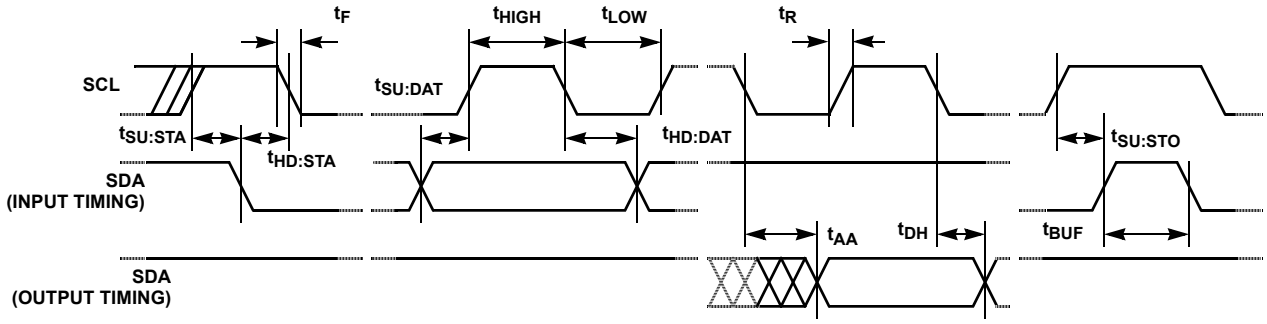
Test Conditions: V_{DD} = +2.7 to +5.5V, Temperature = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS	NOTES
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}.	600			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}.	600			ns	
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}.	100			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window.	20		900	ns	
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}.	600			ns	
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}.	600			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window.	0			ns	
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}.	20 + 0.1 x Cb		300	ns	12, 13
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}.	20 + 0.1 x Cb		300	ns	12, 13
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF	12, 13
R_{PU}	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ~2.5kΩ. For Cb = 40pF, max is about 15kΩ~20kΩ	1			kΩ	12, 13

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Specified at +25°C.
8. Temperature Conversion is inactive below V_{BAT} = 2.7V. Device operation is not guaranteed at V_{BAT} <1.8V.
9. $\overline{IRQ}/F_{OUT}$ inactive.
10. $V_{DD} > V_{BAT} + V_{BATHYS}$
11. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
12. Limits should be considered typical and are not production tested.
13. These are I^2C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.
14. Minimum V_{DD} and/or V_{BAT} of 1V to sustain the SRAM. The value is based on characterization and it is not tested.
15. To avoid EEPROM recall issues, it is advised to use this minimum power-up slew rate. Not tested; shown as typical only.
16. Defined as the deviation from a target oscillator frequency of 32,768.0Hz at room temperature.
17. Defined as the deviation from the room temperature measured 1Hz frequency, V_{DD} = 3.3V, at T_A = -40°C to +85°C.
18. Defined as the deviation at room temperature from the measured 1Hz frequency (or equivalent) at V_{DD} = 3.3, over the range of V_{DD} = 2.7V to V_{DD} = 5.5V.

SDA vs SCL Timing



EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{DD} = 5V

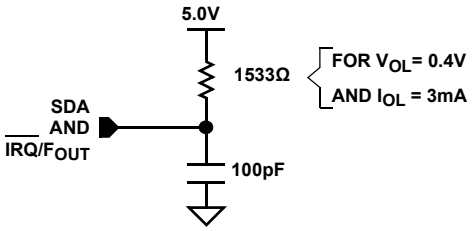


FIGURE 3. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 5.0V

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LO W	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Typical Performance Curves

Temperature is +25°C unless otherwise specified.

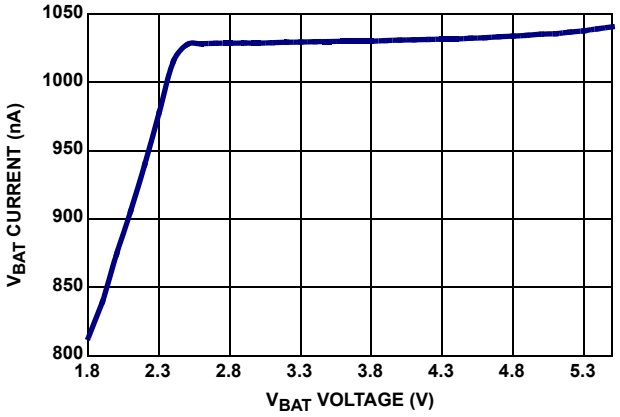


FIGURE 4. I_{BAT} vs V_{BAT} (V_{DD} = 0V)

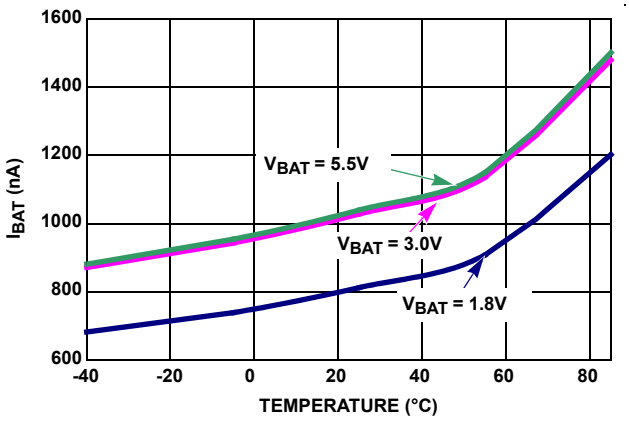


FIGURE 5. I_{BAT} vs TEMPERATURE (V_{DD} = 0V)

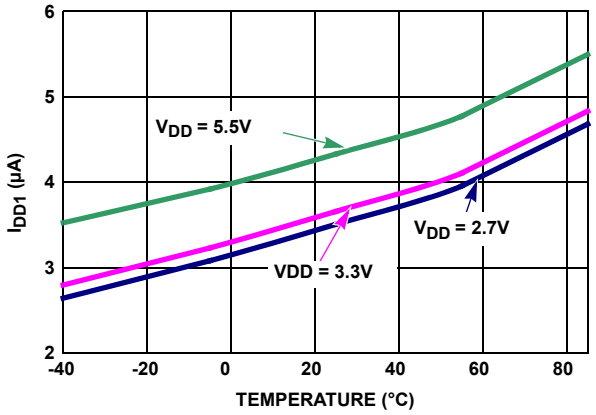


FIGURE 6. I_{DD1} vs TEMPERATURE

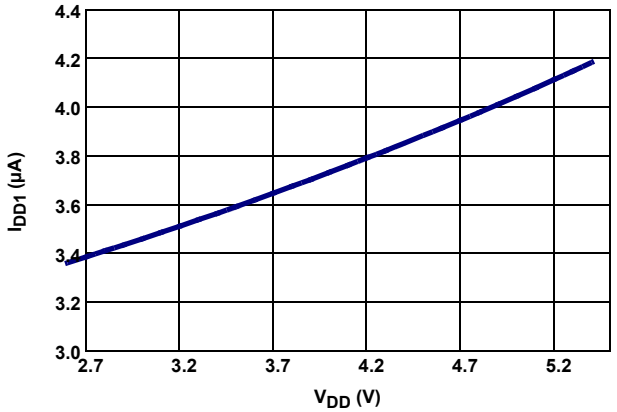


FIGURE 7. I_{DD1} vs V_{DD}

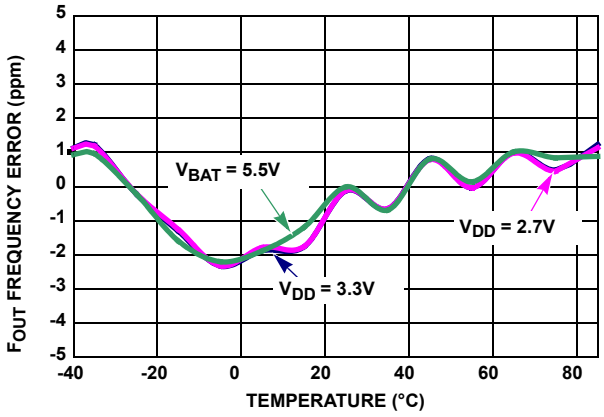


FIGURE 8. OSCILLATOR ERROR vs TEMPERATURE

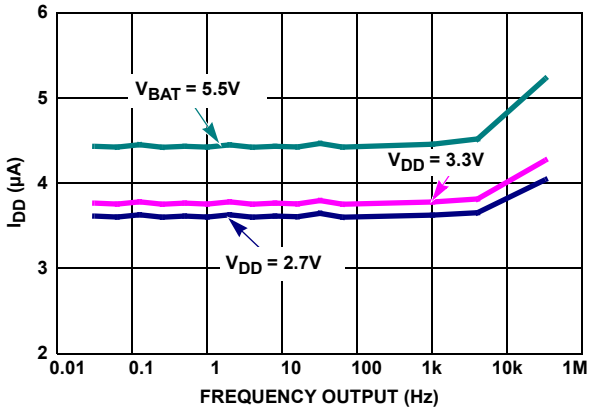


FIGURE 9. F_{OUT} vs I_{DD}

Typical Performance Curves

Temperature is +25°C unless otherwise specified. **(Continued)**

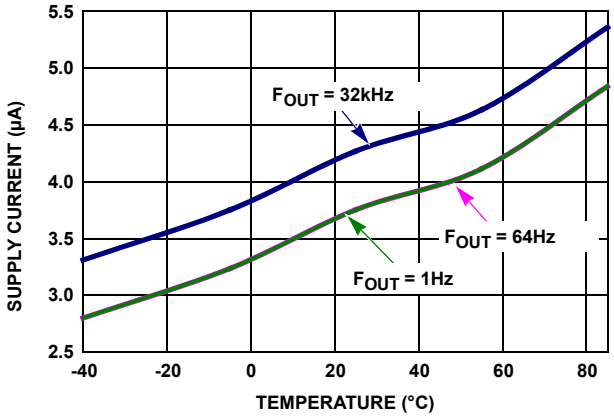


FIGURE 10. I_{DD} vs TEMPERATURE, 3 DIFFERENT F_{OUT}

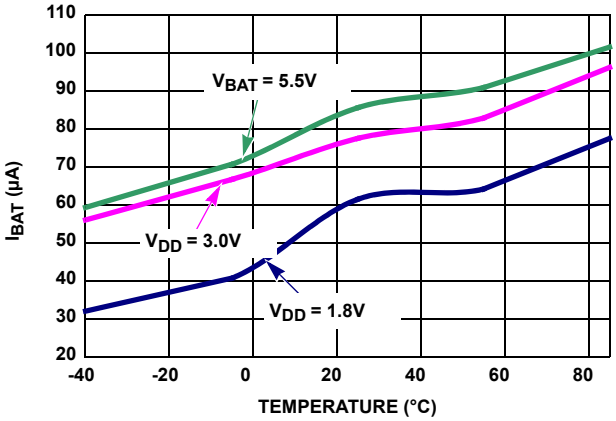


FIGURE 11. I_{BAT} WITH TSE = 1, BTSE = 1 vs TEMPERATURE

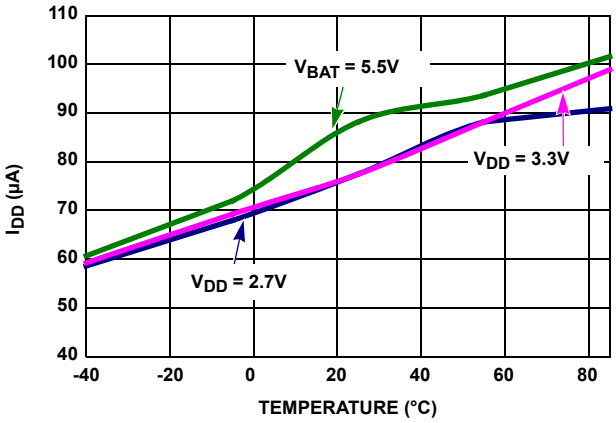


FIGURE 12. I_{DD} WITH TSE = 1 vs TEMPERATURE

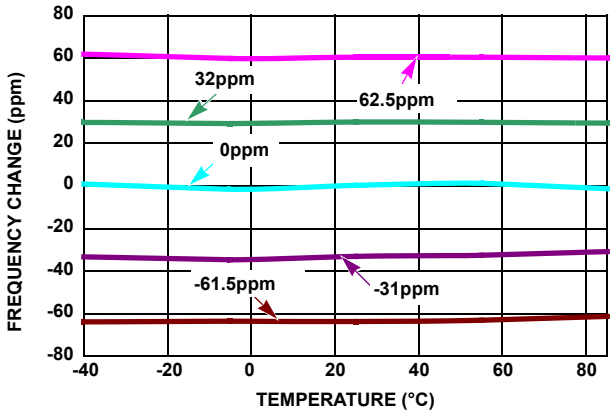


FIGURE 13. OSCILLATOR CHANGE vs TEMPERATURE AT DIFFERENT AGING SETTINGS (IATR) (BETA SET FOR 1ppm STEPS)

General Description

The ISL12022MR5421 device is a low power real time clock (RTC) with embedded temperature sensor and crystal. It contains crystal frequency compensation circuitry over the operating temperature range good to ±5ppm accuracy. It also contains a clock/calendar with Daylight Savings Time (DST) adjustment, power fail and low battery monitors, brownout indicator, 1 periodic or polled alarm, intelligent battery backup switching and 128 Bytes of battery-backed user SRAM.

The oscillator uses an internal 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction. In addition, the ISL12022MR5421 can be programmed for automatic Daylight Saving Time (DST) adjustment by entering local DST information.

The ISL12022MR5421's alarm can be set to any clock/calendar value for a match. For example, every minute, every Tuesday or at 5:23 AM on March 21. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the $\overline{IRQ}/F_{OUT}$ pin. There is a repeat mode for the alarm allowing a periodic interrupt every minute, every hour, every day, etc.

The device also offers a backup power input pin. This V_{BAT} pin allows the device to be backed up by battery or supercapacitor with automatic switchover from V_{DD} to V_{BAT}. The ISL12022MR5421 device is specified for V_{DD} = 2.7V to 5.5V and the clock/calendar portion of the device remains fully operational in battery backup mode down to 1.8V (Standby Mode). The V_{BAT} level is monitored and reported against preselected levels. The first report is registered when the V_{BAT} level falls below 85% of nominal level; the second level is set for 75%. Battery levels are stored in PWR_VBAT registers.

The ISL12022MR5421 offers a "Brownout" alarm once the V_{DD} falls below a pre-selected trip level. This allows system Micro to save vital information to memory before complete power loss. There are six V_{DD} levels that could be selected for initiation of the Brownout alarm.

Functional Description

Power Control Operation

The power control circuit accepts a V_{DD} and a V_{BAT} input. Many types of batteries can be used with Intersil RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power the ISL12022MR5421 for up to 10 years. Another option is to use a supercapacitor for applications where V_{DD} is interrupted for up to a month. See the "Application Section" on page 27 for more information.

Normal Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

To transition from the V_{DD} to V_{BAT} mode, both of the following conditions must be met:

Condition 1:

$V_{DD} < V_{BAT} - V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} < V_{TRIP}$
where $V_{TRIP} \approx 2.2V$

Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

The ISL12022MR5421 device will switch from the V_{BAT} to V_{DD} mode when one of the following conditions occurs:

Condition 1:

$V_{DD} > V_{BAT} + V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} > V_{TRIP} + V_{TRIPHYS}$
where $V_{TRIPHYS} \approx 30mV$

These power control situations are illustrated in Figures 14 and 15.

The I^2C bus is deactivated in battery backup mode to reduce power consumption. Aside from this, all RTC functions are operational during battery backup mode. Except for SCL and SDA, all the inputs and outputs of the ISL12022MR5421 are active during battery backup mode unless disabled via the control register.

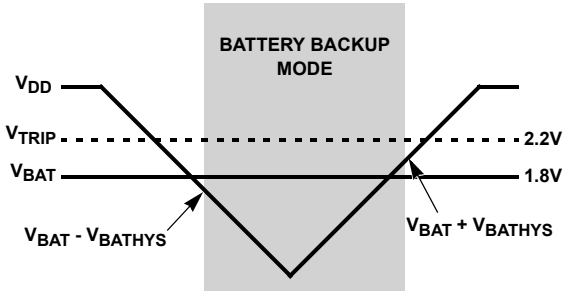


FIGURE 14. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$

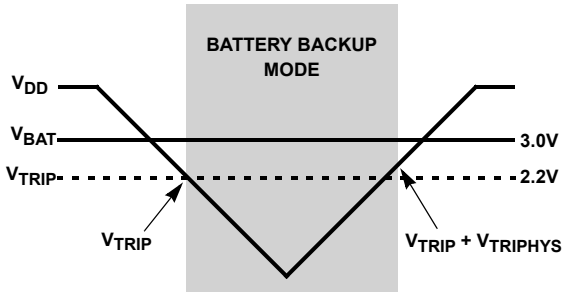


FIGURE 15. BATTERY SWITCHOVER WHEN $V_{BAT} > V_{TRIP}$

The device Time Stamps the switchover from V_{DD} to V_{BAT} and V_{BAT} to V_{DD}, and the time is stored in t_{SV2B} and t_{SB2V} registers respectively. If multiple V_{DD} power-down sequences occur before the status is read, the earliest V_{DD} to V_{BAT} power-down time is stored and the most recent V_{BAT} to V_{DD} time is stored.

Temperature conversion and compensation can be enabled in battery backup mode. Bit BTSE in the BETA register controls this operation, as described in "BETA Register (BETA)" on page 19.

Power Failure Detection

The ISL12022MR5421 provides a Real Time Clock Failure Bit (RTCF) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (both V_{DD} and V_{BAT}).

Brownout Detection

The ISL12022MR5421 monitors the V_{DD} level continuously and provides warning if the V_{DD} level drops below prescribed levels. There are six (6) levels that can be selected for the trip level. These values are 85% below popular V_{DD} levels. The LVDD bit in the Status Register will be set to "1" when brownout is detected. Note that the I^2C serial bus remains active unless the Battery V_{TRIP} levels are reached.

Battery Level Monitor

The ISL12022MR5421 has a built-in warning feature once the backup battery level drops first to 85% and then to 75% of the battery's nominal V_{BAT} level. When the battery voltage drops to between 85% and 75%, the LBAT85 bit is set in the status register. When the level drops below 75%, both LBAT85 and LBAT75 bits are set in the status register.

The battery level monitor is not functional in battery backup mode. In order to read the monitor bits after powering up V_{DD}, instigate a battery level measurement by setting the TSE bit to "1" (BETA register), and then read the bits.

There is a Battery Time Stamp Function available. Once the V_{DD} is low enough to enable switchover to the battery, the RTC time/date are written into the TSV2B register. This information can be read from the TSV2B registers to discover the point in time of the V_{DD} power-down. If there are multiple power-down cycles before reading these registers, the first values stored in these registers will be retained. These registers will hold the original power-down value until they are cleared by setting CLRTS = 1 to clear the registers.

The normal power switching of the ISL12022MR5421 is designed to switch into battery backup mode only if the V_{DD} power is lost. This will ensure that the device can accept a wide range of backup voltages from many types of sources while reliably switching into backup mode.

Note that the ISL12022MR5421 is not guaranteed to operate with V_{BAT} < 1.8V. If the battery voltage is expected to drop lower than this minimum, correct operation of the device, (especially after a V_{DD} power-down cycle) is not guaranteed.

The minimum V_{BAT} to insure SRAM is stable is 1.0V. Below that, the SRAM may be corrupted when V_{DD} power resumes.

Real Time Clock Operation

The Real Time Clock (RTC) uses an integrated 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24-hour or AM/PM format. When the ISL12022MR5421 powers up after the loss of both V_{DD} and V_{BAT}, the clock will not begin incrementing until at least one byte is written to the clock register.

Single Event and Interrupt

The alarm mode is enabled via the MSB bit. Choosing single event or interrupt alarm mode is selected via the IM bit. Note that when the frequency output function is enabled, the alarm function is disabled.

The standard alarm allows for alarms of time, date, day of the week, month, and year. When a time alarm occurs in single event mode, the $\overline{IRQ}/F_{OUT}$ pin will be pulled low and the alarm status bit (ALM) will be set to “1”.

The pulsed interrupt mode allows for repetitive or recurring alarm functionality. Hence, once the alarm is set, the device will continue to alarm for each occurring match of the alarm and present time. Thus, it will alarm as often as every minute (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During pulsed interrupt mode, the $\overline{IRQ}/F_{OUT}$ pin will be pulled low for 250ms and the alarm status bit (ALM) will be set to “1”.

The ALM bit can be reset by the user or cleared automatically using the auto reset mode (see ARST bit). The alarm function can be enabled/disabled during battery backup mode using the FOBATB bit. For more information on the alarm, please see “ALARM Registers (10h to 15h)” on page 21.

Frequency Output Mode

The ISL12022MR5421 has the option to provide a clock output signal using the $\overline{IRQ}/F_{OUT}$ open drain output pin. The frequency output mode is set by using the FO bits to select 15 possible output frequency values from 1/32Hz to 32kHz. The frequency output can be enabled/disabled during Battery Backup mode using the FOBATB bit.

General Purpose User SRAM

The ISL12022MR5421 provides 128 bytes of user SRAM. The SRAM will continue to operate in battery backup mode. However, it should be noted that the I^2C bus is disabled in battery backup mode.

I^2C Serial Interface

The ISL12022MR5421 has an I^2C serial bus interface that provides access to the control and status registers and the user SRAM. The I^2C serial interface is compatible with other industry I^2C serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

Oscillator Compensation

The ISL12022MR5421 provides both initial timing correction and temperature correction due to variation of the crystal oscillator. Analog and digital trimming control is provided for initial adjustment, and a temperature compensation function is provided to automatically correct for temperature drift of the crystal. Initial values for the initial AT and DT settings (ITR0), temperature coefficient (ALPHA), crystal capacitance (BETA), as well as the crystal turn-over temperature (XTO), are preset internally and recalled to RAM registers on power-up. The compensation function can be enabled/disabled at any time and can be used in battery mode as well.

Register Descriptions

The battery-backed registers are accessible following a slave byte of “1101111x” and reads or writes to addresses [00h:2Fh]. The defined addresses and default values are described in the Table 1. The battery backed general purpose SRAM has a different slave address (1010111x), so it is not possible to read/write that section of memory while accessing the registers.

REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 8 sections. They are:

1. Real Time Clock (7 bytes): Address 00h to 06h.
2. Control and Status (9 bytes): Address 07h to 0Fh.
3. Alarm (6 bytes): Address 10h to 15h.
4. Time Stamp for Battery Status (5 bytes): Address 16h to 1Ah.
5. Time Stamp for V_{DD} Status (5 bytes): Address 1Bh to 1Fh.
6. Day Light Saving Time (8 bytes): 20h to 27h.
7. TEMP (2 bytes): 28h to 29h.
8. Crystal Net PPM Correction, NPPM (2 bytes): 2Ah, 2Bh
9. Crystal Turnover Temperature, XT0 (1 byte): 2Ch
10. Crystal ALPHA at high temperature, ALPHA_H (1 byte): 2Dh
11. Scratch Pad (2 bytes): Address 2Eh and 2Fh

Write capability is allowable into the RTC registers (00h to 06h) only when the WRTC bit (bit 6 of address 08h) is set to “1”. A multi-byte read or write operation should be limited to one section per operation for best RTC time keeping performance.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC and Alarm registers, the read instruction latches all clock registers into a buffer, so an update of the clock

does not change the time being read. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register. When the previous address is 2Fh, the next address will wrap around to 00h.

It is not necessary to set the WRTC bit prior to writing into the control and status, alarm, and user SRAM registers.

TABLE 1. REGISTER MEMORY MAP (YELLOW SHADING INDICATES READ-ONLY BITS)

ADDR.	SECTION	REG NAME	BIT								RANGE	DEFAULT
			7	6	5	4	3	2	1	0		
00h	RTC	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0 to 59	00h
01h		MN	0	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0 to 59	00h
02h		HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0 to 23	00h
03h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1 to 31	01h
04h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1 to 12	01h
05h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0 to 99	00h
06h		DW	0	0	0	0	0	DW2	DW1	DW0	0 to 6	00h
07h	CSR	SR	BUSY	OSCF	DSTADJ	ALM	LVDD	LBAT85	LBAT75	RTCF	N/A	01h
08h		INT	ARST	WRTC	IM	FOBATB	FO3	FO2	FO1	FO0	N/A	01h
09h		PWR_VDD	CLRTS	D	D	D	D	V_{DD}Trip2	V_{DD}Trip1	V_{DD}Trip0	N/A	00h
0Ah		PWR_VBAT	D	RESEALB	VB85Tp2	VB85Tp1	VB85Tp0	VB75Tp2	VB75Tp1	VB75Tp0	N/A	00h
0Bh		ITRO	IDTR01	IDTR00	IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	N/A	XXh
0Ch		ALPHA	D	ALPHA6	ALPHA5	ALPHA4	ALPHA3	ALPHA2	ALPHA1	ALPHA0	N/A	XXh
0Dh		BETA	TSE	BTSE	BTSR	BETA4	BETA3	BETA2	BETA1	BETA0	N/A	XXh
0Eh		FATR	0	0	FFATR5	FATR4	FATR3	FATR2	FATR1	FATR0	N/A	00h
0Fh		FDTR	0	0	0	FDTR4	FDTR3	FDTR2	FDTR1	FDTR0	N/A	00h
10h	ALARM	SCA0	ESCA0	SCA022	SCA021	SCA020	SCA013	SCA012	SCA011	SCA010	00 to 59	00h
11h		MNA0	EMNA0	MNA022	MNA021	MNA020	MNA013	MNA012	MNA011	MNA010	00 to 59	00h
12h		HRA0	EHRA0	D	HRA021	HRA020	HRA013	HRA012	HRA011	HRA010	0 to 23	00h
13h		DTA0	EDTA0	D	DTA021	DTA020	DTA013	DTA012	DTA011	DTA010	01 to 31	00h
14h		MOA0	EMOA00	D	D	MOA020	MOA013	MOA012	MOA011	MOA010	01 to 12	00h
15h		DWA0	EDWA0	D	D	D	D	DWA02	DWA01	DWA00	0 to 6	00h
16h	TSV2B	VSC	0	VSC22	VSC21	VSC20	VSC13	VSC12	VSC11	VSC10	0 to 59	00h
17h		VMN	0	VMN22	VMN21	VMN20	VMN13	VMN12	VMN11	VMN10	0 to 59	00h
18h		VHR	VMIL	0	VHR21	VHR20	VHR13	VHR12	VHR11	VHR10	0 to 23	00h
19h		VDT	0	0	VDT21	VDT20	VDT13	VDT12	VDT11	VDT10	1 to 31	00h
1Ah		VMO	0	0	0	VMO20	VMO13	VMO12	VMO11	VMO10	1 to 12	00h
1Bh	TSB2V	BSC	0	BSC22	BSC21	BSC20	BSC13	BSC12	BSC11	BSC10	0 to 59	00h
1Ch		BMN	0	BMN22	BMN21	BMN20	BMN13	BMN12	BMN11	BMN10	0 to 59	00h
1Dh		BHR	BMIL	0	BHR21	BHR20	BHR13	BHR12	BHR11	BHR10	0 to 23	00h
1Eh		BDT	0	0	BDT21	BDT20	BDT13	BDT12	BDT11	BDT10	1 to 31	00h
1Fh		BMO	0	0	0	BMO20	BMO13	BMO12	BMO11	BMO10	1 to 12	00h

TABLE 1. REGISTER MEMORY MAP (YELLOW SHADING INDICATES READ-ONLY BITS) (Continued)

ADDR.	SECTION	REG NAME	BIT 7	6	5	4	3	2	1	0	RANGE	DEFAULT
20h	DSTCR	DstMoFd	DSTE	D	D	DstMoFd20	DstMoFd13	DstMoFd12	DstMoFd11	DstMoFd10	1 to 12	00h
21h		DstDwFd	D	DstDwFdE	DstWkFd12	DstWkFd11	DstWkFd10	DstDwFd12	DstDwFd11	DstDwFd10	0 to 6	00h
22h		DstDtFd	D	D	DstDtFd21	DstDtFd20	DstDtFd13	DstDtFd12	DstDtFd11	DstDtFd10	1 to 31	00h
23h		DstHrFd	D	D	DstHrFd21	DstHrFd20	DstHrFd13	DstHrFd12	DstHrFd11	DstHrFd10	0 to 23	00h
24h		DstMoRv	D	D	D	DstMoRv20	DstMoRv13	DstMoR12v	DstMoRv11	DstMoRv10	01 to 12	00h
25h		DstDwRv	D	DstDwRvE	DstWkrv12	DstWkRv11	DstWkRv10	DstDwRv12	DstDwRv11	DstDwRv10	0 to 6	00h
26h		DstDtRv	D	D	DstDtRv21	DstDtRv20	DstDtRv13	DstDtRv12	DstDtRv11	DstDtRv10	01 to 31	00h
27h		DstHrRv	D	D	DstHrRv21	DstHrRv20	DstHrRv13	DstHrRv12	DstHrRv11	DstHrRv10	0 to 23	00h
28h	TEMP	TK0L	TK07	TK06	TK05	TK04	TK03	TK02	TK01	TK00	00 to FF	00h
29h		TK0M	0	0	0	0	0	0	TK09	TK08	00 to 03	00h
2Ah	NPPM	NPPML	NPPM7	NPPM6	NPPM5	NPPM4	NPPM3	NPPM2	NPPM1	NPPM0	00 to FF	00h
2Bh		NPPMH	0	0	0	0	0	NPPM10	NPPM9	NPPM8	00 to 07	00h
2Ch	XT0	XT0	D	D	D	XT4	XT3	XT2	XT1	XT0	00 to FF	XXh
2Dh	ALPHAH	ALPHAH	D	ALP_H6	ALP_H5	ALP_H4	ALP_H3	ALP_H2	ALP_H1	ALP_H0	00 to 7F	XXh
2Eh	GPM	GPM1	GPM17	GPM16	GPM15	GPM14	GPM13	GPM12	GPM11	GPM10	00 to FF	00h
2Fh		GPM2	GPM27	GPM26	GPM25	GPM24	GPM23	GPM22	GPM21	GPM20	00 to FF	00h

Real Time Clock Registers

Addresses [00h to 06h]

RTC REGISTERS (SC, MN, HR, DT, MO, YR, DW)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 0 to 59, HR (Hour) can either be a 12-hour or 24-hour mode, DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99, and DW (Day of the Week) is 0 to 6.

The DW register provides a Day of the Week status and uses three bits (DW2 to DW0) to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-...
The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as “0”.

24-HOUR TIME

If the MIL bit of the HR register is “1”, the RTC uses a 24-hour format. If the MIL bit is “0”, the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a “1” representing PM. The clock defaults to 12-hour format time with HR21 = “0”.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year and the year 2100 is not. The ISL12022MR5421 does not correct for the leap year in the year 2100.

Control and Status Registers (CSR)

Addresses [07h to 0Fh]

The Control and Status Registers consist of the Status Register, Interrupt and Alarm Register, Analog Trimming and Digital Trimming Registers.

STATUS REGISTER (SR)

The Status Register is located in the memory map at address 07h. This is a volatile register that provides either control or status of RTC failure (RTCF), Battery Level Monitor (LBAT85, LBAT75), alarm trigger, Daylight Saving Time, crystal oscillator

enable and temperature conversion in progress bit.

TABLE 2. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
07h	BUSY	OSCF	DSTDJ	ALM	LVDD	LBAT85	LBAT75	RTCF

BUSY BIT (BUSY)

Busy Bit indicates temperature sensing is in progress. In this mode, Alpha, Beta and ITRO registers are disabled and cannot be accessed.

OSCILLATOR FAIL BIT (OSCF)

Oscillator Fail Bit indicates that the oscillator has failed. The oscillator frequency is either zero or very far from the desired 32.768kHz due to failure, PC board contamination or mechanical issues.

DAYLIGHT SAVING TIME CHANGE BIT (DSTADJ)

DSTADJ is the Daylight Saving Time Adjusted Bit. It indicates the daylight saving time forward adjustment has happened. If a DST Forward event happens, DSTADJ will be set to “1”. The DSTADJ bit will stay high when DSTFD event happens, and will be reset to “0” when the DST Reverse event happens. It is read-only and cannot be written. Setting time during a DST forward period will not set this bit to “1”.

The DSTE bit must be enabled when the RTC time is more than one hour before the DST Forward or DST Reverse event time setting, or the DST event correction will not happen.

DSTADJ is reset to “0” upon power-up. It will reset to “0” when the DSTE bit in Register 15h is set to “0” (DST disabled), but no time adjustment will happen.

ALARM BIT (ALM)

This bit announces if the alarm matches the real time clock. If there is a match, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”. An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

LOW V_{DD} INDICATOR BIT (LV_{DD})

This bit indicates when V_{DD} has dropped below the pre-selected trip level (Brownout Mode). The trip points for the brownout levels are selected by three bits: V_{DD} Trip2, V_{DD} Trip1 and V_{DD} Trip0 in PWR_ VDD registers. The LVDD detection is only enabled in V_{DD} mode and the detection happens in real time. The LVDD bit is set whenever the V_{DD} has dropped below the pre-selected trip level, and self clears whenever the V_{DD} is above the pre-selected trip level.

LOW BATTERY INDICATOR 85% BIT (LBAT85)

In Normal Mode (V_{DD}), this bit indicates when the battery level has dropped below the pre-selected trip levels. The trip points are selected by three bits: VB85Tp2, VB85Tp1 and VB85Tp0 in the PWR_VBAT registers. The LBAT85 detection happens automatically once every minute when seconds register reaches 59. The detection can also be manually triggered by setting the TSE bit in BETA register to “1”. The LBAT85 bit is set when the V_{BAT} has dropped below the pre-selected trip level, and will self clear when the V_{BAT} is above the pre-selected trip level at the next detection cycle either by manual or automatic trigger.

In Battery Mode (V_{BAT}), this bit indicates the device has entered into battery mode by polling once every 10 minutes. The LBAT85 detection happens automatically once when the minute register reaches x9h or x0h minutes.

Example - When LBAT85 is Set To “1” In Battery Mode

The minute the register changes to 19h when the device is in battery mode, the LBAT85 is set to “1” the next time the device switches back to Normal Mode.

Example - When LBAT85 Remains at “0” In Battery Mode

If the device enters into battery mode after the minute register reaches 20h and switches back to Normal Mode before the minute register reaches 29h, then the LBAT85 bit will remain at “0” the next time the device switches back to Normal Mode.

LOW BATTERY INDICATOR 75% BIT (LBAT75)

In Normal Mode (V_{DD}), this bit indicates when the battery level has dropped below the pre-selected trip levels. The trip points are selected by three bits: VB75Tp2, VB75Tp1 and VB75Tp0 in the PWR_VBAT registers. The LBAT75 detection happens automatically once every minute when seconds register reaches 59. The detection can also be manually triggered by setting the TSE bit in BETA register to “1”. The LBAT75 bit is set when the V_{BAT} has dropped below the pre-selected trip level, and will self clear when the V_{BAT} is above the pre-selected trip level at the next detection cycle either by manual or automatic trigger.

In Battery Mode (V_{BAT}), this bit indicates the device has entered into battery mode by polling once every 10 minutes. The LBAT85 detection happens automatically once when the minute register reaches x9h or x0h minutes.

Example - When LBAT75 is Set to “1” in Battery Mode

The minute register changes to 30h when the device is in battery mode, the LBAT75 is set to “1” the next time the device switches back to Normal Mode.

Example - When LBAT75 Remains at “0” in Battery Mode

If the device enters into battery mode after the minute register reaches 49h and switches back to Normal Mode before minute register reaches 50h, then the LBAT75 bit will remain at “0” the next time the device switches back to Normal Mode.

REAL TIME CLOCK FAIL BIT (RTCF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL12022MR5421 internally) when the device powers up after having lost all power (defined as V_{DD} = 0V and V_{BAT} = 0V). The bit is set regardless of whether V_{DD} or V_{BAT} is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

Interrupt Control Register (INT)

TABLE 3. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
08h	ARST	WRTC	IM	FOBATB	FO3	FO2	FO1	FO0

AUTOMATIC RESET BIT (ARST)

This bit enables/disables the automatic reset of the ALM, LVDD, LBAT85, and LBAT75 status bits only. When ARST bit is set to "1", these status bits are reset to "0" after a valid read of the respective status register (with a valid STOP condition). When the ARST is cleared to "0", the user must manually reset the ALM, LVDD, LBAT85, and LBAT75 bits.

WRITE RTC ENABLE BIT (WRTC)

The WRTC bit enables or disables write capability into the RTC Timing Registers. The factory default setting of this bit is "0". Upon initialization or power-up, the WRTC must be set to "1" to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle.

INTERRUPT/ALARM MODE BIT (IM)

This bit enables/disables the interrupt mode of the alarm function. When the IM bit is set to "1", the alarm will operate in the interrupt mode, where an active low pulse width of 250ms will appear at the $\overline{IRQ}/F_{OUT}$ pin when the RTC is triggered by the alarm, as defined by the alarm registers (0Ch to 11h). When the IM bit is cleared to "0", the alarm will operate in standard mode, where the $\overline{IRQ}/F_{OUT}$ pin will be set low until the ALM status bit is cleared to "0".

TABLE 4. IM REGISTER

IM BIT	INTERRUPT/ALARM FREQUENCY
0	Single Time Event Set By Alarm
1	Repetitive/Recurring Time Event Set By Alarm

FREQUENCY OUTPUT AND INTERRUPT BIT (FOBATB)

This bit enables/disables the $\overline{IRQ}/F_{OUT}$ pin during battery backup mode (i.e. V_{BAT} power source active). When the FOBATB is set to "1", the $\overline{IRQ}/F_{OUT}$ pin is disabled during battery backup mode. This means that both the frequency output and alarm output functions are disabled. When the FOBATB is cleared to "0", the $\overline{IRQ}/F_{OUT}$ pin is enabled during battery backup mode. Note that the open drain $\overline{IRQ}/F_{OUT}$ pin will need a pull-up to the battery voltage to operate in battery backup mode.

FREQUENCY OUT CONTROL BITS (FO <3:0>)

These bits enable/disable the frequency output function and select the output frequency at the $\overline{IRQ}/F_{OUT}$ pin. See Table 5 for frequency selection. Default for the ISL12022MR5421 is FO<3:0> = 1h, or 32.768kHz output (F_{OUT} is ON). When the frequency mode is enabled, it will override the alarm mode at the $\overline{IRQ}/F_{OUT}$ pin.

TABLE 5. FREQUENCY SELECTION OF $\overline{IRQ}/F_{OUT}$ PIN

FREQUENCYF_{OUT}	UNITS	FO3	FO2	FO1	FO0
0	Hz	0	0	0	0
32768	Hz	0	0	0	1
4096	Hz	0	0	1	0
1024	Hz	0	0	1	1
64	Hz	0	1	0	0
32	Hz	0	1	0	1
16	Hz	0	1	1	0
8	Hz	0	1	1	1
4	Hz	1	0	0	0
2	Hz	1	0	0	1
1	Hz	1	0	1	0
1/2	Hz	1	0	1	1
1/4	Hz	1	1	0	0
1/8	Hz	1	1	0	1
1/16	Hz	1	1	1	0
1/32	Hz	1	1	1	1

Power Supply Control Register (PWR_VDD)

CLEAR TIME STAMP BIT (CLRTS)

This bit clears Time Stamp V_{DD} to Battery (TSV2B) and Time Stamp Battery to V_{DD} Registers (TSB2V). The default setting is 0 (CLRTS = 0) and the Enabled setting is 1 (CLRTS = 1).

TABLE 6. CLRTS REGISTER

ADDR	7	6	5	4	3	2	1	0
09h	CLRTS	0	0	0	0	V_{DD}Trip2	V_{DD}Trip1	V_{DD}Trip0

V_{DD} BROWNOUT TRIP VOLTAGE BITS (V_{DD}TRIP<2:0>)

These bits set the trip level for the V_{DD} alarm, indicating that V_{DD} has dropped below a preset level. In this event, the LVDD bit in the Status Register is set to "1". See Table 7.

TABLE 7. V_{DD} TRIP LEVELS

V_{DD}Trip2	V_{DD}Trip1	V_{DD}Trip0	TRIP VOLTAGE (V)
0	0	0	2.295
0	0	1	2.550
0	1	0	2.805
0	1	1	3.060
1	0	0	4.250
1	0	1	4.675

Battery Voltage Trip Voltage Register (PWR_VBAT)

This register controls the trip points for the two V_{BAT} alarms, with levels set to approximately 85% and 75% of the nominal battery level.

TABLE 8. BATTERY VOLTAGE TRIP VOLTAGE REGISTER

ADDR	7	6	5	4	3	2	1	0
0Ah	D	RESEALB	VB85 Tp2	VB85 Tp1	VB85 Tp0	VB75 Tp2	VB75T p1	VB75 Tp0

RESEAL BIT (RESEALB)

This is the Reseal bit for actively disconnecting the V_{BAT} pin from the internal circuitry. Setting this bit allows the device to disconnect the battery and eliminate standby current drain while the device is unused. Once V_{DD} is powered up, this bit is reset and the V_{BAT} pin is then connected to the internal circuitry.

The application for this bit involves placing the chip on a board with a battery and testing the board. Once the board is tested and ready to ship, it is desirable to disconnect the battery to keep it fresh until the board or unit is placed into final use. Setting RESEALB = “1” initiates the battery disconnect, and after V_{DD} power is cycled down and up again, the RESEAL bit is cleared to “0”.

BATTERY LEVEL MONITOR TRIP BITS (VB85TP <2:0>)

Three bits select the first alarm (85% of Nominal V_{BAT}) level for the battery voltage monitor. There are a total of 7 levels that could be selected for the first alarm. Any of the of levels could be selected as the first alarm with no reference as to nominal Battery voltage level. See Table 9.

TABLE 9. VB85T ALARM LEVEL

VB85Tp2	VB85Tp1	VB85Tp0	BATTERY ALARM TRIP LEVEL (V)
0	0	0	2.125
0	0	1	2.295
0	1	0	2.550
0	1	1	2.805
1	0	0	3.060
1	0	1	4.250
1	1	0	4.675

BATTERY LEVEL MONITOR TRIP BITS (VB75TP <2:0>)

Three bits select the second alarm (75% of Nominal V_{BAT}) level for the battery voltage monitor. There are a total of 7 levels that could be selected for the second alarm. Any of the of levels could be selected as the second alarm with no reference as to nominal Battery voltage level. See Table 10.

TABLE 10. BATTERY LEVEL MONITOR TRIP BITS (VB75TP <2:0>)

VB75Tp2	VB75Tp1	VB75Tp0	BATTERY ALARM TRIP LEVEL (V)
0	0	0	1.875
0	0	1	2.025
0	1	0	2.250
0	1	1	2.475
1	0	0	2.700
1	0	1	3.750
1	1	0	4.125

Initial AT and DT Setting Register (ITR0)

These bits are used to trim the initial error (at room temperature) of the crystal. Both Digital Trimming (DT) and Analog Trimming (AT) methods are available. The digital trimming uses clock pulse skipping and insertion for frequency adjustment. Analog trimming uses load capacitance adjustment to pull the oscillator frequency. A range of +62.5ppm to -61.5ppm is possible with combined digital and analog trimming.

Initial values for the ITR0 register are preset internally and recalled to RAM registers on power-up. **These values are pre-set in device production and are READ-ONLY. They cannot be overwritten by the user. If an application requires adjustment of the IATR bits outside the preset values, the user should contact Intersil.**

AGING AND INITIAL TRIM DIGITAL TRIMMING BITS (IDTR0<1:0>)

These bits allow ±30.5ppm initial trimming range for the crystal frequency. This is meant to be a coarse adjustment if the range needed is outside that of the IATR control. See Table 11. The IDTR0 register should only be changed while the TSE (Temp Sense Enable) bit is “0”.

The ISL12022MR5421 has a preset Initial Digital Trimming value corresponding to the crystal in the module. **This value is recalled on initial power-up and is READ-ONLY. It cannot be overwritten by the user.**

TABLE 11. IDTR0 TRIMMING RANGE

IDTR01	IDTR00	TRIMMING RANGE
0	0	Default/Disabled
0	1	+30.5ppm
1	0	0ppm
1	1	-30.5ppm

AGING AND INITIAL ANALOG TRIMMING BITS (IATR0<5:0>)

The Initial Analog Trimming Register allows +32ppm to -31ppm adjustment in 1ppm/bit increments. This enables fine frequency adjustment for trimming initial crystal accuracy error or to correct for aging drift.

The ISL12022MR5421 has a preset Initial Analog Trimming value corresponding to the crystal in the module. **This value is recalled on initial power-up, is preset in device production and is READ-ONLY. It cannot be overwritten by the user.**

TABLE 12. INITIAL AT AND DT SETTING REGISTER

ADDR	7	6	5	4	3	2	1	0
0Bh	IDTR01	IDTR00	IATR05	IATR04	IATR03	IATR02	IATR01	IATR00

TABLE 13. IATRO TRIMMING RANGE

IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	TRIMMING RANGE
0	0	0	0	0	0	+32
0	0	0	0	0	1	+31
0	0	0	0	1	0	+30
0	0	0	0	1	1	+29
0	0	0	1	0	0	+28
0	0	0	1	0	1	+27
0	0	0	1	1	0	+26
0	0	0	1	1	1	+25
0	0	1	0	0	0	+24
0	0	1	0	0	1	+23
0	0	1	0	1	0	+22
0	0	1	0	1	1	+21
0	0	1	1	0	0	+20
0	0	1	1	0	1	+19
0	0	1	1	1	0	+18
0	0	1	1	1	1	+17
0	1	0	0	0	0	+16
0	1	0	0	0	1	+15
0	1	0	0	1	0	+14
0	1	0	0	1	1	+13
0	1	0	1	0	0	+12
0	1	0	1	0	1	+11
0	1	0	1	1	0	+10
0	1	0	1	1	1	+9
0	1	1	0	0	0	+8
0	1	1	0	0	1	+7
0	1	1	0	1	0	+6
0	1	1	0	1	1	+5
0	1	1	1	0	0	+4
0	1	1	1	0	1	+3
0	1	1	1	1	0	+2
0	1	1	1	1	1	+1
1	0	0	0	0	0	0
1	0	0	0	0	1	-1
1	0	0	0	1	0	-2
1	0	0	0	1	1	-3
1	0	0	1	0	0	-4
1	0	0	1	0	1	-5
1	0	0	1	1	0	-6
1	0	0	1	1	1	-7
1	0	1	0	0	0	-8
1	0	1	0	0	1	-9
1	0	1	0	1	0	-10

TABLE 13. IATRO TRIMMING RANGE (Continued)

IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	TRIMMING RANGE
1	0	1	0	1	1	-11
1	0	1	1	0	0	-12
1	0	1	1	0	1	-13
1	0	1	1	1	0	-14
1	0	1	1	1	1	-15
1	1	0	0	0	0	-16
1	1	0	0	0	1	-17
1	1	0	0	1	0	-18
1	1	0	0	1	1	-19
1	1	0	1	0	0	-20
1	1	0	1	0	1	-21
1	1	0	1	1	0	-22
1	1	0	1	1	1	-23
1	1	1	0	0	0	-24
1	1	1	0	0	1	-25
1	1	1	0	1	0	-26
1	1	1	0	1	1	-27
1	1	1	1	0	0	-28
1	1	1	1	0	1	-29
1	1	1	1	1	0	-30
1	1	1	1	1	1	-31

ALPHA Register (ALPHA)

TABLE 14. ALPHA REGISTER

ADDR	7	6	5	4	3	2	1	0
0Ch	D	ALPHA6	ALPHA5	ALPHA4	ALPHA3	ALPHA2	ALPHA1	ALPHA0

The ALPHA variable is 8 bits and is defined as the temperature coefficient of crystal from -40°C to T0, or the ALPHA Cold (there is an Alpha Hot register that must be programmed as well). It is normally given in units of ppm/°C^2, with a typical value of -0.034. The ISL12022MR5421 device uses a scaled version of the absolute value of this coefficient in order to get an integer value. Therefore, ALPHA <7:0> is defined as the (|Actual ALPHA Value| x 2048) and converted to binary. For example, a crystal with Alpha of -0.034ppm/°C^2 is first scaled (|2048*(-0.034)| = 70d) and then converted to a binary number of 01000110b.

The practical range of Actual ALPHA values is from -0.020 to -0.060.

The ISL12022MR5421 has a preset ALPHA value corresponding to the crystal in the module. **This value is recalled on initial power-up and is preset in device production. It is READ ONLY and cannot be overwritten by the user.**

BETA Register (BETA)

TABLE 15. BETA REGISTER

ADDR	7	6	5	4	3	2	1	0
0Dh	TSE	BTSE	BTSR	BETA4	BETA3	BETA2	BETA1	BETA0

The BETA register has special Write properties. Only the TSE, BTSE and BTSR bits can be written; the BETA bits are READ-ONLY.

A write to both bytes in this register will only change the 3 MSB's (TSE, BTSE, BTSR), and the 5 LSB's will remain the same as set at the factory.

TEMPERATURE SENSOR ENABLED BIT (TSE)

This bit enables the Temperature Sensing operation, including the temperature sensor, A/D converter and FATR/FDTR register adjustment. The default mode after power-up is disabled: (TSE = 0). To enable the operation, TSE should be set to 1. (TSE = 1). When temp sense is disabled, the initial values for IATR and IDTR registers are used for frequency control.

When TSE is set to 1, the temperature conversion cycle begins and will end when two temperature conversions are completed. The average of the two conversions is in the TEMP registers.

TEMP SENSOR CONVERSION IN BATTERY MODE BIT (BTSE)

This bit enables the Temperature Sensing and Correction in battery mode. BTSE = 0 (default) no conversion, Temp Sensing or Compensation in battery mode. BTSE = 1 indicates Temp Sensing and Compensation enabled in battery mode. The BTSE is disabled when the battery voltage is lower than 2.7V. No temperature compensation will take place with V_{BAT} < 2.7V.

FREQUENCY OF TEMPERATURE SENSING AND CORRECTION BIT (BTSR)

This bit controls the frequency of Temp Sensing and Correction. BTSR = 0 default mode is every 10 minutes, BTSR = 1 is every 1.0 minute. Note that BTSE has to be enabled in both cases. See Table 16.

TABLE 16. FREQUENCY OF TEMPERATURE SENSING AND CORRECTION BIT

BTSE	BTSR	TC PERIOD IN BATTERY MODE
0	0	OFF
0	1	OFF
1	0	10 Minutes
1	1	1 Minute

The temperature measurement conversion time is the same for battery mode as for V_{DD} mode, approximately 22ms. The battery mode current will increase during this conversion time to typically 68µA. The average increase in battery current is much lower than this due to the small duty cycle of the ON-time versus OFF-time for the conversion.

To figure the average increase in battery current, we take the change in current times the duty cycle. For the 1 minute temperature period, the average current is expressed in Equation 1:

$$\Delta I_{BAT} = \frac{0.022s}{60s} \times 68\mu A = 250nA \quad \text{(EQ. 1)}$$

For the 10 minute temperature period the average current is expressed in Equation 2:

$$\Delta I_{BAT} = \frac{0.022s}{600s} \times 68\mu A = 25nA \quad \text{(EQ. 2)}$$

If the application has a stable temperature environment that doesn't change quickly, the 10 minute option will work well and the backup battery lifetime impact is minimized. If quick temperature variations are expected (multiple cycles of more than 10° within an hour), then the 1 minute option should be considered and the slightly higher battery current figured into overall battery life.

GAIN FACTOR OF AT BIT (BETA<4:0>)

Beta is specified to take care of the Cm variations of the crystal. Most crystals specify Cm around 2.2fF. For example, if Cm > 2.2fF, the actual AT steps may reduce from 1ppm/step to approximately 0.80ppm/step. Beta is then used to adjust for this variation and restore the step size to 1ppm/step.

BETA values are limited in the range from 01000 to 11111, as shown in Table 17. To use Table 17, the device is tested at two AT settings as follows:

BETA VALUES = (AT(max) - AT (min))/63, where:

AT(max) = F_{OUT} in ppm (at AT = 00H) and

AT(min) = F_{OUT} in ppm (at AT = 3FH).

The BETA VALUES result is indexed in the right hand column and the resulting Beta factor (for the register) is in the same row in the left column.

The ISL12022MR5421 has a preset BETA value corresponding to the crystal in the module. **This value is recalled on initial power-up and is preset in device production. It is READ ONLY and cannot be overwritten by the user.**

TABLE 17. BETA VALUES

BETA<4:0>	AT STEP ADJUSTMENT
01000	0.5000
00111	0.5625
00110	0.6250
00101	0.6875
00100	0.7500
00011	0.8125
00010	0.8750
00001	0.9375
00000	1.0000
10000	1.0625
10001	1.1250
10010	1.1875
10011	1.2500
10100	1.3125
10101	1.3750
10110	1.4375
10111	1.5000
11000	1.5625
11001	1.6250

TABLE 17. BETA VALUES (Continued)

BETA<4:0>	AT STEP ADJUSTMENT
11010	1.6875
11011	1.7500
11100	1.8125
11101	1.8750
11110	1.9375
11111	2.0000

Final Analog Trimming Register (FATR)

This register shows the final setting of AT after temperature correction. It is read-only; the user cannot overwrite a value to this register. This value is accessible as a means of monitoring the temperature compensation function. See Table 18 and Table 19 (for values).

TABLE 18. FINAL ANALOG TRIMMING REGISTER

ADDR	7	6	5	4	3	2	1	0
0Eh	0	0	FATR5	FATR4	FATR3	FATR2	FATR1	FATR0

TABLE 19. FINAL DIGITAL TRIMMING REGISTER

ADDR	7	6	5	4	3	2	1	0
0Fh	0	0	0	FDTR4	FDTR3	FDTR2	FDTR1	FDTR0

Final Digital Trimming Register (FDTR)

This Register shows the final setting of DT after temperature correction. It is read-only; the user cannot overwrite a value to this register. The value is accessible as a means of monitoring the temperature compensation function. The corresponding clock adjustment values are shown in Table 20. The FDTR setting has both positive and negative settings to adjust for any offset in the crystal.

TABLE 20. CLOCK ADJUSTMENT VALUES FOR FINAL DIGITAL TRIMMING REGISTER

FDTR<4:0>	DECIMAL	ppm ADJUSTMENT
00000	0	0
00001	1	30.5
00010	2	61
00011	3	91.5
00100	4	122
00101	5	152.5
00110	6	183
00111	7	213.5
01000	8	244
01001	9	274.5
01010	10	305
10000	0	0
10001	-1	-30.5

TABLE 20. CLOCK ADJUSTMENT VALUES FOR FINAL DIGITAL TRIMMING REGISTER (Continued)

FDTR<4:0>	DECIMAL	ppm ADJUSTMENT
10010	-2	-61
10011	-3	-91.5
10100	-4	-122
10101	-5	-152.5
10110	-6	-183
10111	-7	-213.5
11000	-8	-244
11001	-9	-274.5
11010	-10	-305

ALARM Registers (10h to 15h)

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. Note that there is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

- **Single Event Mode** is enabled by setting Bit 7 on any of the Alarm registers (ESCA0... EDWA0) to “1”, the IM bit to “0”, and disabling the frequency output. This mode permits a one-time match between the Alarm registers and the RTC registers. Once this match occurs, the ALM bit is set to “1” and the $\overline{IRQ}/F_{OUT}$ output will be pulled low and will remain low until the ALM bit is reset. This can be done manually or by using the auto-reset feature.
- **Interrupt Mode** is enabled by setting Bit 7 on any of the Alarm registers (ESCA0... EDWA0) to “1”, the IM bit to “1”, and disabling the frequency output. The $\overline{IRQ}/F_{OUT}$ output will now be pulsed each time an alarm occurs. This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading.

To clear a single event alarm, the ALM bit in the status register must be set to “0” with a write. Note that if the ARST bit is set to 1 (address 08h, bit 7), the ALM bit will automatically be cleared when the status register is read.

Following are examples of both Single Event and periodic Interrupt Mode alarms.

Example 1

- Alarm set with single interrupt (IM = “0”)
- A single alarm will occur on January 1 at 11:30 a.m.
- Set Alarm registers as follows:

TABLE 21. SINGLE-EVENT ALARM

ALARM REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
SCA0	0	0	0	0	0	0	0	0	00h	Seconds disabled
MNA0	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
HRA0	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
DTA0	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
MOA0	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30 a.m. on January 1 (after seconds changes from 59 to 00) by setting the ALM bit in the status register to “1” and also bringing the $\overline{IRQ}/F_{OUT}$ output low.

Example 2

- Pulsed interrupt once per minute (IM = “1”)
- Interrupts at one minute intervals when the seconds register is at 30 seconds.
- Set Alarm registers as follows:

TABLE 22. PERIODIC INTERRUPT MODE ALARM

ALARM REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
SCA0	1	0	1	1	0	0	0	0	B0h	Seconds set to 30, enabled
MNA0	0	0	0	0	0	0	0	0	00h	Minutes disabled
HRA0	0	0	0	0	0	0	0	0	00h	Hours disabled
DTA0	0	0	0	0	0	0	0	0	00h	Date disabled
MOA0	0	0	0	0	0	0	0	0	00h	Month disabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

Once the registers are set, the following waveform will be seen at $\overline{IRQ}/F_{OUT}$:

FIGURE 16. $\overline{IRQ}/F_{OUT}$ WAVEFORM

Note that the status register ALM bit will be set each time the alarm is triggered, but does not need to be read or cleared.

Time Stamp V_{DD} to Battery Registers (TSV2B)

The TSV2B Register bytes are identical to the RTC register bytes, except they do not extend beyond the Month. The Time Stamp captures the FIRST V_{DD} to Battery Voltage transition time, and will not update upon subsequent events until cleared (only the first event is captured before clearing). Set CLRTS = 1 to clear this register (Add 09h, PWR_V_{DD} register).

Note that the time stamp registers are cleared to all “0”, including the month and day, which is different from the RTC and alarm registers (those registers default to 01h). This is the indicator that no time stamping has occurred since the last clear or initial power-up. Once a time stamp occurs, there will be a non-zero time stamp.

Time Stamp Battery to V_{DD} Registers (TSB2V)

The Time Stamp Battery to V_{DD} Register bytes are identical to the RTC register bytes, except they do not extend beyond Month. The Time Stamp captures the LAST transition of V_{BAT} to V_{DD} (only the last event of a series of power-up/power-down events is retained). Set CLRTS = 1 to clear this register (Add 09h, PWR_V_{DD} register).

TABLE 23. DST FORWARD REGISTERS

ADDRESS	FUNCTION	7	6	5	4	3	2	1	0
20h	**Month Forward**	DSTE	0	0	MoFd20	MoFd13	MoFd12	MoFd11	MoFd10
21h	Day Forward	0	DwFdE	WkFd12	WkFd11	WkFd10	DwFd12	DwFd11	DwFd10
22h	Date Forward	0	0	DtFd21	DtFd20	DtFd13	DtFd12	DtFd11	DtFd10
23h	**Hour Forward**	0	0	HrFd21	HrFd20	HrFd13	HrFd12	HrFd11	HrFd10

TABLE 24. DST REVERSE REGISTERS

ADDRESS	NAME	7	6	5	4	3	2	1	0
24h	**Month Reverse**	0	0	0	MoRv20	MoRv13	MoRv12	MoRv11	MoRv10
25h	Day Reverse	0	DwRvE	WkRv12	WkRv11	WkRv10	DwRv12	DwRv11	DwRv10
26h	Date Reverse	0	0	DtRv21	DtRv20	DtRv13	DtRv12	DtRv11	DtRv10
27h	Hour Reverse	0	0	HrRv21	HrRv20	HrRv13	HrRv12	HrRv11	HrRv10

DST Control Registers (DSTCR)

8 bytes of control registers have been assigned for the Daylight Savings Time (DST) functions. DST beginning (set Forward) time is controlled by the registers DstMoFd, DstDwFd, DstDtFd, and DstHrFd. DST ending time (set Backward or Reverse) is controlled by DstMoRv, DstDwRv, DstDtRv and DstHrRv.

Tables 23 and 24 describe the structure and functions of the DSTCR.

DST FORWARD REGISTERS (20H TO 23H)

DST forward is controlled by the following DST Registers:

DST Enable

DSTE is the DST Enabling Bit located in Bit 7 of register 20h (DstMoFdxx). Set DSTE = 1 will enable the DSTE function. Upon powering up for the first time (including battery), the DSTE bit defaults to “0”. When DSTE is set to “1” the RTC time must be at least one hour before the scheduled DST time change for the correction to take place. When DSTE is set to “0”, the DSTADJ bit in the Status Register automatically resets to “0”.

DST Month Forward

DstMoFd sets the Month that DST starts. The format is the same as for the RTC register month, from 1 to 12. The default value for the DST begin month is 00h.

DST Day/Week Forward

DstDwFd contains both the Day of the Week and the Week of the Month data for DST Forward control. DST can be controlled either by actual date or by setting both the Week of the month and the Day of the Week. DstDwFdE sets the priority of the Day/Week over the Date. For DstDwFdE = 1, Day/Week is the priority. You must have the correct Day of Week entered in the RTC registers for the Day/Week correction to work properly.

- Bits 0, 1, 2 contain the Day of the week information which sets the Day of the Week that DST starts. Note that Day of the week counts from 0 to 6, like the RTC registers. The default for the DST Forward Day of the Week is 00h (normally Sunday).
- Bits 3, 4, 5 contain the Week of the Month information that sets the week that DST starts. The range is from 1 to 5, and Week 7 is used to indicate the last week of the month. The default for the DST Forward Week of the Month is 00h.

DST Date Forward

DstDtfd controls which Date DST begins. The format for the Date is the same as for the RTC register, from 1 to 31. The default value for DST forward date is 00h. DstDtFd is only effective if DstDwFdE = 0.

DST Hour Forward

DstHrFd controls the hour that DST begins. The RTC hour and DstHrFd registers have the same formats except there is no Military bit for DST hour. The user sets the DST hour with the same format as used for the RTC hour (AM/PM or MIL) but without the MIL bit, and the DST will still advance as if the MIL bit were there. The default value for DST hour Forward is 00h.

DST REVERSE REGISTERS (24H TO 27H)

DST end (reverse) is controlled by the following DST Registers:

DST Month Reverse

DstMoRv sets the Month that DST ends. The format is the same as for the RTC register month, from 1 to 12. The default value for the DST end month is October (10h).

DST Day/Week Reverse

DstDwRv contains both the Day of the Week and the Week of the Month data for DST Reverse control. DST can be controlled either by actual date or by setting both the Week of the month and the Day of the Week. DstDwRvE sets the priority of the Day/Week over the Date. For DstDwRvE = 1, Day/Week is the priority. You must have the correct Day of Week entered in the RTC registers for the Day/Week correction to work properly.

- Bits 0, 1, 2 contain the Day of the week information which sets the Day of the Week that DST ends. Note that Day of the week counts from 0 to 6, like the RTC registers. The default for the DST Reverse Day of the Week is 00h (normally Sunday).
- Bits 3, 4, 5 contain the Week of the Month information that sets the week that DST ends. The range is from 1 to 5, and Week 7 is used to indicate the last week of the month. The default for the DST Reverse Week of the Month is 00h.

DST Date Reverse

DstDtRv controls which Date DST ends. The format for the Date is the same as for the RTC register, from 1 to 31. The default value for DST Date Reverse is 00h. The DstDtRv is only effective if the DwRvE = 0.

DST Hour Reverse

DstHrRv controls the hour that DST ends. The RTC hour and DstHrFd registers have the same formats except there is no Military bit for DST hour. The user sets the DST hour with the same format as used for the RTC hour (AM/PM or MIL) but without the MIL bit, and the DST will still advance as if the MIL bit were there. The default value for DST hour Reverse is 00h.

TEMP Registers (TEMP)

The temperature sensor produces an analog voltage output which is input to an A/D converter and produces a 10-bit temperature value in degrees Kelvin. TK07:00 are the LSBs of the code, and TK09:08 are the MSBs of the code. The temperature result is actually the average of two successive temperature measurements to produce greater resolution for the temperature control. The output code can be converted to °C by first converting from binary to decimal, dividing by 2, and then subtracting 273d.

$$\text{Temperature in °C} = [(TK<9:0>)/2] - 273 \quad \text{(EQ. 3)}$$

The practical range for the temp sensor register output is from 446d to 726d, or -50°C to +90°C. The temperature compensation function is only guaranteed over -40°C to +85°C. The TSE bit must be set to "1" to enable temperature sensing.

TABLE 25. TEMP REGISTER

TEMP	7	6	5	4	3	2	1	0
TK0L	TK07	TK06	TK05	TK04	TK03	TK02	TK01	TK00
TK0M	0	0	0	0	0	0	TK09	TK08

NPPM Registers (NPPM)

The NPPM value is exactly 2x the net correction, in ppm, required to bring the oscillator to 0ppm error. The value is the combination of oscillator Initial Correction (IPPM) and crystal temperature dependent correction (CPPM).

IPPM is used to compensate the oscillator offset at room temperature and is controlled by the ITR0 and BETA registers. This value is normally set during room temperature testing.

The CPPM compensates the oscillator frequency fluctuation over-temperature. It is determined by the temperature (T), crystal curvature parameter (ALPHA), and crystal turnover temperature (XT0). T is the result of the temp sensor/ADC conversion, whose decimal result is 2x the actual temperature in Kelvin. ALPHA is from either the ALPHA (cold) or ALPHAH (hot) register depending on T, and XT0 is from the XT0 register.

NPPM is governed by Equations 4 and 5:

NPPM = IPPM(ITR0, BETA) + ALPHA x (T-T0)2

$$NPPM = IPPM + CPPM$$

$$NPPM = IPPM + \frac{ALPHA \bullet (T - T0)^2}{4096} \quad \text{(EQ. 4)}$$

where

$$ALPHA = \alpha \bullet 2048$$

T is the reading of the ADC, result is 2 x temperature in degrees Kelvin.

$$T = (2 \bullet 298) + XT0 \quad \text{(EQ. 5)}$$

or $T = 596 + XT0$

Note that NPPM can also be predicted from the FATR and FDTR register by the relationship (all values in decimal):

NPPM = 2*(BETA*FATR - (FDTR-16)

XT0 Registers (XT0)

TURNOVER TEMPERATURE (XT<3:0>)

The apex of the Alpha curve occurs at a point called the turnover temperature, or XT0. Crystals normally have a turnover temperature between +20°C and +30°C, with most occurring near +25°C.

TABLE 26. TURNOVER TEMPERATURE

ADDR	7	6	5	4	3	2	1	0
2Ch	0	0	0	XT4	XT3	XT2	XT1	XT0

The ISL12022MR5421 has a preset Turnover temperature corresponding to the crystal in the module. **This value is recalled on initial power-up and is preset in device production. It is READ ONLY and cannot be overwritten by the user.**

Table 27 shows the values available, with a range from +17.5°C to +32.5°C in +0.5°C increments. The default value is 00000b or +25°C.

TABLE 27. XT0 VALUES

XT<4:0>	TURNOVER TEMPERATURE
01111	32.5
01110	32.0
01101	31.5
01100	31
01011	30.5
01010	30
01001	29.5
01000	29.0
00111	28.5
00110	28.0
00101	27.5
00100	27.0
00011	26.5
00010	26.0
00001	25.5
00000	25.0

TABLE 27. XT0 VALUES (Continued)

XT<4:0>	TURNOVER TEMPERATURE
10000	25.0
10001	24.5
10010	24.0
10011	23.5
10100	23.0
10101	22.5
10110	22.0
10111	21.5
11000	21.0
11001	20.5
11010	20.0
11011	19.5
11100	19.0
11101	18.5
11110	18.0
11111	17.5

ALPHA Hot Register (ALPHAH)

TABLE 28. ALPHAH REGISTER

ADDR	7	6	5	4	3	2	1	0
2Dh	D	ALP_H6	ALP_H5	ALP_H4	ALP_H3	ALP_H2	ALP_H1	ALP_H0

The ALPHA Hot variable is 7 bits and is defined as the temperature coefficient of Crystal from the XT0 value to +85°C (both Alpha Hot and Alpha Cold must be programmed to provide full temperature compensation). It is normally given in units of ppm/°C^2, with a typical value of -0.034. Like the ALPHA Cold version, a scaled version of the absolute value of this coefficient is used in order to get an integer value. Therefore, ALP_H <7:0> is defined as the (|Actual Alpha Hot Value| x 2048) and converted to binary. For example, a crystal with Alpha Hot of -0.034ppm/°C^2 is first scaled (|2048*(-0.034)| = 70d) and then converted to a binary number of 01000110b.

The practical range of Actual ALPHAH values is from -0.020 to -0.060.

The ISL12022MR5421 has a preset ALPHAH value corresponding to the crystal in the module. **This value is recalled on initial power-up and is preset in device production. It is READ ONLY and cannot be overwritten by the user.**

User Registers (Accessed by Using Slave Address 1010111x)

Addresses [00h to 7Fh]

These registers are 128 bytes of battery-backed user SRAM. The separate I^{2}C slave address must be used to read and write to these registers.

I^{2}C Serial Interface

The ISL12022MR5421 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12022MR5421 operates as a slave device in all applications.

All communication over the I^{2}C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 17). On power-up of the ISL12022MR5421, the SDA pin is in the input mode.

All I^{2}C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12022MR5421 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 17). A START condition is ignored during the power-up sequence.

All I^{2}C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 17). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

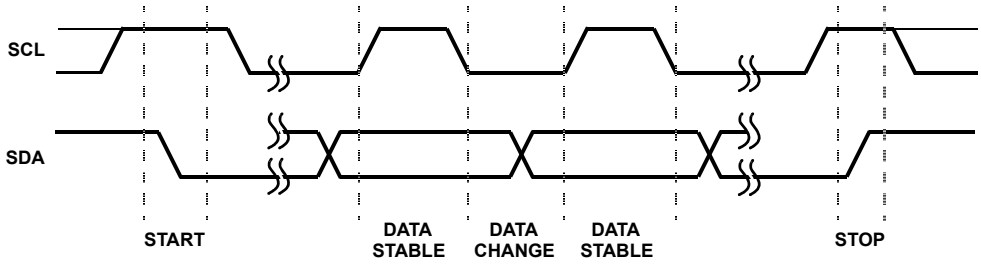


FIGURE 17. VALID DATA CHANGES, START AND STOP CONDITIONS

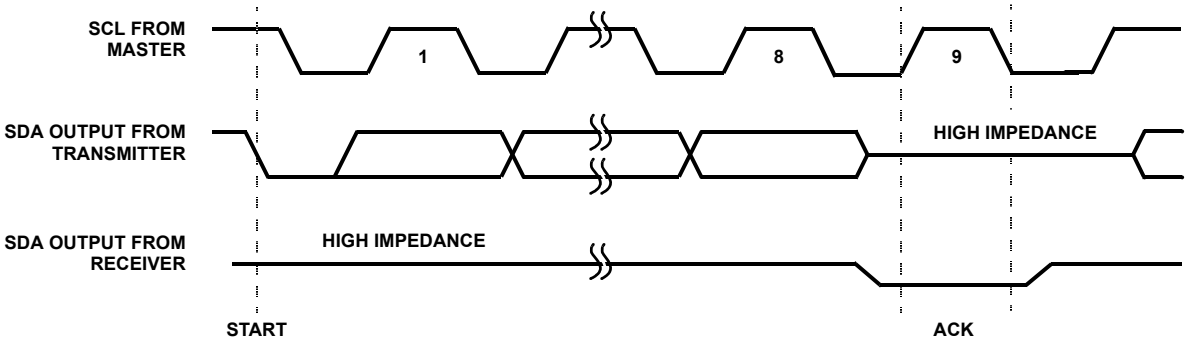


FIGURE 18. ACKNOWLEDGE RESPONSE FROM RECEIVER

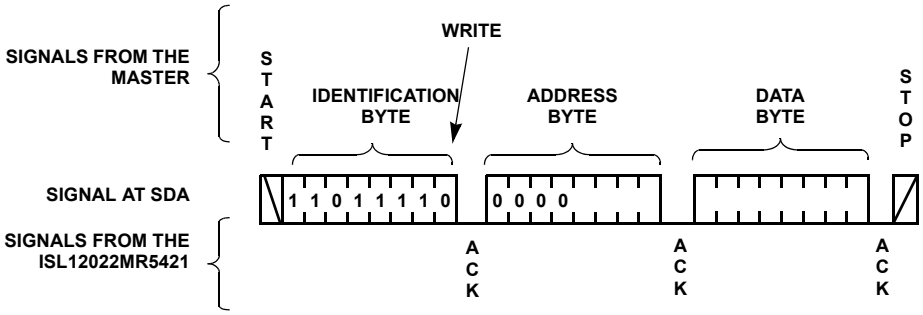


FIGURE 19. BYTE WRITE SEQUENCE (SLAVE ADDRESS FOR CSR SHOWN)

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 18).

The ISL12022MR5421 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again, after successful receipt of an Address Byte. The ISL12022MR5421 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifiers. These bits are "1101111" for the RTC registers and "1010111" for the User SRAM.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a "1", a read operation is selected. A "0" selects a write operation (refer to Figure 20).

After loading the entire Slave Address Byte from the SDA bus, the ISL12022MR5421 compares the device identifier and device select bits with "1101111" or "1010111". Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address 00h, so a current address read starts at address 00h. When required, as part of a random read, the master must supply the 1 Word Address Bytes, as shown in Figure 22.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. For a random read of the Control/Status Registers, the slave byte must be "1101111x" in both places.

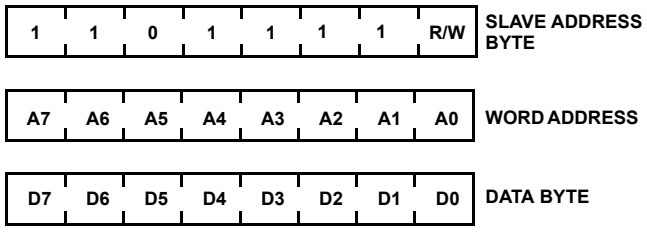


FIGURE 20. SLAVE ADDRESS, WORD ADDRESS AND DATA BYTES

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12022MR5421 responds with an ACK. At this time, the I^2C interface enters a standby state.

Read Operation

A Read operation consists of a three byte instruction, followed by one or more Data Bytes (see Figure 22). The master initiates the operation issuing the following sequence: a START, the

Identification byte with the R/$\overline{W}$ bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to "1". After each of the three bytes, the ISL12022MR5421 responds with an ACK. Then the ISL12022MR5421 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 22).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer's initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 2Fh, the pointer "rolls over" to 00h, and the device continues to output data for each ACK received.

Application Section

Power Supply Considerations

The ISL12022M contains programmed EEPROM registers which are recalled to volatile RAM registers during initial power-up. These registers contain DC voltage, frequency and temperature calibration settings. Initial power-up can be either application of V_{BAT} or V_{DD} power, whichever is first. It is important that the initial power-up meet the power supply slew rate specification to avoid faulty EEPROM power-up recall. Also, any glitches or low voltage DC pauses should be avoided, as these may activate recall at a low voltage and load erroneous data into the calibration registers. Note that a very slow V_{DD} ramp rate (outside data sheet limits) will almost always trigger erroneous recall and should be avoided entirely.

Battery Backup Details

The ISL12022MR5421 has automatic switchover to battery backup when the V_{DD} drops below the V_{BAT} mode threshold. A wide variety of backup sources can be used, including standard and rechargeable lithium, super-capacitors, or regulated secondary sources. The serial interface is disabled in battery backup, while the oscillator and RTC registers are operational. The SRAM register contents are powered to preserve their contents as well.

The input voltage range for V_{BAT} is 1.8V to 5.5V, but keep in mind the temperature compensation only operates for V_{BAT} > 2.7V. Note that the device is not guaranteed to operate with a V_{BAT} < 1.8V, so the battery should be changed before discharging to that level. It is strongly advised to monitor the low battery indicators in the status registers and take action to replace discharged batteries.

If a supercapacitor is used, it is possible that it may discharge to below 1.8V during prolonged power-down. Once powered up, the device may lose serial bus communications until both V_{DD} and V_{BAT} are powered down together. To avoid that situation, including situations where a battery may discharge deeply, the circuit in Figure 21 can be used.

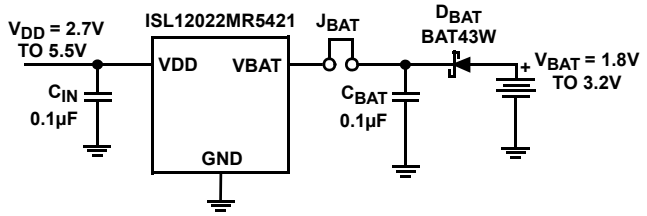


FIGURE 21. SUGGESTED BATTERY BACKUP CIRCUIT

The diode, D_{BAT} will add a small drop to the battery voltage but will protect the circuit should battery voltage drop below 1.8V. The jumper is added as a safeguard should the battery ever need to be disconnected from the circuit.

The V_{DD} negative slew rate should be limited to below the data sheet spec (10V/ms) otherwise battery switchover can be delayed, resulting in SRAM contents corruption and oscillator operation interruption.

Some applications will require separate supplies for the RTC V_{DD} and the I^2C pull-ups. This is not advised, as it may compromise the operation of the I^2C bus. For applications that do require serial bus communication with the RTC V_{DD} powered down, the SDA pin must be pulled low during the time the RTC V_{DD} ramps down to 0V. Otherwise, the device may lose serial bus communications once V_{DD} is powered up, and will return to normal operation ONLY once V_{DD} and V_{BAT} are both powered down together.

Layout Considerations

The ISL12022MR5421 contains a quarts crystal and requires special handling during PC board assembly. Excessive shock and vibrations should be avoided, especially with automated handling equipment. Ultrasound cleaning is not advisable as it subjects the crystal to resonance and possible failure. See also Note 5 on page 6 in the specifications tables, which pertains to solder reflow effects on oscillator accuracy.

The part of the package from pin 1 to 5 and from pin 16 to 20 contains the crystal. Low frequency RTC crystals are known to pick up noise very easily if layout precautions are not followed, even embedded within a plastic package. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 23 shows a suggested layout for the ISL12022MR5421 device. The following main precautions should be followed:

- Do not run the serial bus lines or any high speed logic lines in the vicinity of pins 1 and 20, or under the package. These logic level lines can induce noise in the oscillator circuit, causing misclocking.
- Add a ground trace around the device with one end terminated at the chip ground. This guard ring will provide termination for emitted noise in the vicinity of the RTC device
- Be sure to ground pins 6 and 15 as well as pin 8 as these all insure the integrity of the device ground
- Add a 0.1µF decoupling capacitor at the device V_{DD} pin, especially when using the 32.768kHz F_{OUT} function.

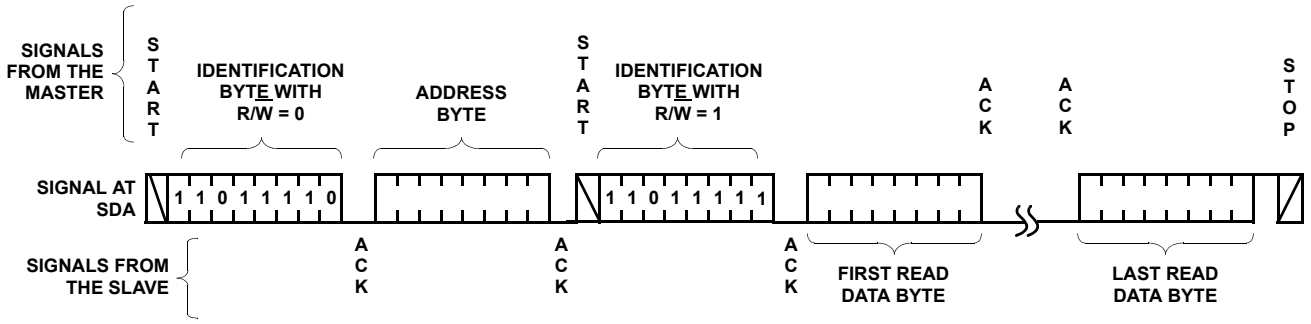


FIGURE 22. READ SEQUENCE (CSR SLAVE ADDRESS SHOWN)

The best way to run clock lines around the RTC is to stay outside of the ground ring by at least a few millimeters. Also, use the V_{BAT} and V_{DD} as guard ring lines as well, they can isolate clock lines from the oscillator section. In addition, if the $\overline{IRQ}/F_{OUT}$ pin is used as a clock, it should be routed away from the RTC device as well.

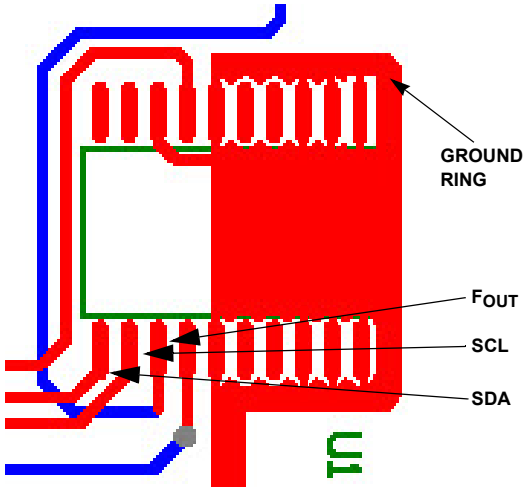


FIGURE 23. SUGGESTED LAYOUT FOR THE ISL12022MR5421

Measuring Oscillator Accuracy

The best way to analyze the ISL12022MR5421 frequency accuracy is to set the $\overline{IRQ}/F_{OUT}$ pin for a specific frequency, and look at the output of that pin on a high accuracy frequency counter (at least 7 digits accuracy). Note that the $\overline{IRQ}/F_{OUT}$ is an drain output and will require a pull-up resistor.

Using the 1.0Hz output frequency is the most convenient as the ppm error is expressed in Equation 6:

$$\text{ppm error} = F_{OUT} - 1 \bullet 1e6 \quad \text{(EQ. 6)}$$

Other frequencies may be used for measurement but the error calculation becomes more complex. Use the F_{OUT} output and a frequency counter for the most accurate results. Also, when the proper layout guidelines above are observed, the oscillator should start-up in most circuits in less than one second.

Temperature Compensation Operation

The ISL12022MR5421 temperature compensation feature needs to be enabled by the user. This must be done in a specific order as follows.

1. Read register 0Dh, the BETA register. This register contains the 5-bit BETA trimmed value, which is automatically loaded on initial power-up. Mask off the 5 LSB's of the value just read.
2. Bit 7 of the BETA register is the master enable control for temperature sense operation. Set this to "1" to allow continuous temperature frequency correction. Frequency correction will then happen every 60 seconds with V_{DD} applied.
3. Bits 5 and 6 of the BETA register control temperature compensation in battery backup mode (see Table 16). Set the values for the operation desired.
4. Write back to register 0Dh making sure not to change the 5 LSB values, and include the desired compensation control bits.

Note that every time the BETA register is written with the TSE bit = 1, a temperature compensation cycle is instigated and a new correction value will be loaded into the FATR/FDTR registers (if the temperature changed since the last conversion).

Also note that registers 0Bh and 0Ch, the ITR0 and ALPHA registers, are READ-ONLY, and cannot be written to. Also the value for BETA is locked and cannot be changed with a write. However, It is still a good idea to do the bit masking when doing TSE bit changes.

Daylight Savings Time (DST) Example

DST involves setting the forward and back times and allowing the RTC device to automatically advance the time or set the time back. This can be done for current year, and future years. Many regions have DST rules that use standard months, weeks and time of the day, which permit a pre-programmed, permanent setting.

Table 29 shows an example setup for the ISL12022MR5421.

TABLE 29. DST EXAMPLE

VARIABLE	VALUE	REGISTER	VALUE
Month Forward and DST Enable	April	15h	84h
Week and Day Forward and select Day/Week, not Date	1st Week and Sunday	16h	48h
Date Forward	not used	17h	00h
Hour Forward	2am	18h	02h
Month Reverse	October	19h	10h

TABLE 29. DST EXAMPLE

VARIABLE	VALUE	REGISTER	VALUE
Week and Day Reverse and select Day/Week, not Date	Last Week and Sunday	1Ah	78h
Date Reverse	not used	1Bh	00h
Hour Reverse	2am	1Ch	02h

The Enable bit (DSTE) is in the Month forward register, so the BCD value for that register is altered with the additional bit. The Week and Day values along with Week/Day vs Date select bit is in the Week/Day register, so that value is also not straight BCD. Hour and Month are normal BCD, but the Hour doesn't use the MIL bit since Military time PM values are already discretely different from AM/PM time PM values. The DST reverse setting utilizes the option to select the last week of the month for October, which could have 4 or 5 weeks but needs to have the time change on the last Sunday.

Note that the DSTADJ bit in the status register monitors whether the DST forward adjustment has happened. When it is "1", DST forward has taken place. When it is "0", then either DST reverse has happened, or it has been reset either by initial power-up or if the DSTE bit has been set to "0".

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
May 14, 2012	FN7576.3	• Added “OSCILLATOR ACCURACY” heading to specification table on page 7. Updated Oscillator accuracy specifications. • Removed Min/Max of -5/5ppm for “Oscillator Stability vs Temperature” on page 7. Added typ of ±2ppm. • Added notes 16, 17, 18 to specification table. • Corrected text errors.
October 14, 2011	FN7576.2	• On page 6, Absolute Maximum Ratings: added Shock Resistance and Vibration values. • On page 6, DC Operating Characteristics: for I_{DD1} at 5V and 3V limits, changed MAX from 7µA and 6µA to 15µA and 14µA. • On page 7, Power-Down Timing: added V_{DDSR+} with TYP value of 0.05V/ms, with reference to Note 15. • On page 8, added Note 15 for V_{DDSR+} • On page 13, Oscillator Compensation: text deleted: "These values can be overwritten by the user although this is not suggested as the resulting temperature compensation performance will be compromised." • On page 16, Oscillator Fail Bit: changed text from "Oscillator Fail Bit indicates that the oscillator has stopped." to: "Oscillator Fail Bit indicates that the oscillator has failed. The oscillator frequency is either zero or very far from the desired 32.768kHz due to failure, PC board contamination or mechanical issues." • On page 16, Daylight Saving Time Change Bit (DSTADJ): removed "DSTADJ can be set to "1" for instances where the RTC device is initialized during the DST Forward period." and added "It is read-only and cannot be written. Setting time during a DST forward period will not set this bit to "1"." • On page 21, Table 20, FDTR column heading changed from <2:0> to <4:0> • On page 27, added “Power Supply Considerations” section. • On Page 32, Package Outline Drawing: replaced M20.3, Rev 2, 6/15, with M20.3, Rev 3, 2/11.
May 27, 2010	FN7576.1	Changed CDM in “ESD Rating” on page 6 from >1500V to >2200V
March 22, 2010	FN7576.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

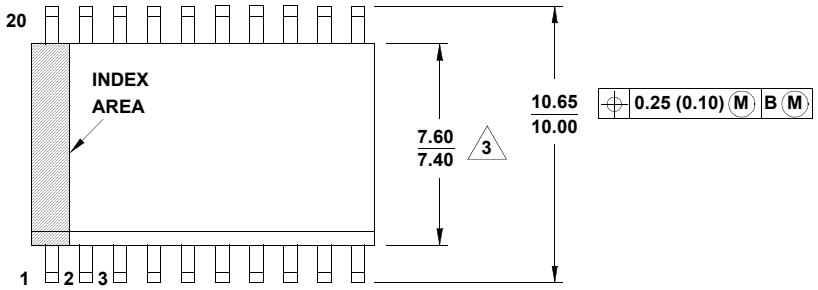
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

Package Outline Drawing

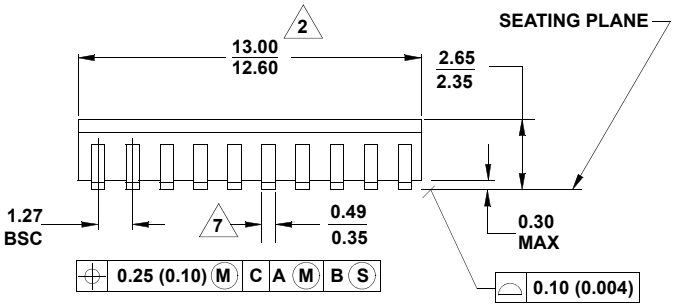
M20.3

20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)

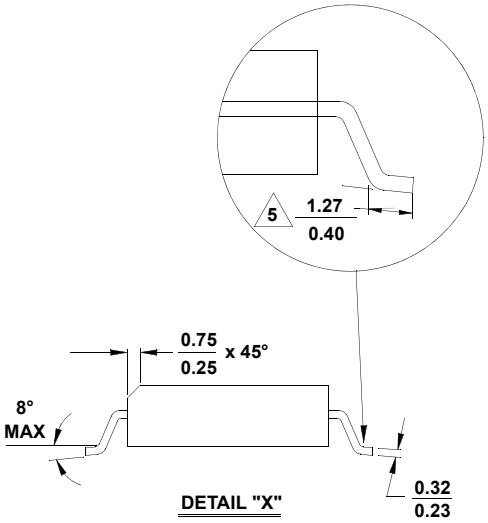
Rev 3, 2/11



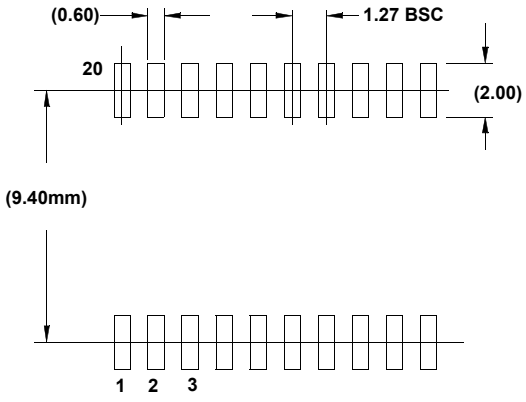
TOP VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Dimension does not include interlead lash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Dimension is the length of terminal for soldering to a substrate.
6. Terminal numbers are shown for reference only.
7. The lead width as measured 0.36mm (0.14 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
8. Controlling dimension: MILLIMETER.
9. Dimensions in ( ) for reference only.
10. JEDEC reference drawing number: MS-013-AC.