Click ***here*** *for production status of specific part numbers.*

MAX77278

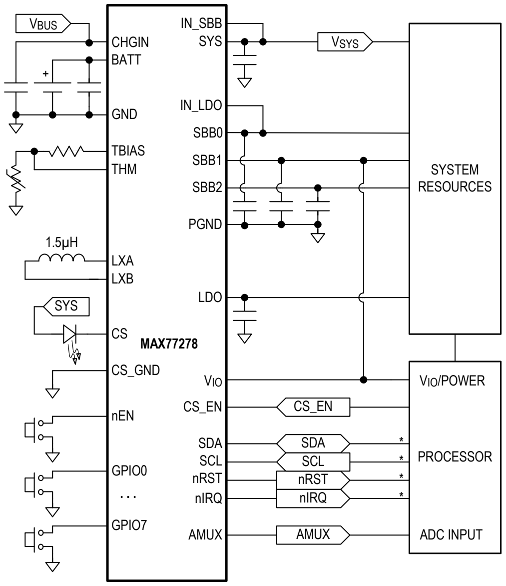
Ultra-Low Power PMIC with 3-Output SIMO, Power Path Charger Optimized for Small Li+, 425mA Current Sink, and 8 GPIO

General Description

The MAX77278 provides highly-integrated battery charging and power supply solutions for low-power applications where size and efficiency are critical. The device features a single-inductor multiple-output (SIMO) buck-boost regulator that provides three independently programmable power rails from a single inductor to minimize total solution size. A 50mA LDO provides ripple rejection for audio and other noise-sensitive applications. A highly-configurable linear charger supports a wide range of Li+ battery capacities and includes battery temperature monitoring for additional safety (JEITA).

The device includes other features such as a programmable current sink that can be used to drive an IR-LED, 8 general-purpose input/output (GPIO) control pins, and an analog multiplex (AMUX) output that provides access to useful battery charging signals. A bidirectional I^{2}C interface allows for configuring and checking the status of the device. An internal on/off controller provides a controlled startup sequence for the regulators and provides supervisory functionality when the device is on. Numerous factory programmable options allow the device to be tailored for many applications, enabling faster time to market.

Simplified Application Circuit



*THE PROCESSOR HAS INTERNAL PULLUP RESISTORS FOR THIS NODE.

Benefits and Features

- Highly Integrated
  - Smart Power Selector™ Li+/Li-Poly Charger
  - Three Output, SIMO Buck-Boost Regulator
  - 50mA LDO
  - Programmable 250mA to 425mA Current Sink Driver
  - Analog MUX Output for Power Monitoring
  - Eight GPIOs (Configured for One-Button Wake-Up and Two-Button Shutdown)
- Low Power
  - 0.3µA Standby Current
  - 16µA Operating Current
- Charger Optimized for Small Battery Size
  - Programmable Fast-Charge Current from 7.5mA to 300mA
  - Programmable Battery Regulation Voltage from 3.6V to 4.6V
  - Programmable Termination Current from 0.375mA to 45mA
  - JEITA Battery Temperature Monitors Adjust Charge Current and Battery Regulation Voltage for Safe Charging
- Flexible and Configurable
  - I^{2}C-Compatible Interface
  - Eight GPIOs
  - Factory OTP Options Available
- Small Size
  - 3.15mm x 2.15mm x 0.7mm
  - 35-Bump, 0.4mm-Pitch, 7x5 Ball Array, WLP
  - Small Total Solution Size (24mm^2)

Applications

- Remote Controls
- Wearables
- Internet of Things (IoT)

Ordering Information *appears at end of data sheet.*

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

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Absolute Maximum Ratings

CHGIN to AGND	-0.3V to +30.0V
SCL, SDA to AGND	-0.3V to V_{IO} + 0.3V
SYS, BATT to AGND	-0.3V to +6.0V
IN_SBB, GPIO0-7 to AGND	-0.3V to V_{SYS} + 0.3V
CS_EN, nEN, nRST, nIRQ, to AGND	-0.3V to V_{SYS} + 0.3V
THM, TBIAS, V_L to AGND	-0.3V to +6.0V
LDO to AGND (Note 1)	-0.3V to V_{IN_LDO} + 0.3V
CS to CS_GND	-0.3V to +6.0V
IN_SBB to PGND	-0.3V to +6.0V
BST to LXB	-0.3V to +6.0V
CS_GND, PGND to AGND	-0.3V to +0.3V
V_{IO} to AGND	-0.3V to V_{SYS} + 0.3V
BST to IN_SBB	-0.3V to +6.0V
SBB0, SBB1, SBB2 to PGND (Note 1)	-0.3V to +6.0V
IN_LDO to AGND	-0.3V to +6.0V
nEN, nIRQ, nRST, SDA, SCL, GPIO0-7 Continuous Current	±20mA
CHGIN Continuous Current	$1.2A_{RMS}$
SYS Continuous Current	$1.2A_{RMS}$
BATT Continuous Current (Note 2)	$1.2A_{RMS}$
LXA Continuous Current (Note 3)	$1.2A_{RMS}$
LXB Continuous Current (Note 4)	$1.2A_{RMS}$
SBB0, SBB1, SBB2 Short-Circuit Duration	Continuous
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Soldering Temperature (reflow)	+260°C
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 20.4mW/°C above +70°C)	1632mW

Note 1: When the active discharge resistor is engaged, limit its power dissipation to an average of 10mW.

Note 2: Do not repeatedly hot-plug a source to the BATT terminal at a rate greater than 10Hz. Hot plugging low-impedance sources results in an ~8A momentary (~2µs) current spike.

Note 3: LXA has internal clamping diodes to PGND and IN_SBB. It is normal for these diodes to briefly conduct during switching events. Avoid steady-state conduction of these diodes.

Note 4: Do not externally bias LXB. LXB has an internal low-side clamping diode to PGND, and an internal high-side clamping diode that dynamically shifts to the selected SIMO output. It is normal for these internal clamping diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to V_{SBB0} +0.3V.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

35 WLP 0.4mm Pitch

PACKAGE CODE	W352C3+1
Outline Number	21-100152
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	35°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics—Global Resources

(V_{SYS} = 3.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Operating Voltage Range	V_{SYS}			2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	Current measured into BATT, IN_SBB, and IN_LDO, all resources are off (LDO, SBB0, SBB1, SBB2, CS), T_A = +25°C	Main bias is off (SBIA_EN = 0). This is the standby state		0.3		µA
			Main bias is on in low-power mode (SBIA_EN = 1, SBIA_LPM = 1)		1		
		Current measured into BATT, IN_SBB, and IN_LDO, all resources are off (LDO, SBB0, SBB1, SBB2, CS), T_A = +25°C	Main bias is on in normal mode (SBIA_EN = 1, SBIA_LPM = 0)		28		
Quiesent Supply Current	I_Q	Current measured into BATT, IN_SBB, and IN_LDO. LDO, SBB0, SBB1, and SBB2 are enabled with no load. CS is disabled.	Main bias is in low-power mode (SBIA_LPM = 1)		13		µA
			Main bias is in normal mode (SBIA_LPM = 0)		48		
Main Bias Enable Time	t_{SBIAS_EN}				0.5		ms
VOLTAGE MONITORS/POWER-ON RESET (POR)							
POR Threshold	V_{POR}	V_{SYS} falling		1.65	1.9	2.15	V
POR Threshold Hysteresis					100		mV
VOLTAGE MONITORS/UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	$V_{SYSUVLO}$	V_{SYS} falling, UVLO_F[3:0] = 0xA		2.4	2.6	2.8	V
UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$	UVLO_H[3:0] = 0x5			300		mV
VOLTAGE MONITORS/OVERVOLTAGE LOCKOUT (OVLO)							
OVLO Threshold	$V_{SYSOVLO}$	V_{SYS} rising		5.65	5.85	6.05	V
THERMAL MONITORS							
Overtemperature Lockout Threshold	T_{OTLO}	T_J rising			165		°C
Thermal Alarm Temperature 1	T_{JAL1}	T_J rising			80		°C
Thermal Alarm Temperature 2	T_{JAL2}	T_J rising			100		°C
Thermal Alarm Temperature Hysteresis					15		°C

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ENABLE INPUT (nEN)							
nEN Input Leakage Current	I_{nEN_LKG}	V_{SYS} = 5.5V, V_{nEN} = 0V, and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
nEN Input Falling Threshold	$V_{TH\_nEN\_F}$	nEN Falling		V_{SYS} - 1.4	V_{SYS} - 1.0		V
nEN Input Rising Threshold	$V_{TH\_nEN\_R}$	nEN Rising			V_{SYS} - 0.9	V_{SYS} - 0.6	V
Debounce Time	t_{DBNC_nEN}	DBEN_nEN = 0			100		µs
		DBEN_nEN = 1			30		ms
Manual Reset Time	t_{MRST}			14	16	20	s
OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Falling Edge Time	t_{f_nIRQ}	C_{nIRQ} = 25pF			2		ns
Leakage Current	I_{nIRQ_LKG}	V_{SYS} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), V_{nIRQ} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
		V_{SYS} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), V_{nIRQ} = 0V and 5.5V	T_A = +85°C		±0.01		
OPEN-DRAIN RESET OUTPUT (nRST)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Falling Edge Time	t_{f_nRST}	C_{RST} = 25pF			2		ns
nRST Deassert Delay Time	t_{RSTODD}	See Figure 5 and Figure 7 for more information			5.12		ms
nRST Assert Delay Time	t_{RSTOAD}	See Figure 5 for more information			10.24		ms
Leakage Current	I_{nRST_LKG}	V_{SYS} = V_{IO} = 5.5V, nRST set to be high impedance (i.e., not reset), V_{nRST} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage Low	V_{IL}	V_{SYS} = 3.8V				0.3 X V_{SYS}	V
Input Voltage High	V_{IH}	V_{SYS} = 3.8V		0.7 x V_{SYS}			V
Input Leakage Current	I_{GPI_LKG}	DIRx = 1, V_{SYS} = 5.5V, V_{GPIOx} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
Output Voltage Low	V_{OL}	I_{SINK} = 8mA				0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 8mA		0.8 x V_{SYS}			V
Input Debounce Time	t_{DBNC_GPI}	DB_CNFG[1:0] = 0b00			1.25		ms
		DB_CNFG[1:0] = 0b01			2.5		
		DB_CNFG[1:0] = 0b10			5		
		DB_CNFG[1:0] = 0b11			10		
GPIO Manual Reset Time	t_{MRST_GPIO}	GPIO_MRT[1:0] = 0b00			10		s
		GPIO_MRT[1:0] = 0b01			5		
		GPIO_MRT[1:0] = 0b10			2.5		
		GPIO_MRT[1:0] = 0b11			1.25		
Output Falling Edge Time	t_{f_GPIO}	C_{GPIO} = 25pF			3		ns
Output Rising Edge Time	t_{r_GPIO}	C_{GPIO} = 25pF			3		ns
FLEXIBLE POWER SEQUENCER							
Power-Up Event Periods	t_{EN}	See Figure 6			1.28		ms
Power-Down Event Periods	t_{DIS}	See Figure 6			2.56		ms

Electrical Characteristics—Smart Power Selector Charger

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGER/DC INPUT						
CHGIN Valid Voltage Range	V_{CHGIN}	Initial CHGIN voltage before enabling charging	4.10		7.25	V
CHGIN Standoff Voltage Range	$V_{STANDOFF}$	DC Rising		28		V
CHGIN Overvoltage Threshold	V_{CHGIN_OVP}	DC rising	7.25	7.50	7.75	V
CHGIN Overvoltage Hysteresis				100		mV
CHGIN Undervoltage Lockout	V_{CHGIN_UVLO}	DC rising	3.9	4.0	4.1	V
CHGIN Undervoltage-Lockout Hysteresis				500		mV
Input Current-Limit Range	$I_{CHGIN-LIM}$	V_{SYS} = $V_{SYS-REG}$ - 100mV, programmable in 95mA steps	95		475	mA
Input Current-Limit Accuracy		$I_{CHGIN-LIM}$ = 95mA, V_{SYS} = $V_{SYS-REG}$ - 100mV	90	95	100	mA
Minimum Input Voltage Regulation Range	$V_{CHGIN-MIN}$	V_{CHGIN} falling due to loading conditions and/or high-impedance charge source, programmable in 100mV increments with VCHGIN_MIN[2:0]	4.0		4.7	V
Minimum Input Voltage Regulation Accuracy		$V_{CHGIN-MIN}$ = 4.5V (VCHGIN_MIN[2:0] = 0b101), I_{CHGIN} reduced by 10%	4.32	4.50	4.68	V
Charger Input Debounce Timer	$t_{CHGIN-DB}$	V_{CHGIN} = 5V, time before CHGIN is allowed to deliver current to SYS or BATT	100	120	140	ms
CHARGER/SUPPLY AND QUIESCENT CURRENTS						
BATT Bias Current	$I_{BATT-BIAS}$	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), charging is finished (CHG_DTLS indicate done), I_{SYS} = 0mA		5		µA
CHGIN Supply Current	I_{CHGIN}	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), charging is finished (CHG_DTLS indicate done), I_{SYS} = 0mA		1.0	1.8	mA
		V_{CHGIN} = 0V to 1V, V_{BATT} = 3.3V, I_{SYS} = 0A			50	µA
CHGIN Suspend Supply Current	$I_{CHGIN-SUS}$	V_{CHGIN} = 5V, charger in USB suspend (USBS = 1)			50	µA
CHARGER/PREQUALIFICATION						
Charge and Input Current-Limit Soft-Start Slew Time		Zero to full scale		1		ms

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prequalification Voltage Threshold Range	V_{PQ}	Charger is in prequalification mode when $V_{BATT} < V_{PQ}$, this threshold has 100mV of hysteresis, programmable in 100mV steps with CHG_PQ[2:0]	2.3		3.0	V
Prequalification Voltage Threshold Accuracy		V_{PQ} = 3.0V	-3		+3	%
Prequalification Mode Charge Current	I_{PQ}	V_{BATT} = 2.5V, V_{PQ} = 3.0V, expressed as a percentage of $I_{FAST-CHG}$, I_PQ = 0		10		%
		V_{BATT} = 2.5V, V_{PQ} = 3.0V, expressed as a percentage of $I_{FAST-CHG}$, I_PQ = 1		20		
Prequalification Safety Timer	t_{PQ}	$V_{BATT} < V_{PQ}$ = 3.0V	27	30	33	minutes
CHARGER/FAST-CHARGE						
Fast-Charge Voltage Range	$V_{FAST-CHG}$	I_{BATT} = 0mA, programmable in 25mV steps with CHG_CV[5:0]	3.6		4.6	V
Fast-Charge Voltage Accuracy		I_{BATT} = 0mA, $V_{FAST-CHG}$ = 4.3V, V_{SYS} = 4.5V, T_A = +25°C	-0.5	±0.15	+0.5	%
		I_{BATT} = 0mA, $V_{FAST-CHG}$ = 3.6V to 4.6V, V_{SYS} = 4.8V			1.0	
Fast-Charge Current Range	$I_{FAST-CHG}$	Programmable in 7.5mA steps with CHG_CC[5:0]	7.5		300	mA
Fast-Charge Current Accuracy		T_A= +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV, $I_{FAST-CHG}$ = 15mA	-1.5		+1.5	%
		$I_{FAST-CHG}$ = 300mA	-1.5		+1.5	
Fast-Charge Current Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV T_A = 0°C to +85°C	-10		+10	%
Fast-Charge Safety Timer Range	t_{FC}	Programmable in 2 hour increments or disabled with T_FAST_CHG[1:0], from prequal done to timerfault	3		7	hours
Fast-Charge Safety Timer Accuracy		t_{FC} = 3 hours	-10		+10	%
Fast-Charge Safety Timer Suspend Threshold		Fast-charge CC mode, loading conditions and/or a weak charging source caused charge current to drop below this threshold, expressed as a percentage of $I_{FAST-CHG}$		20		%
Junction Temperature Regulation Setting Range	T_{J-REG}	Programmable in 10°C steps with TJ_REG_SET[2:0]	60		100	°C
Junction Temperature Regulation Loop Gain	G_{TJ-REG}	Rate at which $I_{FAST-CHG}/I_{PQ}$ is reduced to maintain T_{J-REG}, expressed a percentage of $I_{FAST-CHG}/I_{PQ}$ per degree centigrade rise		-5.4		%/°C

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGER/TERMINATION AND TOP-OFF						
End-of-Charge Termination Current	I_{TERM}	I_TERM = 0b00 (expressed as a percentage of $I_{FAST-CHG}$)		5		%
		I_TERM = 0b01 (expressed as a percentage of $I_{FAST-CHG}$)		7.5		
		I_TERM = 0b10 (expressed as a percentage of $I_{FAST-CHG}$)		10		
		I_TERM = 0b11 (expressed as a percentage of $I_{FAST-CHG}$)		15		
End-of-Charge Termination Current Accuracy		$I_{FAST-CHG}$ = 15mA, I_{TERM} = 1.5mA (10% of $I_{FAST-CHG}$), T_A = +25°C	1.35	1.5	1.65	mA
		$I_{FAST-CHG}$ = 300mA, I_{TERM} = 30mA (10% of $I_{FAST-CHG}$), T_A = +25°C	27	30	33	
Top-Off Timer Range	t_{TO}	I_{BATT} < I_{TERM}, programmable in 5 minute steps with T_TOPOFF[2:0]	0		35	minutes
Top-Off Timer Accuracy		t_{TO} = 10 minutes	-10		+10	%
CHARGER/DEVICE ON-RESISTANCE AND LEAKAGE						
BATT to SYS On-Resistance		V_{BATT} = 3.7V, I_{BATT} = 300mA, V_{CHGIN} = 0V, battery is discharging to SYS		100		mΩ
Charger FET Leakage Current		V_{SYS} = 4.5V, V_{BATT} = 0V, T_A = +25°C, charger disabled		0.1	1.0	µA
		V_{SYS} = 4.5V, V_{BATT} = 0V, T_A = +85°C, charger disabled		1		
CHGIN to SYS On-Resistance		V_{CHGIN} = 4.65V, I_{CHGIN} = $I_{CHGIN-LIM}$ = 450mA		600		mΩ
Input FET Leakage Current		V_{CHGIN} = 0V, V_{SYS} = 4.2V, T_A = +25°C, body-switched diode is reverse biased		0.1	1.0	µA
		V_{CHGIN} = 0V, V_{SYS} = 4.2V, T_A = +85°C, body-switched diode is reverse biased		1		
CHARGER/SYSTEM NODE						
System Voltage Regulation Range	$V_{SYS-REG}$	Programmable in 25mV steps with VSYS_REG[4:0]	4.1		4.8	V
System Voltage Regulation Accuracy	V_{SYS}	$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA, T_A = +25°C	4.41	4.50	4.59	V
		$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA, T_A = -40°C to +85°C	4.365	4.500	4.635	
Minimum System Voltage Regulation Loop Setpoint	$V_{SYS-MIN}$	V_{CHGIN} = 5V, $V_{SYS-REG}$ = 4.5V, V_{SYS} < $V_{SYS-REG}$ due to I_{CHGIN} = $I_{CHGIN-LIM}$ (input in current limit), battery charging, I_{BATT} reduced to 50% of $I_{FAST-CHG}$ (minimum system voltage regulation active)	4.34	4.40	4.45	V
Supplement Mode System Voltage Regulation		I_{SYS} = 150mA		V_{BATT} - 0.15V		V

Electrical Characteristics—Adjustable Thermistor Temperature Monitors

(V_{CHGIN} = 5.0V, V_{SYS}= 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JEITA TEMPERATURE MONITORS						
TBIAS Voltage	V_{TBIAS}	THM_EN = 1, V_{CHGIN} = 5V		1.25		V
JEITA Cold Threshold Range	V_{COLD}	Voltage rising threshold, programmable with THM_COLD[1:0] in 5°C increments when using an NTC β = 3380K	0.867		1.024	V
JEITA Cool Threshold Range	V_{COOL}	Voltage rising threshold, programmable with THM_COOL[1:0] in 5°C increments when using an NTC β = 3380K	0.747		0.923	V
JEITA Warm Threshold Range	V_{WARM}	Voltage falling threshold, programmable with THM_WARM[1:0] in 5°C increments when using an NTC β = 3380K	0.367		0.511	V
JEITA Hot Threshold Range	V_{HOT}	Voltage falling threshold, programmable with THM_HOT[1:0] in 5°C increments when using an NTC β = 3380K	0.291		0.411	V
Temperature Threshold Accuracy		Voltage threshold accuracy expressed as temperature for an NTCβ = 3380K		±3		°C
Temperature Threshold Hysteresis		Temperature hysteresis set on each voltage threshold for an NTCβ = 3380K		3		°C
JEITA Modified Fast-Charge Voltage Range	$V_{FAST\text{-}CHG\_JEITA}$	I_{BATT} = 0mA, programmable in 25mV steps, battery is either cool or warm	3.6		4.6	V
JEITA Modified Fast-Charge Current Range	$I_{FAST\text{-}CHG\_JEITA}$	Programmable in 7.5mA steps, battery is either cool or warm	7.5		300	mA

Electrical Characteristics—Analog Multiplexer and Power Monitor AFEs

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG MULTIPLEXER AND POWER MONITOR AFEs						
Full-Scale Voltage	V_{FS}			1.25		V
SYS Voltage Monitor Gain	G_{VSYS}	V_{FS} corresponds to maximum $V_{SYS\text{-}REG}$ setting		0.26		V/V
ANALOG MULTIPLEXER AND POWER MONITOR AFEs/CHGIN POWER						
CHGIN Current Monitor Gain	G_{ICHGIN}	V_{FS} corresponds to maximum $I_{CHGIN\text{-}LIM}$ setting		2.632		V/A
CHGIN Voltage Monitor Gain	G_{VCHGIN}	V_{FS} corresponds to V_{CHGIN_OVP}		0.167		V/V

Electrical Characteristics—Analog Multiplexer and Power Monitor AFEs (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG MULTIPLEXER AND POWER MONITOR AFEs/BATT MONITOR							
Battery Charge Current Monitor Gain	$G_{IBATT\text{-}CHG}$	V_{FS} corresponds to 100% of $I_{FAST\text{-}CHG}$ setting (CHG_CC[5:0])			12.5		mV/%
Charge Current Monitor Accuracy		$I_{FAST\text{-}CHG}$ = 15mA, T_A = +25°C, V_{BATT} = $V_{FAST\text{-}CHG}$ - 300mV		-3.5		+3.5	%
		$I_{FAST\text{-}CHG}$ = 300mA, T_A = +25°C, V_{BATT} = $V_{FAST\text{-}CHG}$ - 300mV		-3.5		+3.5	
Charge Current Monitor Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST\text{-}CHG}$ - 300mV		-10		+10	%
Battery Discharge Monitor Full-Scale Current Range	$I_{DISCHG\text{-}SCALE}$	Programmable with IMON_DISCHG_ SCALE[3:0]		8.2		300	mA
Battery Discharge Current Monitor Accuracy		15mA to 300mA battery discharge current, $I_{DISCHG\text{-}SCALE}$ = 300mA		-15		+15	%
Battery Discharge Current Monitor Offset		I_{BATT} = 0mA	T_A = 0°C to +85°C	-0.5		+0.8	mA
			T_A = -40°C	-1.1		+1.4	
Battery-Voltage Monitor Gain	G_{VBATT}	V_{FS} corresponds to maximum $V_{FAST\text{-}CHG}$ setting			0.272		V/V
ANALOG MULTIPLEXER AND POWER MONITOR AFEs/ANALOG MULTIPLEXER							
Channel Switching Time					0.3		µs
Off Leakage Current		V_{AMUX} = 0V, AMUX is high impedance	T_A = +25°C		1	500	nA
			T_A = +85°C		1		µA
ANALOG MULTIPLEXER AND POWER MONITOR AFEs/THM AND TBIAS							
THM Voltage Monitor Gain	G_{VTHM}				1		V/V
TBIAS Voltage Monitor Gain	G_{VTBIAS}				1		V/V

Electrical Characteristics—SIMO Buck-Boost

(V_{SYS} = 3.8V, V_{IN_SBB} = 3.8V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage Range	V_{IN_SBB}			2.8	3.8	5.5	V
Shutdown Current (Note 5)		SBB0, SBB1, SBB2 are disabled, V_{SYS} = V_{IN_SBB} = 5.5V, V_{LXA} = 0V	T_A = +25°C		0.05	1	µA
			T_A = 0°C to +85°C		0.25		
SIMO Quiescent Supply Current (Note 5)	I_{Q_SBB0}	No load	SBB0 set to 5.3V		5.0		µA
	I_{Q_SBB1}		SBB1 set to 1.9V		3.0		
	I_{Q_SBB2}		SBB2 set to 3.2V		4.5		
GENERAL CHARACTERISTICS/OUTPUT VOLTAGE RANGE (SBB0)							
Minimum Output Voltage				2.35			V
Maximum Output Voltage						5.5	V
Output DAC Bits					6		bits
Output DAC LSB Size					50		mV
GENERAL CHARACTERISTICS/OUTPUT VOLTAGE RANGE (SBB1)							
Minimum Output Voltage				1.412			V
Maximum Output Voltage						2.2	V
Output DAC Bits					6		bits
Output DAC LSB Size					12.5		mV
GENERAL CHARACTERISTICS/OUTPUT VOLTAGE RANGE (SBB2)							
Minimum Output Voltage				0.85			V
Maximum Output Voltage						4	V
Output DAC Bits					6		bits
Output DAC LSB Size					50		mV
STATIC OUTPUT VOLTAGE ACCURACY							
Output Voltage Accuracy		T_A = 0°C to +85°C (Note 6)		-4		+4	%
TIMING CHARACTERISTICS							
Soft-Start Ramp Rate	dV/dt_{SS}			2	5.0	8	mV/µs

Electrical Characteristics—SIMO Buck-Boost (continued)

(V_{SYS} = 3.8V, V_{IN_SBB} = 3.8V, C_{SBBx} = 10μF, L = 1.5μH, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER STAGE CHARACTERISTICS							
LXA Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V, or 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	μA
			T_A = +85°C		±1.0		
LXB Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V or 5.5V, all V_{SBBx} = 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	μA
			T_A = +85°C		±1.0		
BST Leakage Current		V_{IN_SBB} = 5.5V, V_{LXB} = 5.5V, V_{BST} = 11V	T_A = +25°C		+0.01	+1.0	μA
			T_A = +85°C		+0.1		
Disabled Output Leakage Current		SBB0, SBB1, SBB2 are disabled, active-discharge disabled (ADE_SBBx = 0), V_{SBBx} = 5.5V, V_{LXB} = 0V, V_{SYS} = V_{IN_SBB} = V_{BST} = 5.5V	T_A = +25°C		+0.1	+1.0	μA
			T_A = +85°C		+0.2		
Active Discharge Impedance	R_{AD_SBBx}	SBB0, SBB1, SBB2 are disabled, active discharge enabled (ADE_SBBx = 1)		80	140	260	Ω
CONTROL SCHEME							
Peak Current Limit (Note 7)	I_{P_SBB}	IP_SBBx = 0b11		0.414	0.500	0.586	A
		IP_SBBx = 0b10		0.589	0.707	0.806	
		IP_SBBx = 0b01		0.713	0.866	0.947	
		IP_SBBx = 0b00		0.892	1.000	1.108	

Note 5: Guaranteed by design and characterization but not directly production tested. Production test coverage is provided by the quiescent supply current specification.

Note 6: Measured as the falling threshold of the output voltage where LXA switches high.

Note 7: Typical values align with bench observations using the stated conditions. Minimum and maximum values are tested in production with DC currents. See the *Typical Operating Characteristics* SIMO switching waveforms for more insight on this specification.

Electrical Characteristics—LDO

(V_{SYS} = 3.8V, V_{IN_LDO} = 5.3V, V_{LDO} = 5.14V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage	V_{IN_LDO}	Note 8		3.733		5.5	V
LDO Shutdown Current	I_{IN_LDO}	Current measured into IN_LDO, LDO output disabled (Note 9)			0.1	1	µA
LDO Quiescent Supply Current (Note 9)	I_{IN_LDO}	Current measured into IN_LDO, I_{LDO} = 0mA, LDO output enabled and in regulation, V_{IN_LDO} = 5.5V, V_{LDO} = 5.1375V			1.1	3.1	µA
Fixed Headroom Control Quiescent Current	I_{Q_FHC}	Additional current into SYS due to fixed headroom controller, V_{LDO} = 5.1375V, EN_FHC = 1			1.8	3.0	µA
Maximum Output Current	I_{OUT}			50			mA
Current Limit		V_{LDO} programmed to 5.1375V, V_{LDO} externally forced to 4.6375V			322		mA
Output Capacitance	C_{OUT}	Effective, derated capacitance. ESR must be less than 10mΩ, ESL must be less than 200pH		4	10	13	µF
GENERAL CHARACTERISTICS/OUTPUT VOLTAGE RANGE							
Output Voltage Range		Programmable with TV_LDO[6:0] in 12.5mV steps		3.7125		5.3000	V
Output DAC Bits					7		bits
Output DAC LSB Size					12.5		mV
STATIC CHARACTERISTICS							
Output Voltage Accuracy		V_{LDO} programmed from 4V to 5.1375V, V_{IN_LDO} = 5.3V,LDO not in dropout, I_{LDO} = 0mA to 20mA, T_A = 0°C to +85°C		-2		+2	%
FHC Headroom Voltage	V_{HDRM}	V_{LDO} = 5.175V, I_{LDO} = 20mA, EN_FHC = 1	V_HDRM[1:0] = 0b00		150		mV
			V_HDRM[1:0] = 0b01		175		
			V_HDRM[1:0] = 0b10		200		
			V_HDRM[1:0] = 0b11		225		

Electrical Characteristics—LDO (continued)

(V_{SYS} = 3.8V, V_{IN_LDO} = 5.3V, V_{LDO} = 5.14V, C_{LDO} = 10μF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS							
Enable Delay		T_A = +25°C			0.32		ms
Soft-Start Slew Rate	dV/dt_{SS}	V_{LDO} from 10% to 90% of final value, T_A = +25°C			1.6		V/ms
POWER STAGE CHARACTERISTICS							
Dropout Voltage	V_{LDO_DO}	5.1375V programmed output voltage (TV_LDO[6:0] = 0x72), V_{IN_LDO} = 5V, I_{LDO} = 20mA (Note 10)			4.6	20	mV
Active-Discharge Impedance	R_{AD_LDO}	Regulator disabled, active discharge enabled (ADE_LDO = 1)		50	100	200	Ω
Disabled Output Leakage Current		Regulator disabled, active discharge disabled (ADE_LDO = 0), V_{SYS} = V_{IN_LDO} = 5.5V, V_{LDO} = 5.5V and 0V	T_A = +25°C		+0.1	+1.0	μA
			T_A = 0°C to +85°C		+1.0		

Note 8: When the input voltage is within the specified range, the LDO headroom is being regulated by the fixed-headroom-control loop and the LDO output voltage is regulated by the LDO. However, the regulator can be in dropout. For example, if the output voltage is fixed at 5.14V and a 5V input is provided, the output is 5.14V minus the dropout voltage (V_{LDO} = V_{IN_LDO} - V_{LDO_DO}). To achieve the specified output voltage, the input voltage must be the output voltage plus the dropout voltage ($V_{IN\_LDO} \geq V_{LDO} + V_{LDO\_DO\_MAX}$).

Note 9: Guaranteed by design and characterization but not directly production tested. Production test coverage is provided by the Shutdown Supply Current and Quiescent Supply Current specification in the Electrical Characteristics—Global Resources table.

Note 10: The dropout voltage is the difference between the input voltage and the output voltage when the input voltage is within the valid input voltage range, but below the output voltage setpoint. For example, if the output voltage setpoint is 1.85V, the input voltage is 1.7V, and the actual output voltage is 1.65V, then the dropout voltage is 50mV (V_{LDO_DO} = V_{IN_LDO} - V_{LDO}).

Electrical Characteristics—Current Sink

(V_{SYS}= 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A= -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Supply Voltage		Supply voltage range for current sink V_{CS} = 400mV, I_{CS} = 350mA		3	3.8	5	V
Input Voltage for LED Termination				3	3.8	5.5	V
Current Sink Quiescent Current	I_Q	Change in supply current at SYS when current sink is enabled			400	550	µA
Current Sink Leakage		CS_PRE_EN = 0, V_{CS} = 4.2V			+0.1	+1.0	µA
CS_EN Input Voltage Low	$V_{CS\_EN\_IL}$	V_{SYS} = 3.8V			0.4		V
CS_EN Input Voltage High	$V_{CS\_EN\_IH}$	V_{SYS} = 3.8V			V_{IO}-0.4		V
CURRENT SINK RANGE							
Minimum Sink Current		CS_CURR[2:0] = 0b000			250		mA
Maximum Sink Current		CS_CURR[2:0] = 0b111			425		mA
Current Sink Accuracy		CS_CURR[2:0] = 0b100, V_{SYS} = 3.8V	T_A = +25°C	-3%	350	+3%	mA
			T_A = 0°C to +85°C	-5%	350	+5%	
Headroom Voltage	V_{CS_HDRM}	CS_CURR[2:0] = 0b100, I_{CS} = 350mA; minimum headroom is defined where current drops 3% from nominal value		400			mV
TIMING CHARACTERISTICS							
Frequency Range	F_{EN}	V_{SYS} = 3.8V,CS_CURR[2:0] = 0b100		10		500	KHz
Preenable Set-Up Time	t_{SU}	Minimum time to operate current sink after current sink preenable (CS_PRE_EN = 1)			10		µs
Watchdog Timer	t_{WD}	Time out after last CS_EN falling edge resulting in an IRQ. Reset after each rising edge of CS_EN			12.8		ms
TIMING CHARACTERISTICS/PULSE PERIOD SETTINGS							
Duty Cycle						50	%
Rise Time	t_{rCS}	V_{SYS} = 3.8V, CS_CURR[2:0] = 0b100, V_{CS_HDRM} = 600mV, T_A = 0°C to +85°C	Time from CS_EN rising edge to 90% of final DC current value.		100	500	ns
Overshoot	I_{CS_OS}	V_{SYS} = 3.8V, CS_CURR[2:0] = 0b100, V_{CS_HDRM} = 600mV, T_A = 0°C to +85°C	Percent overshoot above final DC current value		25%		%

Electrical Characteristics—I²C

(V_{SYS}= 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage Range	V_{IO}		1.7	1.8	3.6	V
V_{IO} Bias Current		V_{IO} = 3.6V, V_{SDA} = V_{SCL} = 0V or 3.6V, T_A = +25°C	-1	0	+1	µA
		V_{IO} = 1.7V, V_{SDA} = V_{SCL}= 0V or 1.7V	-1	0	+1	
SDA and SCL I/O Stage						
SCL, SDA Input High Voltage	V_{IH}	V_{IO} = 1.7V to 3.6V	0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}	V_{IO} = 1.7V to 3.6V			0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V and 3.6V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL} (Note 11)	t_{OF}				120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST MODE PLUS) (Note 11)						
Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 100pF) (Note 11)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns

Electrical Characteristics—I²C (continued)

(V_{SYS}= 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

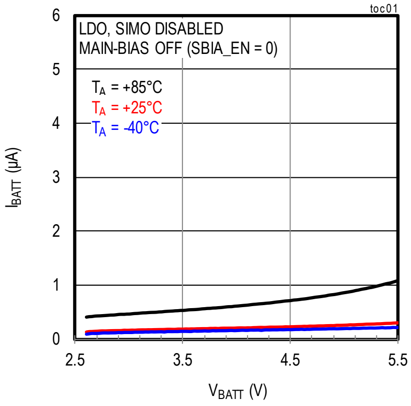
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Low Period	t_{LOW}		160			ns
SCL High Period	t_{HIGH}		60			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		70	ns
SCL Rise Time	t_{rCL}	T_A = +25°C	10		40	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{rCL1}	T_A = +25°C	10		80	ns
SCL Fall Time	t_{fCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{rDA}	T_A = +25°C	10		80	ns
SDA Fall Time	t_{fDA}	T_A = +25°C	10		80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 400pF) (Note 11)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		150	ns
SCL Rise Time	t_{RCL}	T_A = +25°C	20		80	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{RCL1}	T_A = +25°C	20		80	ns
SCL Fall Time	t_{FCL}	T_A = +25°C	20		80	ns
SDA Rise Time	t_{RDA}	T_A = +25°C	20		160	ns
SDA Fall Time	t_{FDA}	T_A = +25°C	20		160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

Note 11: Design guidance only. Not production tested.

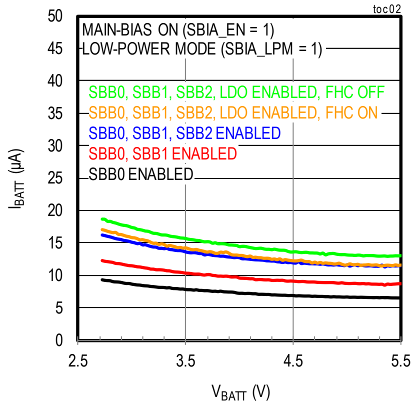
Typical Operating Characteristics

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.) (T_A = +25°C, unless otherwise noted.)

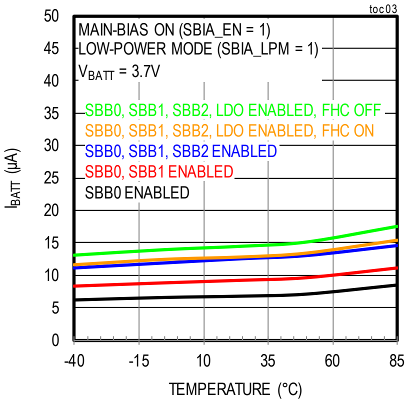
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



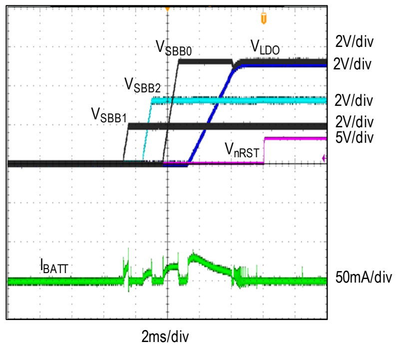
QUIESCENT SUPPLY CURRENT vs. BATTERY VOLTAGE



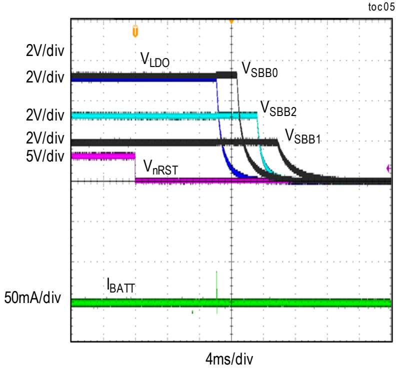
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



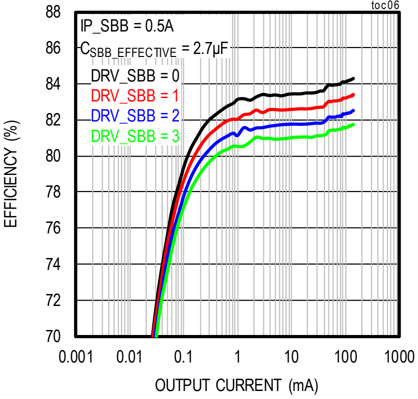
POWER-UP NO LOAD



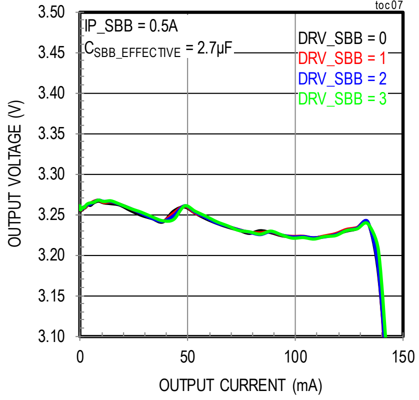
POWER-DOWN NO LOAD



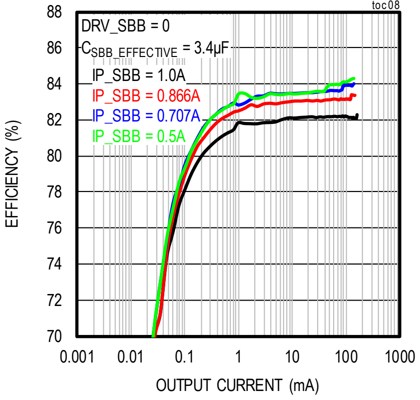
SIMO EFFICIENCY vs. OUTPUT CURRENT (3.3V OUTPUT, PER DRIVE STRENGTH)



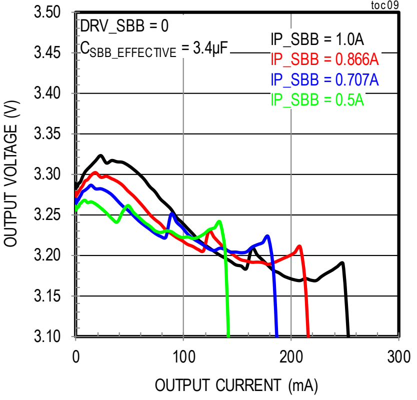
SIMO LOAD REGULATION (3.3V OUTPUT, PER DRIVE STRENGTH)



SIMO EFFICIENCY vs. OUTPUT CURRENT (3.3V OUTPUT, PER CURRENT LIMIT)

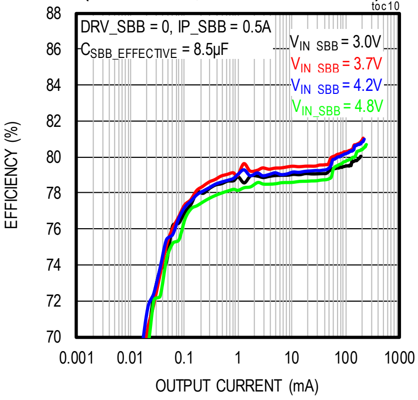


SIMO LOAD REGULATION (3.3V OUTPUT, PER CURRENT LIMIT)

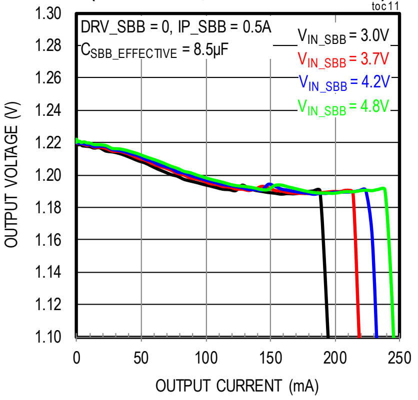


Typical Operating Characteristics (continued)

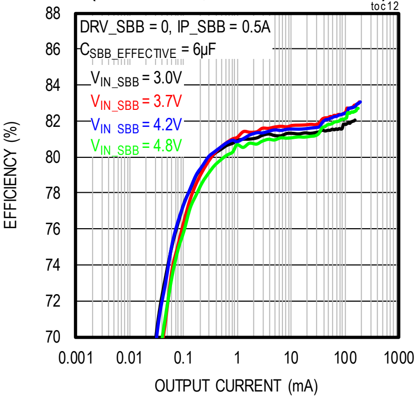
(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.) (T_A = +25°C, unless otherwise noted.)



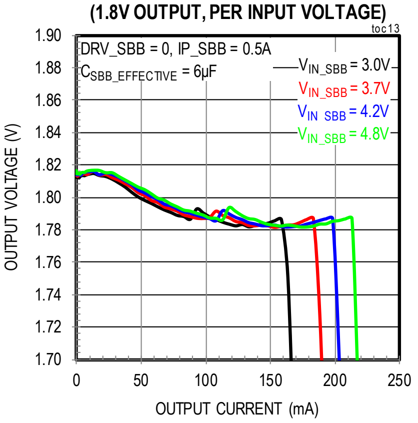
SIMO EFFICIENCY vs. OUTPUT CURRENT (1.2V OUTPUT, PER INPUT VOLTAGE)



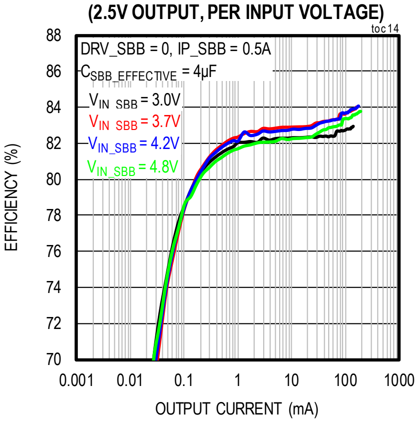
SIMO LOAD REGULATION (1.2V OUTPUT, PER INPUT VOLTAGE)



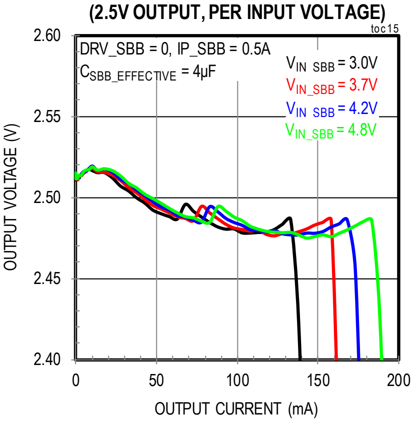
SIMO EFFICIENCY vs. OUTPUT CURRENT (1.8V OUTPUT, PER INPUT VOLTAGE)



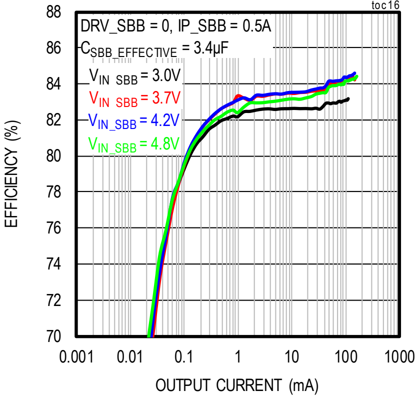
SIMO LOAD REGULATION (1.8V OUTPUT, PER INPUT VOLTAGE)



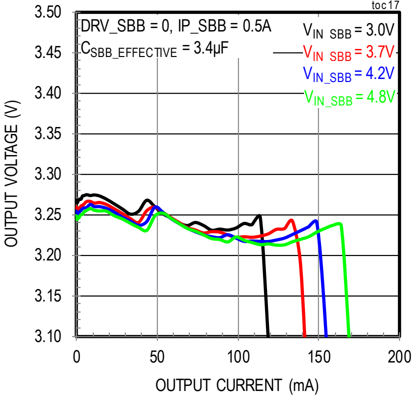
SIMO EFFICIENCY vs. OUTPUT CURRENT (2.5V OUTPUT, PER INPUT VOLTAGE)



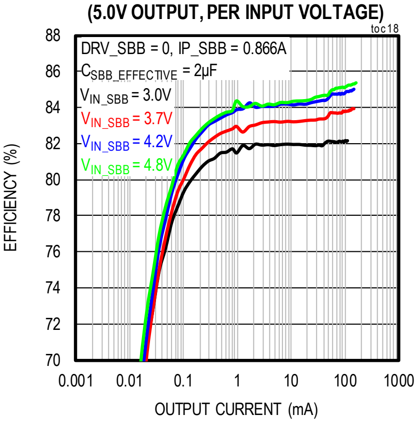
SIMO LOAD REGULATION (2.5V OUTPUT, PER INPUT VOLTAGE)



SIMO EFFICIENCY vs. OUTPUT CURRENT (3.3V OUTPUT, PER INPUT VOLTAGE)



SIMO LOAD REGULATION (3.3V OUTPUT, PER INPUT VOLTAGE)

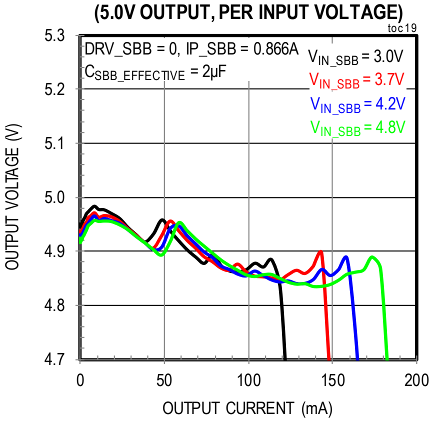


SIMO EFFICIENCY vs. OUTPUT CURRENT (5.0V OUTPUT, PER INPUT VOLTAGE)

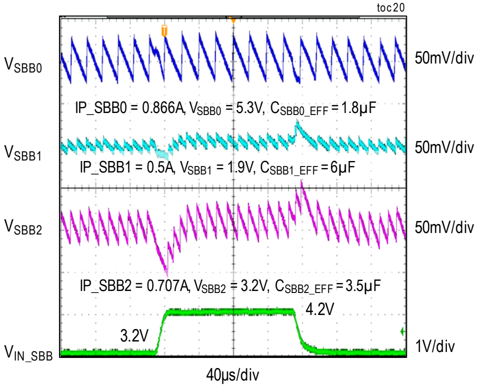
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.) (T_A = +25°C, unless otherwise noted.)

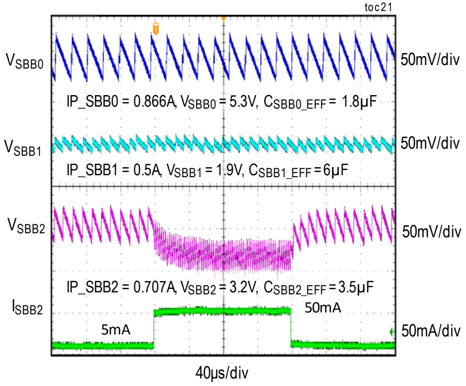
SIMO LOAD REGULATION (5.0V OUTPUT, PER INPUT VOLTAGE)



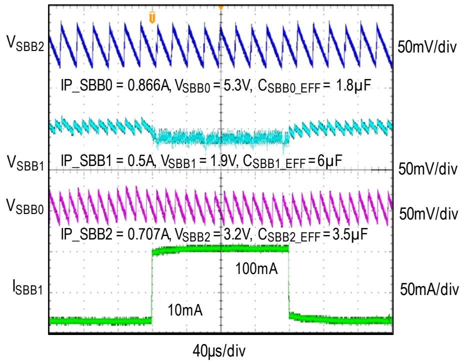
SIMO LINE TRANSIENT



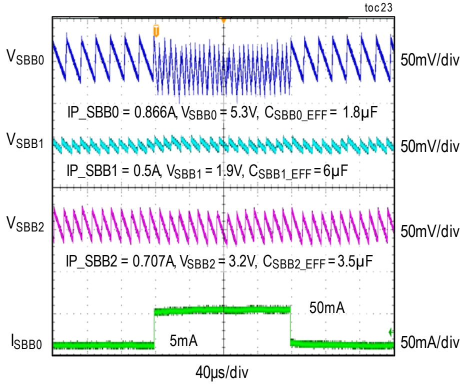
SBB2 LOAD TRANSIENT



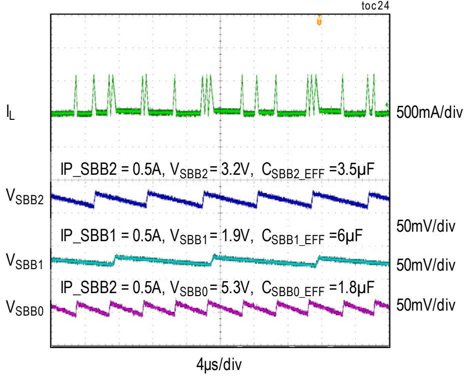
SBB1 LOAD TRANSIENT



SBB0 LOAD TRANSIENT



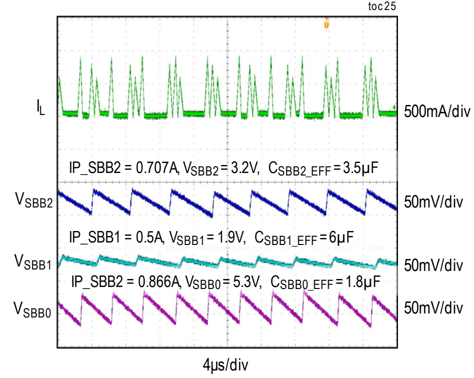
SIMO SWITCHING WAVEFORMS
LIGHT UTILIZATION
10mA PER CHANNEL



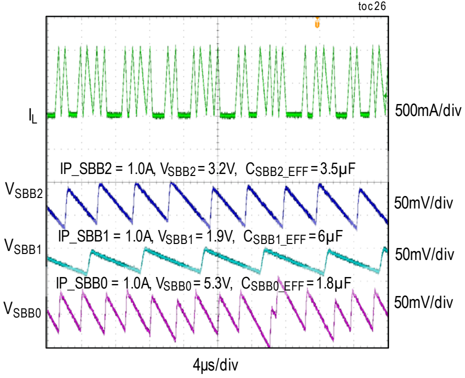
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)
(T_A = +25°C, unless otherwise noted.)

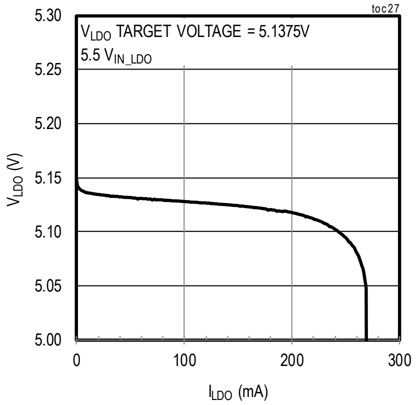
SIMO SWITCHING WAVEFORMS
MEDIUM UTILIZATION
25mA PER CHANNEL



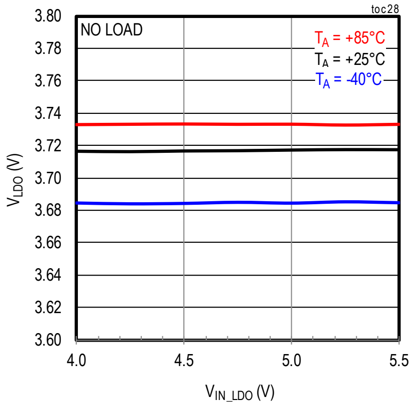
SIMO SWITCHING WAVEFORMS
HEAVY UTILIZATION
75mA PER CHANNEL



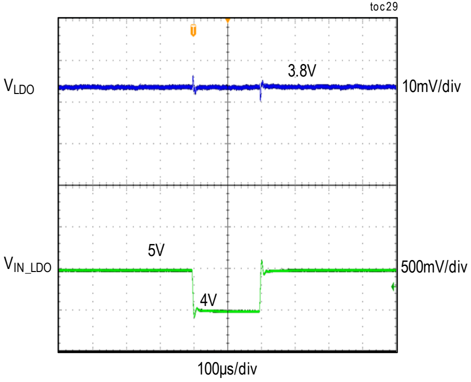
LDO LOAD REGULATION



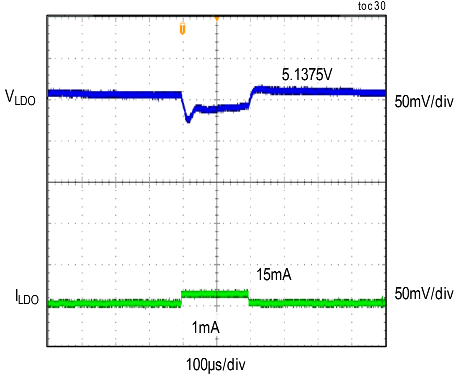
LDO LINE REGULATION



LDO LINE TRANSIENT

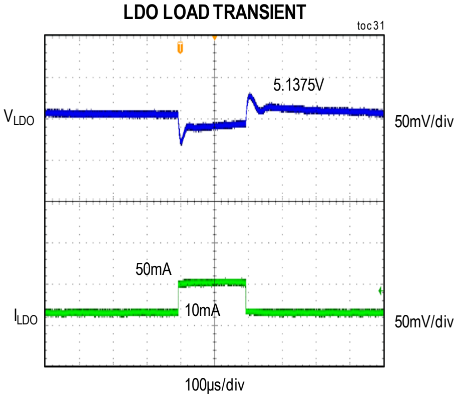


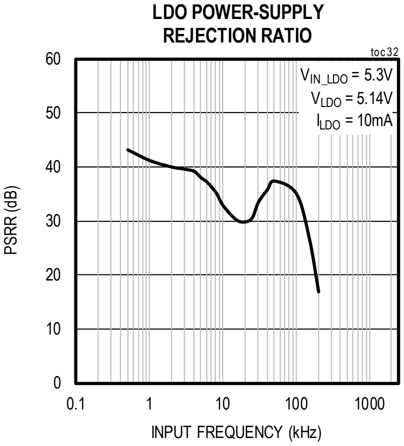
LDO LOAD TRANSIENT

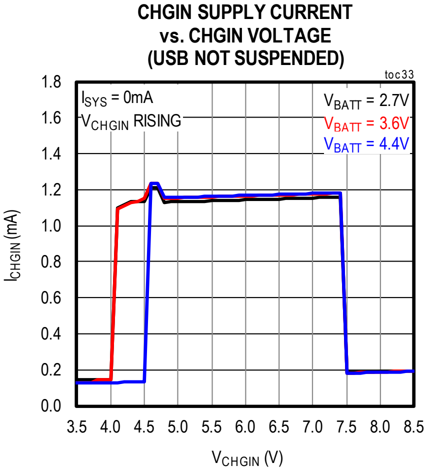


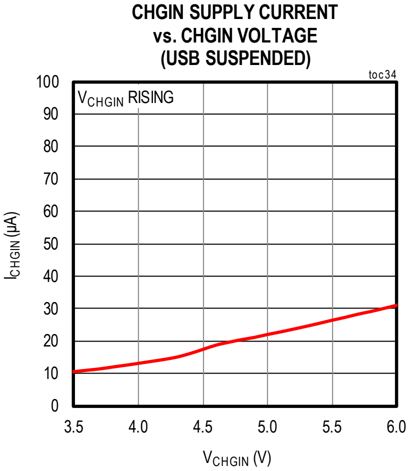
Typical Operating Characteristics (continued)

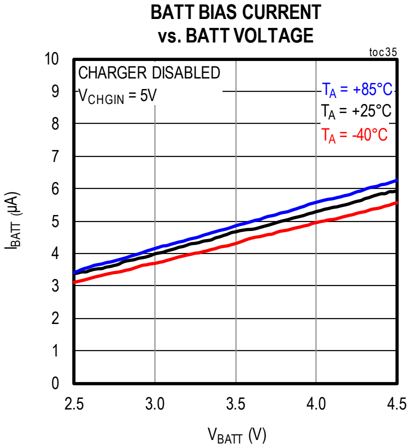
(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.) (T_A = +25°C, unless otherwise noted.)





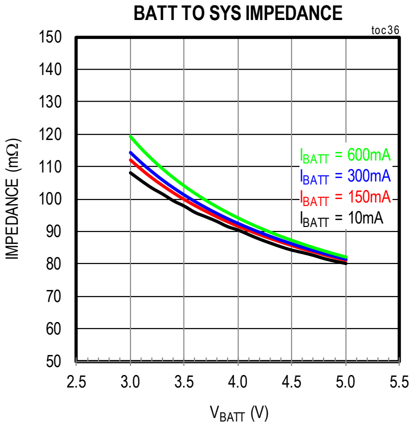


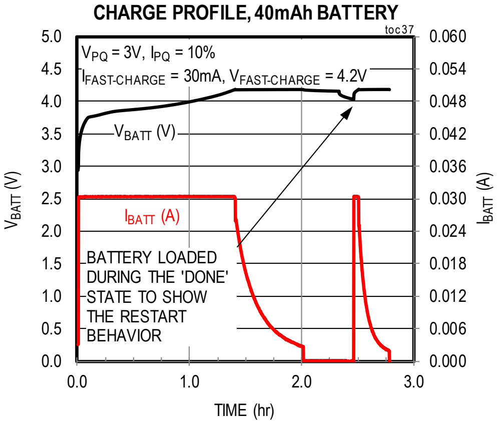


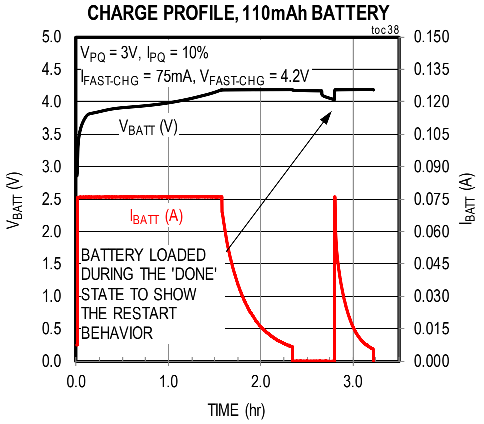


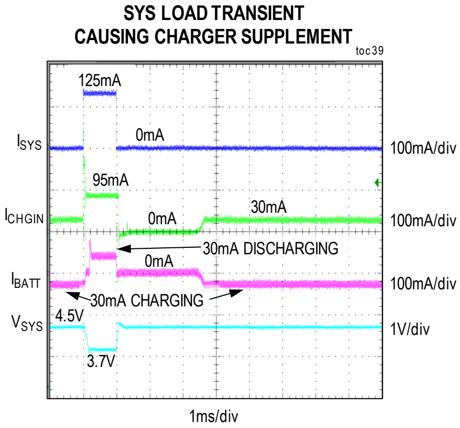
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)
(T_A = +25°C, unless otherwise noted.)

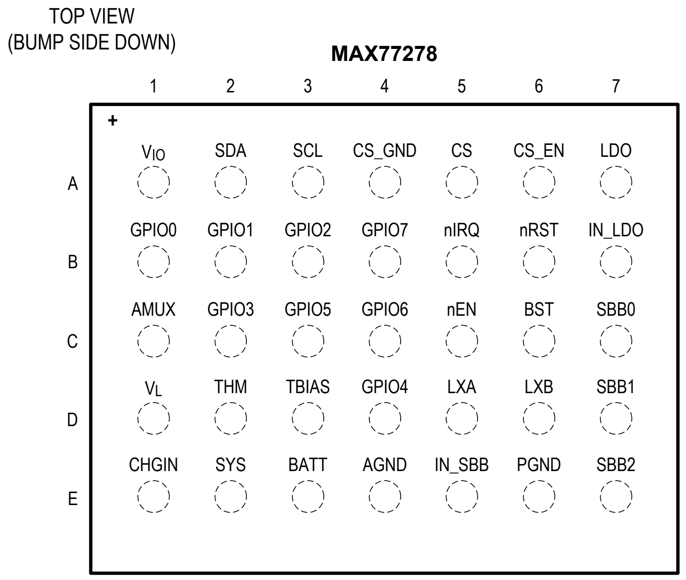








Bump Configuration



	1	2	3	4	5	6	7
A	V_{IO}	SDA	SCL	CS_GND	CS	CS_EN	LDO
B	GPIO0	GPIO1	GPIO2	GPIO7	nIRQ	nRST	IN_LDO
C	AMUX	GPIO3	GPIO5	GPIO6	nEN	BST	SBB0
D	V_L	THM	TBIAS	GPIO4	LXA	LXB	SBB1
E	CHGIN	SYS	BATT	AGND	IN_SBB	PGND	SBB2

WLP
(2.15mm x 3.15mm)

Bump Description

PIN	NAME	FUNCTION	TYPE
TOP LEVEL			
A1	V_{IO}	I^2C Interface Power	power input
A2	SDA	I^2C Data	digital i/o
A3	SCL	I^2C Clock	digital input
B1	GPIO0	General-Purpose Input/Output. The GPIO I/O stage is internally biased with V_{SYS}.	digital i/o
B2	GPIO1	General-Purpose Input/Output. The GPIO I/O stage is internally biased with V_{SYS}.	digital i/o
B3	GPIO2	General-Purpose Input/Output. The GPIO I/O stage is internally biased with V_{SYS}.	digital i/o
B4	GPIO7	General-Purpose Input/Output. The GPIO I/O stage is internally biased with V_{SYS}.	digital i/o
B5	nIRQ	Active-Low, Open-Drain Interrupt Output. Connect a 100kΩ pullup resistor between nIRQ and a voltage equal to or less than V_{SYS}.	digital output
B6	nRST	Active-Low, Open-Drain Reset Output. Connect a 100kΩ pullup resistor between nRST and a voltage equal to or less than V_{SYS}.	digital output
C2	GPIO3	General-Purpose Input/Output. The GPIO I/O stage is internally biased with V_{SYS}.	digital i/o
C3	GPIO5	General-Purpose Input/Output. The GPIO I/O stage is internally biased with V_{SYS}.	digital i/o
C4	GPIO6	General-Purpose Input/Output. The GPIO I/O stage is internally biased with V_{SYS}.	digital i/o
C5	nEN	Active-Low, Enable Input. nEN supports push-button or slide-switch configurations.	digital input
D4	GPIO4	General-Purpose Input/Output. The GPIO I/O stage is internally biased with V_{SYS}.	digital i/o
E4	AGND	Quiet Ground. Connect AGND, PGND, and CS_GND to the low-impedance ground plane of the PCB.	ground

Bump Description (continued)

PIN	NAME	FUNCTION	TYPE
CHARGER			
C1	AMUX	Analog Multiplexer Output. Connect to system ADC to perform conversions on charger power signals.	analog output
D1	V_L	Internal Charger 3V Logic Supply Powered from CHGIN. Bypass to GND with a 1µF ceramic capacitor. Do not load V_L externally.	power
D2	THM	Thermistor Monitor. Thermally couple an NTC to the battery and connect between THM and GND.	analog input
D3	TBIAS	Thermistor Bias Supply. Connect a resistor equal to the NTC's room temperature resistance between TBIAS and THM. Do not load TBIAS with other external circuitry.	analog
E1	CHGIN	Charger Input. Connect to a DC charging source. Bypass to GND with a 4.7µF ceramic capacitor.	power input
E2	SYS	System Power Output. SYS provides power to the system resources as well as the control logic of the device. Bypass to GND with a 22µF ceramic capacitor.	power output
E3	BATT	Li+ Battery Connection. Connect to positive battery terminal. Bypass to GND with a 4.7µF ceramic capacitor.	power i/o
LDO			
A7	LDO	Linear Regulator Output	power output
B7	IN_LDO	Linear Regulator Input	power input
IR-LED CS			
A4	CS_GND	Power Ground for the Current Sink. Connect CS_GND, PGND, and AGND to the low-impedance ground plane of the PCB.	ground
A5	CS	Current Sink Port. CS is typically connected to the cathode of an LED and is capable of sinking up to 425mA of pulsed current.	power
A6	CS_EN	Current Sink Enable Input. Internally biased with V_{IO}. Connect to ground if unused.	digital input
SIMO BUCK BOOST			
C6	BST	SIMO Power Input for the High-Side Output NMOS Drivers. Connect a 3300pF ceramic capacitor between BST and LXB.	power input
C7	SBB0	SIMO Buck-Boost Output 0. SBB0 is the power output for channel 0 of the SIMO buck-boost. Bypass SBB0 to PGND with a 10µF ceramic capacitor.	power output
D5	LXA	Switching Node A. LXA is driven between PGND and IN_SBB when any SIMO channel is enabled. LXA is driven to PGND when all SIMO channels are disabled. Connect a 1.5µH inductor between LXA and LXB.	power i/o
D6	LXB	Switching Node B. LXB is driven between PGND and SBBx when SBBx is enabled. LXB is driven to PGND when all SIMO channels are disabled. Connect a 1.5µH inductor between LXA and LXB.	power i/o
D7	SBB1	SIMO Buck-Boost Output 1. SBB1 is the power output for channel 1 of the SIMO buck-boost. Bypass SBB1 to PGND with a 10µF ceramic capacitor.	power output
E5	IN_SBB	SIMO Power Input. Connect to SYS and bypass to PGND with a 22µF ceramic capacitor as close as possible to the IN_SBB pin.	power input
E6	PGND	Power Ground for the SIMO Low-Side FETs. Connect PGND, AGND, and CS_GND to the low-impedance ground plane of the PCB.	ground
E7	SBB2	SIMO Buck-Boost Output 2. SBB2 is the power output for channel 2 of the SIMO buck boost. Bypass SBB2 to PGND with a 10µF ceramic capacitor.	power output

Detailed Description

The MAX77278 provides a highly-integrated battery charging and power-management solution for low-power applications. The linear charger provides a wide range of charge current and charger termination voltage options to charge various Li+ batteries. Temperature monitoring and JEITA compliance settings add additional functionality and safety to the charger.

This device integrates four regulators. See Table 1. A single-inductor, multiple output (SIMO) buck-boost regulator efficiently provides three independently programmable power rails. A 50mA LDO provides ripple rejection for audio and other low-noise applications.

The device includes other features such as a programmable current sink that can be used to drive an IR-LED, 8 GPIO control pins, and an analog multiplex (AMUX) output that provides access to useful battery charging signals. A bidirectional I^2C interface allows for configuring and checking the status of the devices. An internal on/off controller provides a controlled startup sequence for the regulators and provides supervisory functionality when the devices are on. Numerous factory programmable options allow the device to be tailored for many applications, enabling faster time to market.

Support Materials

The following support materials are available for this device:

- *AN6490: MAX77278 Programmer's Guide* provides a description of all device registers, as well as software implementation advice.
- *AN6474: MAX77278 I^2C-Compatible Serial Interface Implementation Guide* provides a detailed look at the I^2C-compatible serial interface and standard read/write patterns.
- *MAX77278 SIMO Calculator* details the SIMO design procedure. See the *SIMO Available Output Current* section of the data sheet for more information.

Visit the product page at *www.maximintegrated.com/MAX77278* and/or contact Maxim for more information.

Top-Level Interconnect Simplified Diagram

Figure 1 shows the same major blocks as the *Typical Application Circuit* with an increased emphasis on the routing between each block. This diagram is intended to familiarize the user with the landscape of the device. Many of the details associated with these signals are discussed throughout the data sheet. At this stage of the data sheet, note the addition of the main bias and clock block that are not shown in the *Typical Application Circuit*. The main bias and clock block provides voltage, current, and clock references for other blocks as well as many resources for the top-level digital control.

Table 1. Regulator Summary

REGULATOR NAME	REGULATOR TOPOLOGY	MAXIMUM I_{OUT} (MA)	V_{IN} RANGE	MAX77278 V_{OUT} RANGE/ RESOLUTION
SBB0	SIMO	up to 300*	2.8 to 5.5V	2.35V to 5.5V in 50mV steps
SBB1	SIMO	up to 300*	2.8 to 5.5V	1.412V to 2.2V in 12.5mV steps
SBB2	SIMO	up to 300*	2.8 to 5.5V	0.85 to 4V in 50mV steps
LDO	PMOS LDO	up to 50*	3.733 to 5.5V	3.713 to 5.3V in 12.5mV steps

**Shared capacity with other SBBx channels. See the SIMO Available Output Current section for more information.*

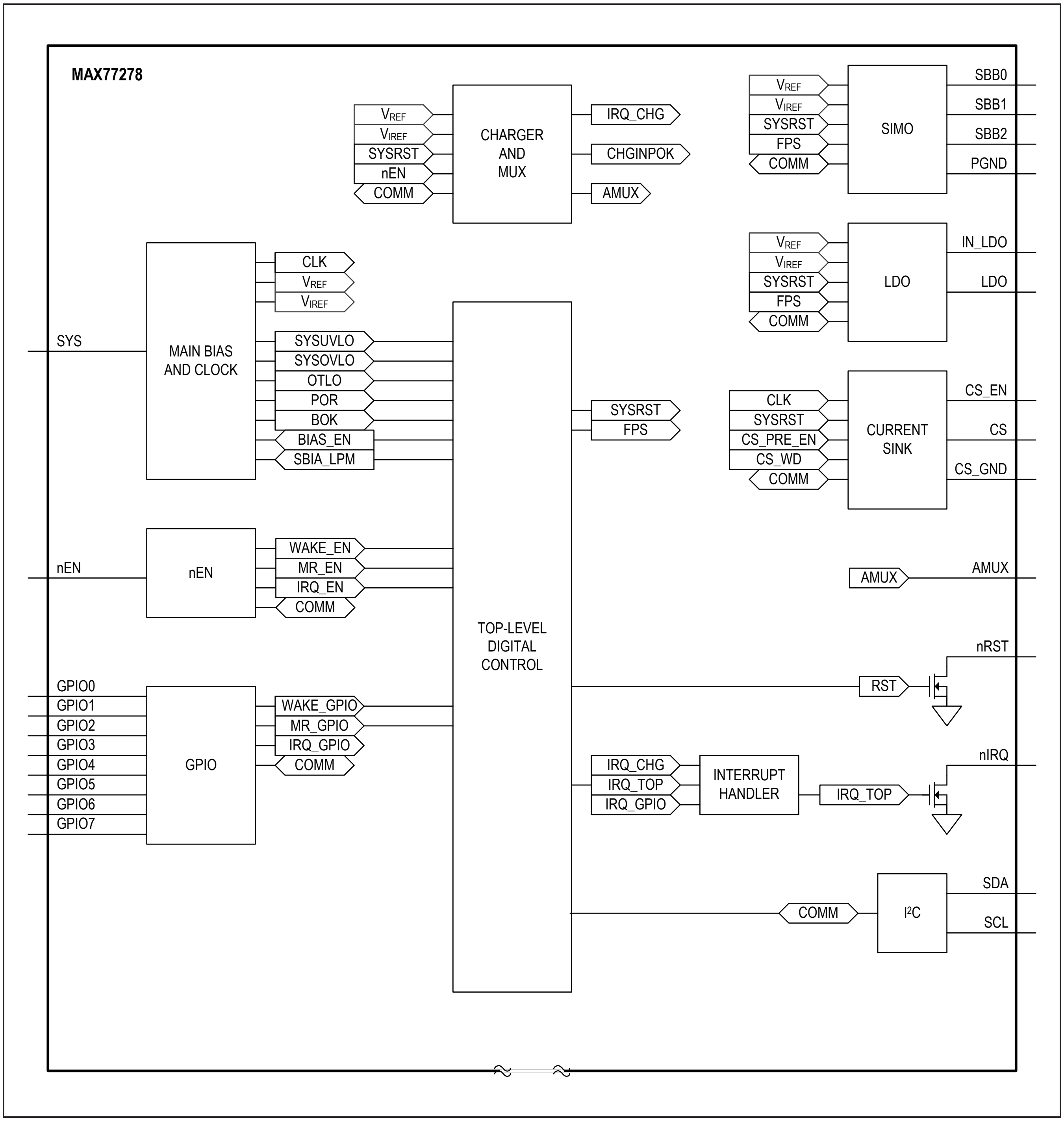


Figure 1. Top-Level Interconnect Simplified Diagram

Detailed Description—Global Resources

The global resources encompass a set of circuits that serve the entire device and ensure safe, consistent, and reliable operation.

Features and Benefits

- Voltage Monitors
  - SYS POR (power-on-reset) comparator generates a reset signal upon power-up.
  - SYS undervoltage ensures repeatable behavior when power is applied to and removed from the device.
  - SYS overvoltage monitor inhibits operation with overvoltage power sources to ensure reliability in faulty environments.
- Thermal Monitors
  - 165°C junction temperature shutdown
- Manual Reset
  - 8s/16s period (OTP programmable)
- Wake-Up Events
  - Charger insertion (with 120ms debounce)
  - nEN input assertion
  - GPIO input assertion
- Interrupt Handler
  - Interrupt output (nIRQ)
  - All interrupts are maskable
- Push-Button/Slide-Switch On-Key (nEN)
  - Configurable push-button/slide-switch functionality
  - 100µs or 30ms debounce timer interfaces directly with mechanical switches
- On/Off Controller
  - Startup/shut-down sequencing
  - Programmable sequencing delay
- nRST Digital Output

Voltage Monitors

The device monitors the system voltage (V_{SYS}) to ensure proper operation using three comparators (POR, UVLO, and OVLO). These comparators include hysteresis to prevent their outputs from toggling between states during noisy system transitions.

SYS POR Comparator

The SYS POR comparator monitors V_{SYS} and generates a power-on reset signal (POR). When V_{SYS} is below V_{POR}, the device is held in reset (SYSRST = 1). When V_{SYS} rises above V_{POR}, internal signals and on-chip memory stabilize and the device is released from reset (SYSRST = 0).

SYS Undervoltage-Lockout Comparator

The SYS undervoltage lockout (UVLO) comparator monitors V_{SYS} and generates a SYSUVLO signal when the V_{SYS} falls below UVLO threshold. The SYSUVLO signal is provided to the top-level digital controller. See Figure 4 and Table 2 for additional information regarding the UVLO comparator:

- When the device is in the STANDBY state, the UVLO comparator is disabled.
- When transitioning out of the STANDBY state, the UVLO comparator is enabled allowing the device to check for sufficient input voltage. If the device has sufficient input voltage, it can transition to the on state; if there is insufficient input voltage, the device transitions back to the STANDBY state.

SYS Overvoltage-Lockout Comparator

The device is rated for 5.5V maximum operating voltage (V_{SYS}) with an absolute maximum input voltage of 6.0V. An overvoltage lockout monitor increases the robustness of the device by inhibiting operation when the supply voltage is greater than $V_{SYSOVLO}$. See Figure 4 and Table 2 for additional information regarding the OVLO comparator:

- When the device is in the STANDBY state, the OVLO comparator is disabled.

nEN Enable Input

nEN is an active-low internally debounced digital input that typically comes from the system's on-key. The debounce time is programmable with DBEN_nEN. The primary purpose of this input is to generate a wake-up signal for the PMIC that turns on the regulators. Maskable rising/falling interrupts are available for nEN (nEN_R and nEN_F) for alternate functionality.

The nEN input can be configured to work either with a momentary push-button (nEN_MODE = 0) or a persistent slide-switch (nEN_MODE = 1). See Figure 2 for more information. In both push-button mode and slide-switch mode, the on/off controller looks for a falling edge on the nEN input to initiate a power-up sequence.

nEN Manual Reset

nEN works as a manual reset input when the on/off controller is in the on via on/off controller state. The manual reset function is useful for forcing a power-down in case the communication with the processor fails. When nEN is configured for a push-button mode and the input is asserted (nEN = low) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to standby mode. When nEN is configured for a slide-switch mode and the input is deasserted (nEN = high) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to standby mode.

A dedicated internal oscillator is used to create the 30ms (t_{DBNC_nEN}) and 16s (t_{MRST}) timers for nEN. Whenever the device is actively counting either of these times, the supply current increases by the oscillator's supply current (65µA when the battery voltage is at 3.7V). As soon as the event driving the timer goes away or is fulfilled, the oscillator automatically turns off and its supply current goes away.

nEN Dual-Functionality: Push-Button vs. Slide-Switch

The nEN digital input can be configured to work with a push-button switch or a slide-switch. The timing diagram below shows nEN's dual functionality for power-on sequencing and manual reset. The default configuration of the device is push-button mode (nEN_MODE = 0) and no additional programming is necessary. Applications that use a slide-switch on-key configuration must set nEN_MODE = 1 within t_{MRST}.

Interrupts (nIRQ)

Several status, interrupt, and interrupt mask registers monitor key information and assert the nIRQ output signal when an interrupt event has occurred. Refer to the *Programmer's Guide* for a comprehensive list of all interrupt bits and status registers.

nIRQ is an active-low, open-drain output that is typically routed to the processor's interrupt input to allow for quick notification of interrupt events. A pullup resistor is required for this signal. This pullup resistor is typically found inside the processor that interprets the interrupt signal, but a board-mounted pullup resistor is required if one is unavailable. The pullup resistor bias voltage should be less than or equal to V_{SYS}.

All interrupts are masked by default. Initialization software should unmask interrupts of interest so nIRQ can be asserted when they occur.

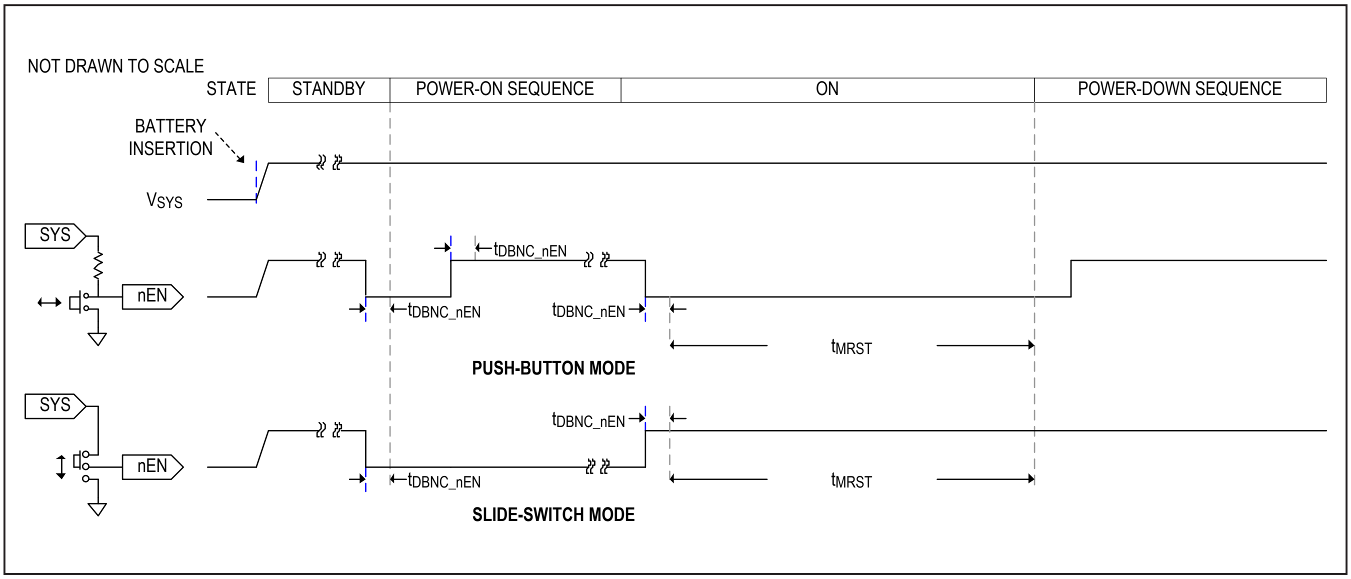


Figure 2. nEN Usage Timing Diagram

Reset Output (nRST)

nRST is an open-drain, active-low output that is typically used to hold the processor in a reset state when the device is powered down. During a power-up sequence, the nRST deasserts after the last regulator in the power-up chain is enabled (t_{RSTODD}). During a power-down sequence, the nRST output asserts before any regulator is powered down (t_{RSTOAD}). See Figure 5 for nRST timing.

A pullup resistor is required for the nRST open-drain output. This pullup resistor is typically inside the processor that is receiving the reset signal. A board-mounted pullup resistor is required if one is unavailable inside the processor. The pullup resistor bias voltage should be less than or equal to V_{SYS}.

General-Purpose Input/Output (GPIO)

Eight general-purpose input/outputs (GPIOs) are provided to increase system flexibility. See the GPIO Controller Block Diagram (Figure 3) for schematic details.

Clear DIRx to configure GPIOx as a general-purpose output (GPO). The GPO can either be in push-pull mode (DRVx = 1) or open-drain mode (DRVx = 0).

- The push-pull output mode is ideal for applications that need fast (~2ns) edges and low-power consumption.
- The open-drain mode requires an external pullup resistor (typically 10kΩ–100kΩ). Connect the external pullup resistor to a bias voltage that is less than or equal to V_{SYS}.
  - The open-drain mode can be used to communicate to different logic domains. For example, to send a signal from the GPO on a 4.2V logic domain (V_{SYS} = 4.2V) to a device on a 1.2V logic domain, connect the external pullup resistor to 1.2V.
  - The open-drain mode can be used to connect several open-drain (or open-collector) devices together on the same bus to create wired logic (wired AND logic is positive-true; wired OR logic is negative-true).
- The general-purpose input (GPI) functions are still available while the pin is configured as a GPO. In other words, the DIx (input status) bit still functions properly and does not collide with the state of the DIRx bit.

Set DIRx to disable the output drivers associated with the GPO and have the device function as a GPI. The GPI features a 10ms max debounce timer (t_{DBNC_GPI}) that can be enabled or disabled with DBEN_GPIx, and programmed to 1.25ms, 2.5ms, 5ms, or 10ms.

- Enable the debounce timer (DBEN_GPIx = 1) if the GPI is connected to a device that can bounce or chatter (like a mechanical switch).
- If the GPI is connected to a circuit with clean logic transitions and no risk of bounce, disable the debounce timer (DBEN_GPIx = 0) to eliminate unnecessary logic delays. With no debounce timer, the GPI input logic propagates to nIRQ in 10ns.

A dedicated internal oscillator is used to create the 1.25ms to 10ms (t_{DBNC_GPI}) debounce timer. Whenever the device is actively counting this time, the supply current increases by the oscillator's supply current (65µA when the battery voltage is at 3.7V). As soon as the event driving the timer goes away or is fulfilled, the oscillator automatically turns off and its supply current goes away. If GPI is connected to a signal that toggles infrequently, the oscillator supply current is inconsequential. However, if the GPI signal is periodic and greater than 1Hz, this supply current can be detrimental.

For example:

- If the GPI signal has a period of 20ms, the timer runs continuously, and the supply current increases by the full 65µA.
- If the signal has a longer period, the supply current increase by a fraction of 65µA; a period of 40ms increases the supply current by 50% of the 65µA oscillator current (20ms/40ms x 65µA = 32.5µA).

The GPI features edge detectors that feed into the top-level interrupt system of the chip. This allows software to use interrupts to service events associated with a GPI change instead of having to poll for these changes.

- If the application wants nIRQ to go low **only on a GPI rising edge**, then it should **clear** the GPI rising edge interrupt mask bit (RM_GPIOx = **0**) and **set** the GPI falling edge interrupt mask bit (FM_GPIOx = **1**).
- If the applications wants nIRQ to go low **only on a GPI falling edge**, then it should **set** the GPI rising edge interrupt mask bit (RM_GPIOx = **1**) and **clear** the GPI falling edge interrupt mask bit (FM_GPIOx = **0**).
- If the applications wants nIRQ to go low **on both GPI falling and rising edges**, then it should **clear** the GPI rising edge interrupt mask bit (RM_GPIOx = **0**) and **clear** the GPI falling edge interrupt mask bit (GFM_GPIOx = **0**).

The GPIO scan also be used as a wake-up or shutdown source. The GPIO DIRx (level-triggered) bits and the IRQ (edge-triggered) bits are internally OR'ed to wake-up the device if any GPIO is pulled low. All GPIOs that have WK_ENx set must be configured as general-purpose inputs and pulled up to V_{SYS} for any GPIO to act as a wake-up source. Set the WK_ENx bit low to remove a specific GPIO as a wake-up source. All WK_ENx bits are set high upon system reset. A system that uses the device as the master PMIC has all GPIOs set as a wake-up source by default. A system that uses the device as a slave PMIC can set the desired WK_ENx bits to configure which GPIOs should be used as a wake-up source.

The device enters shutdown if two (programmable) pins are held low for t_{MRST_GPIO}. Use MR_GPIO_INC to define which GPIOs are configured to perform the manual reset. GPIO0 and GPIO2 are configured to perform the manual reset by default.

Figure 3 shows a block diagram representation of GPIO0. All GPIO channels are identical and match the block diagram of GPIO0. The R_GPIOx and F_GPIOx interrupts are cleared by reading the INT_GPIO_R and INT_GPIO_F register respectively.

On/Off Controller

The on/off controller monitors multiple power-up (wake-up) and power-down (shutdown) conditions to enable or disable resources that are necessary for the system and its processor to move between its operating modes.

Many systems have one power-management controller and one processor and rely on the on/off controller to be the master controller. In this case, the on/off controller receives the wake-up events and enables some or all of the regulators in order to power up a processor. That processor then manages the system. To conceptualize this master operation, see Figure 4 and Table 2. A typical path through the on/off controller in master mode is:

1) Start in the no power state.
2) Apply a battery to the system and transition through path 1 and 2 to the standby state.
3) Press the system's on-key (nEN = low) or pull one of the GPIO pins low.
4) The processor boots up and drives the transition state through path 4C to the ON state (deasserting nRST).
5) The device performs its desired functions in the on through on/off controller state.
6) To enter the standby state, pull the manual reset GPIOs (GPIO0 and GPIO2 by default) low for longer than $t_{MRST\text{-}GPIO}$, pull nEN low for longer than t_{MRST}, or use the SFT_RST bits to enter the software off state.

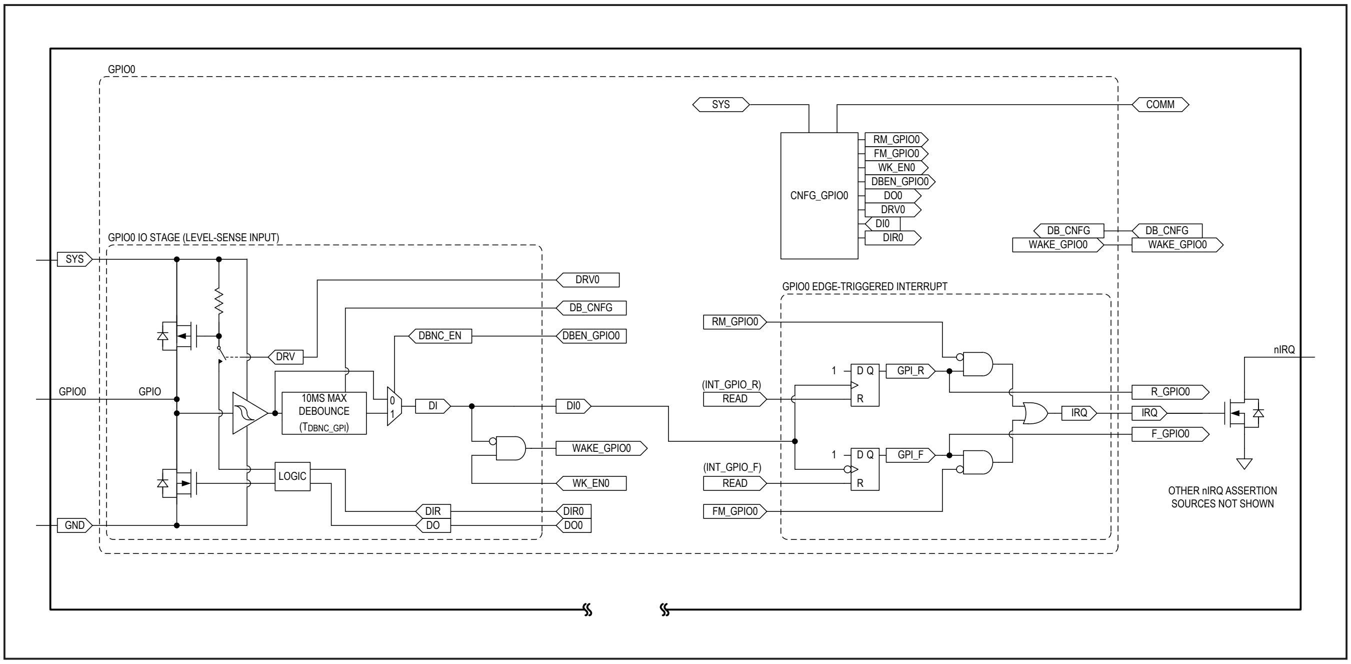


Figure 3. GPIO Controller Block Diagram

Some systems have several power-management blocks, a main processor, and sub processors. These systems can use this device as a subpower-management block for a peripheral portion of circuitry as long as there is an I^2C port available from a higher level processor. To conceptualize this slave operation, see Figure 4 and Table 2. A typical path through the on/off controller in slave mode is:

1) Start in the no power state.
2) Apply a battery to the system and transition through path 1 and 2 to the standby state.
3) When the higher level processor wants to turn on this device's resources, it enables the main bias circuits through I^2C (SBIA_EN = 1) to transition along path 2A to the on through software state.
4) The higher level processor can now control this device's resources with I^2C commands (i.e., turn on/off regulators).
5) When the higher level processor is ready to turn this device off, it turns off everything through I^2C and then disables the main bias circuits through I^2C (SBIA_EN = 0) to transition along path 2B to the standby state

Note that in this slave style of operation, the SFT_RST bits should not be used to turn the device off. The SFT_RST bits establish directives to the on/off controller itself that does not make sense in slave mode. In slave mode, since the I^2C commands enable the device's resources, they should also disable them.

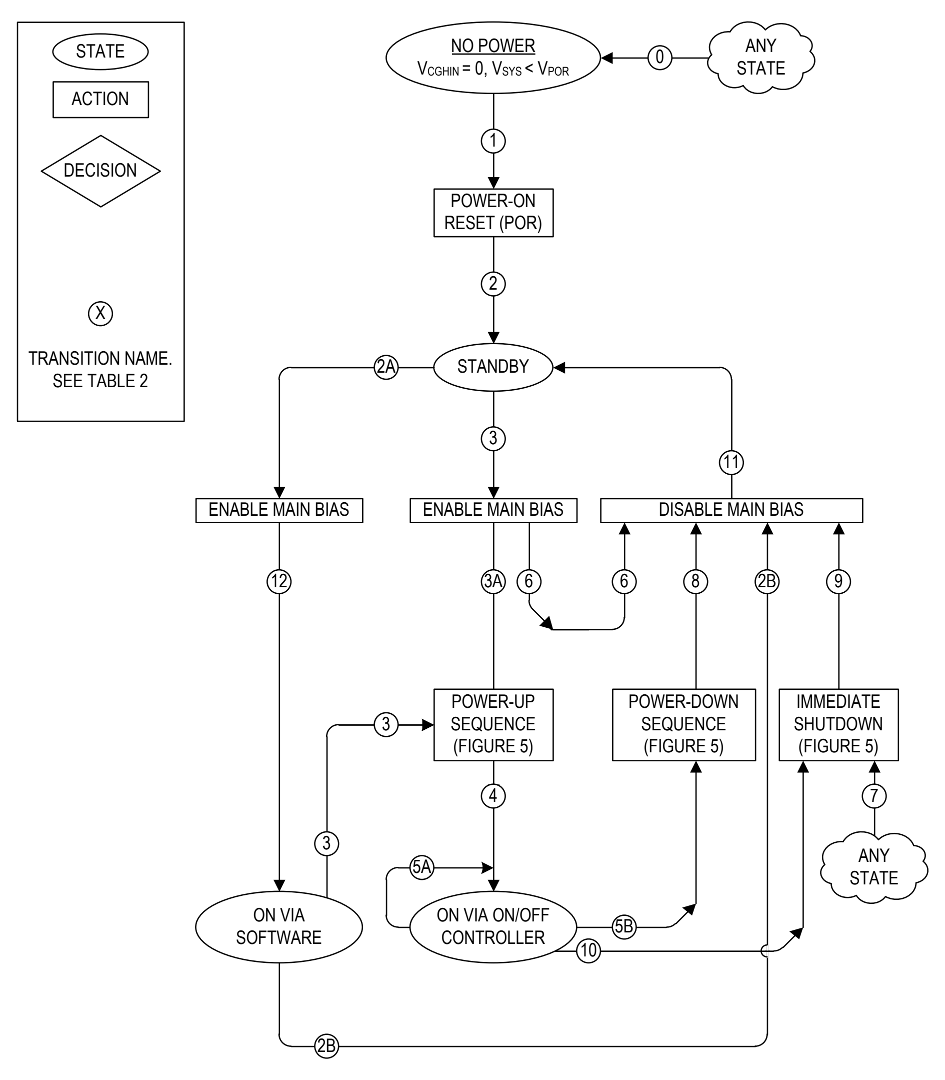


Figure 4. Top-Level On/Off Controller

Table 2. On/Off Controller Transition/State

TRANSITION/STATE	CONDITION
0	System voltage is below the POR threshold ($V_{SYS} < V_{POR}$).
1	System voltage is above the POR threshold ($V_{SYS} > V_{POR}$).
2	Internal signals and on-chip memory stabilize and the device is released from reset.
STANDBY	The device is waiting for a wake-up signal or an I^2C command to enable the main bias circuits. * This is the lowest current state of the device (I_Q ~0.3μA). * Main bias circuits are off, POR comparator is on. * I^2C is on when V_{IO} is valid. * Peripheral functions (LDO, SIMO, CS, AMUX) do not operate in this state because the main bias circuits are off. To utilize a function, enter the on through software or on through on/off controller states.
2A	Main bias circuits enabled through I^2C (SBIA_EN = 1).
2B	Main bias circuits disabled through I^2C (SBIA_EN = 0).
ON VIA SOFTWARE	The main bias circuits are enabled through software and all peripheral functions (LDO, SIMO, CS, AMUX) can be manually enabled or disabled through I^2C.
3	A wake-up signal has been received. * A debounced on-key (nEN) falling edge has been detected (WAKE_EN = 1) or * A charge source has been applied and a rising edge on CHGIN has been detected and debounced ($t_{CHGIN-DB}$ ~120ms) or * Internal wake-up flag has been set due to SFT_CRST = 1 (WKUP = 1) or *A debounced GPIO wake-up event occurred (WAKE_GPIO = 1)
3A	Main bias circuits are OK (BOK = 1).
4	Power-up sequence complete.
ON VIA ON/OFF CONTROLLER	On state. * All flexible power sequencers (FPS) are on. * The main bias circuits are enabled. * NPM is enabled (I_Q ~48μA) with all regulators enabled (no load) and the main bias circuits in normal-power mode.
5B	Software cold reset (SFT_RST[1:0] = 0b01) or Software power off (SFT_RST[1:0] = 0b10) or Manual reset occurred (MR_EN = 1 or MR_GPIO = 1). See the *nEN Manual Reset* section for more information.
6	System overtemperature lockout ($T_J > T_{OTLO}$) or System undervoltage lockout ($V_{SYS} < V_{SYSUVLO} + V_{SYSUVLO\_HYS}$) or System overvoltage lockout ($V_{SYS} > V_{SYSOVLO}$)
7	System undervoltage lockout ($V_{SYS} < V_{SYSUVLO}$) or System overvoltage lockout ($V_{SYS} > V_{SYSOVLO,}$) **Note:** The overvoltage lockout transition does not apply to the ON VIA SOFTWARE state.
8	Finished with the power-down sequence.
9	Finished with immediate shutdown.
10	System overtemperature lockout ($T_J > T_{OTLO}$).
11	Done disabling main bias.
12	Done enabling main bias.

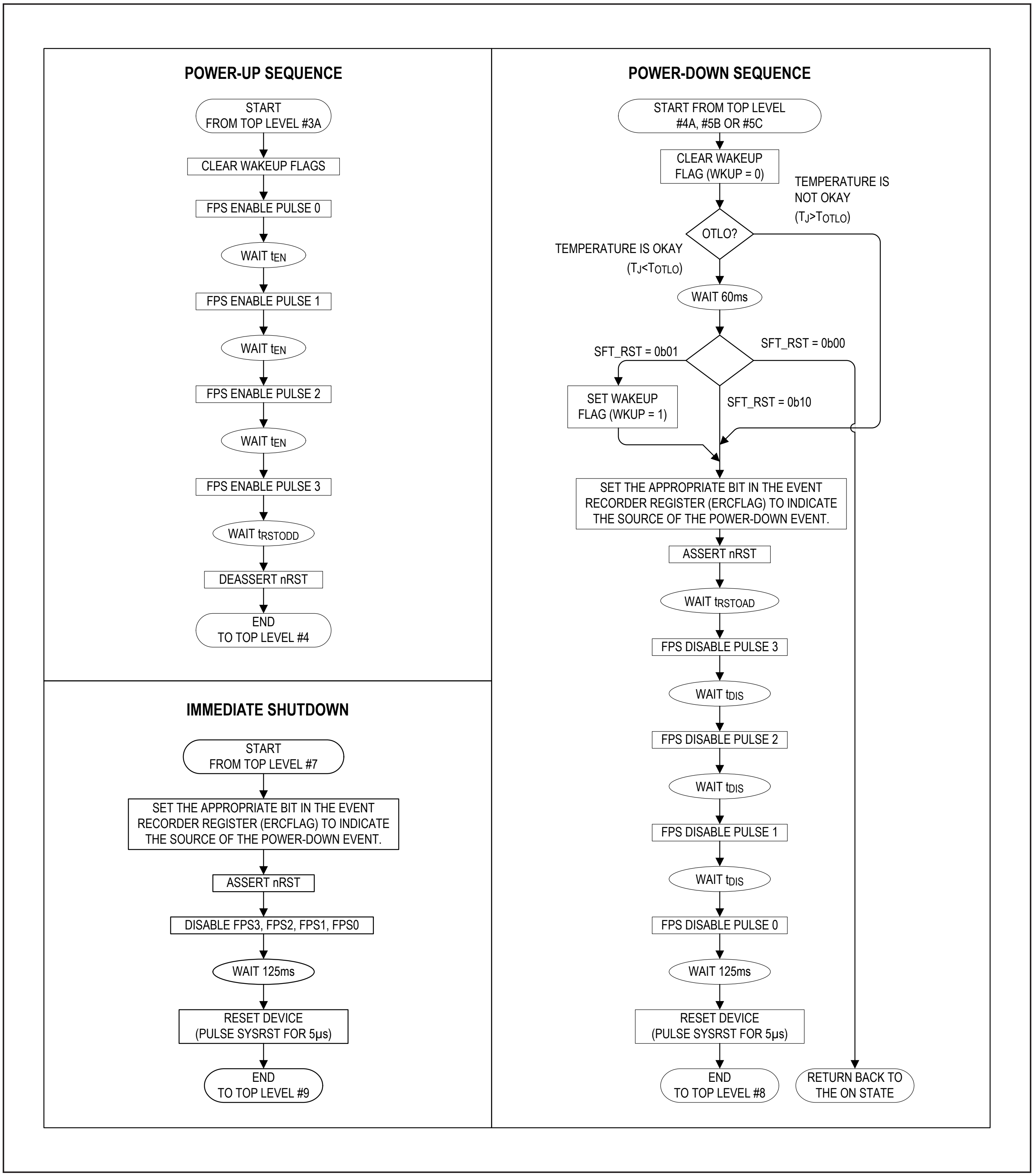


Figure 5. Power-Up/Power-Down Sequence

Flexible Power Sequencer (FPS)

The FPS allows resources to power up under hardware or software control. Additionally, each resource can power up independently or among a group of other regulators with adjustable power-up and power-down delays (sequencing). Figure 6 shows four resources powering up under the control of FPS.

The flexible sequencing structure consists of 1 master sequencing timer and 4 slave resources (SBB0, SBB1, SBB2, and LDO). When the FPS is enabled, a master timer generates four sequencing events for device power-up and power-down.

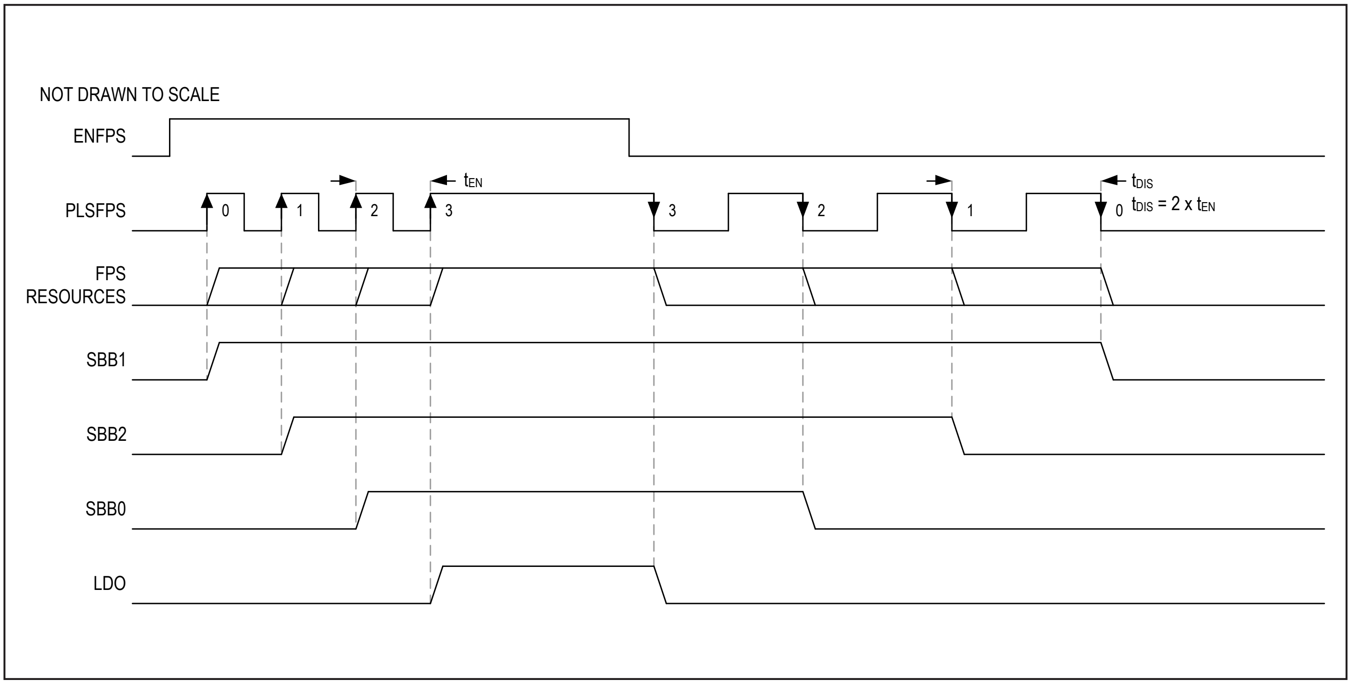
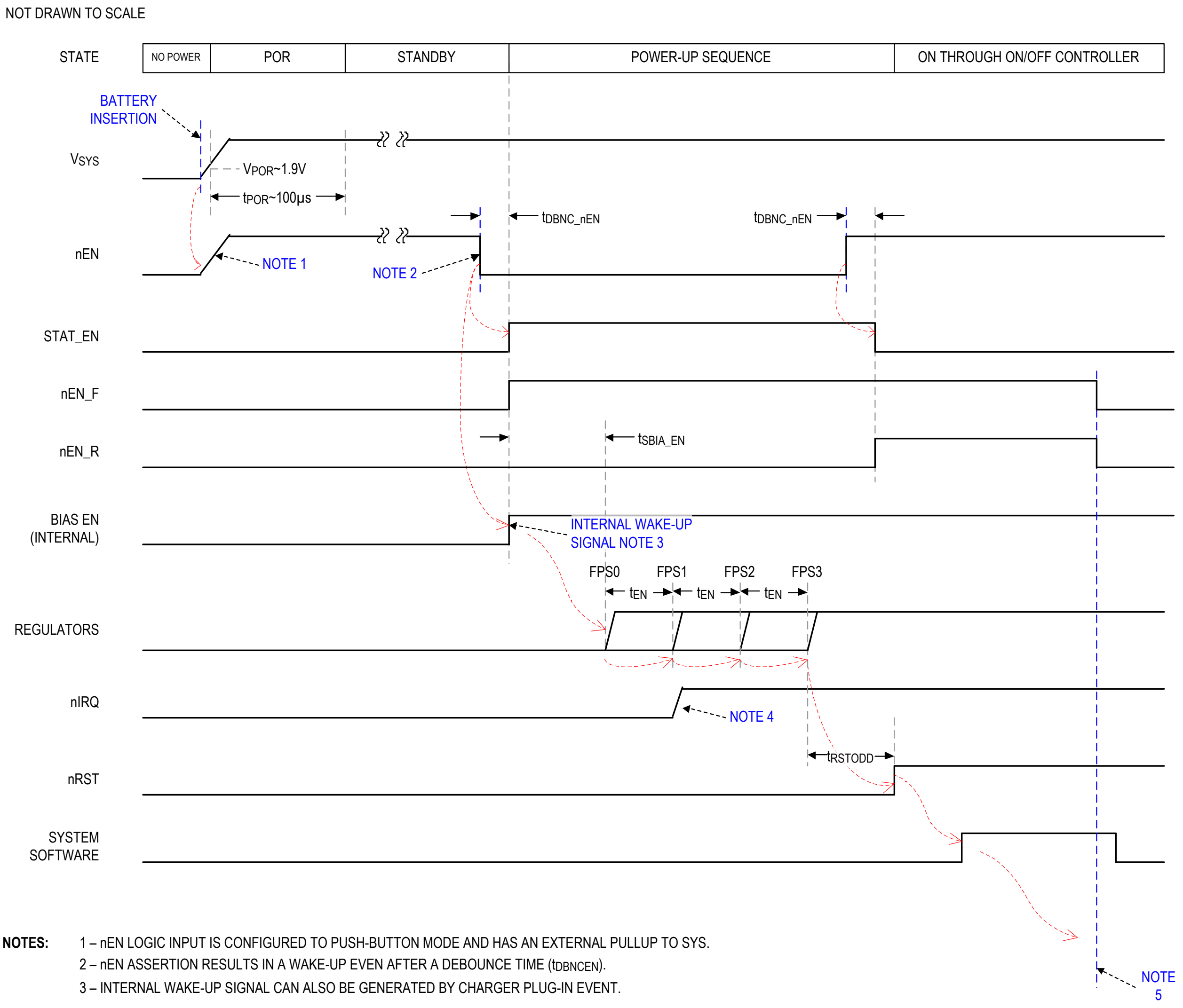


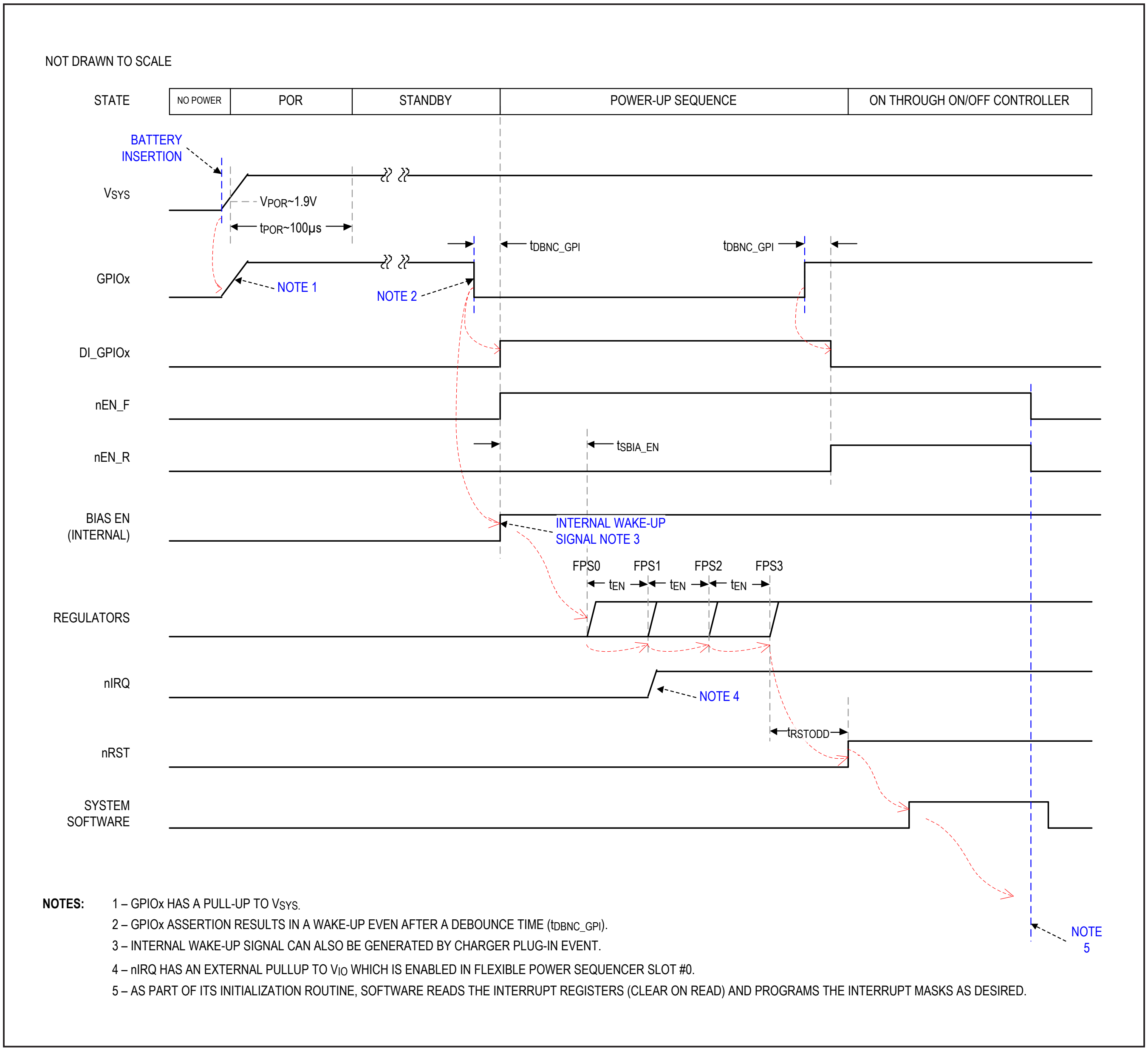
Figure 6. FPS Basic Timing Diagram



NOTES:

1 – nEN LOGIC INPUT IS CONFIGURED TO PUSH-BUTTON MODE AND HAS AN EXTERNAL PULLUP TO SYS.
2 – nEN ASSERTION RESULTS IN A WAKE-UP EVEN AFTER A DEBOUNCE TIME (t_{DBNCEN}).
3 – INTERNAL WAKE-UP SIGNAL CAN ALSO BE GENERATED BY CHARGER PLUG-IN EVENT.
4 – nIRQ HAS AN EXTERNAL PULLUP TO V_{IO} WHICH IS ENABLED IN FLEXIBLE POWER SEQUENCER SLOT #0.
5 – AS PART OF ITS INITIALIZATION ROUTINE, SOFTWARE READS THE INTERRUPT REGISTERS (CLEAR ON READ) AND PROGRAMS THE INTERRUPT MASKS AS DESIRED.

Figure 7. Startup Timing Diagram Due to nEN



NOTES:

1 – GPIOx HAS A PULL-UP TO V_{SYS}.

2 – GPIOx ASSERTION RESULTS IN A WAKE-UP EVEN AFTER A DEBOUNCE TIME (t_{DBNC_GPI}).

3 – INTERNAL WAKE-UP SIGNAL CAN ALSO BE GENERATED BY CHARGER PLUG-IN EVENT.

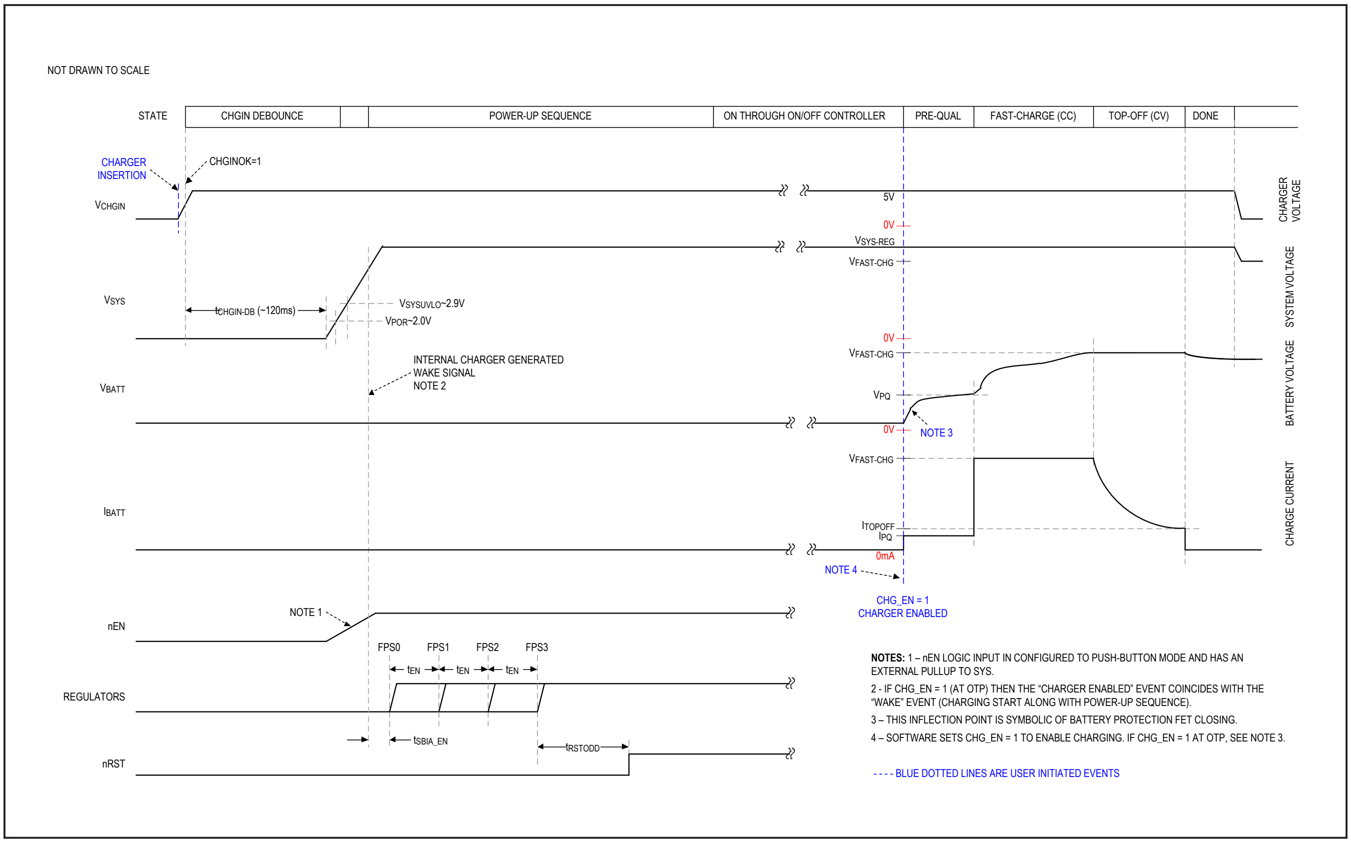
4 – nIRQ HAS AN EXTERNAL PULLUP TO V_{IO} WHICH IS ENABLED IN FLEXIBLE POWER SEQUENCER SLOT #0.

5 – AS PART OF ITS INITIALIZATION ROUTINE, SOFTWARE READS THE INTERRUPT REGISTERS (CLEAR ON READ) AND PROGRAMS THE INTERRUPT MASKS AS DESIRED.

Figure 8. Startup Timing Diagram Due to GPIO

Debounced Inputs (nEN, GPI, CHGIN)

nEN, CHGIN, and GPIO (when operating as an input) are debounced on both rising and falling edges to reject undesired transitions. The input must be at a stable logic level for the entire debounce period for the output to change its logic state. Figure 9 shows an example timing diagram for the nEN debounce.



NOTES: 1 – nEN LOGIC INPUT IN CONFIGURED TO PUSH-BUTTON MODE AND HAS AN EXTERNAL PULLUP TO SYS.

2 - IF CHG_EN = 1 (AT OTP) THEN THE “CHARGER ENABLED” EVENT COINCIDES WITH THE “WAKE” EVENT (CHARGING START ALONG WITH POWER-UP SEQUENCE).

3 – THIS INFLECTION POINT IS SYMBOLIC OF BATTERY PROTECTION FET CLOSING.

4 – SOFTWARE SETS CHG_EN = 1 TO ENABLE CHARGING. IF CHG_EN = 1 AT OTP, SEE NOTE 3.

Figure 9. Startup Timing Diagram Due to Charge Source Insertion

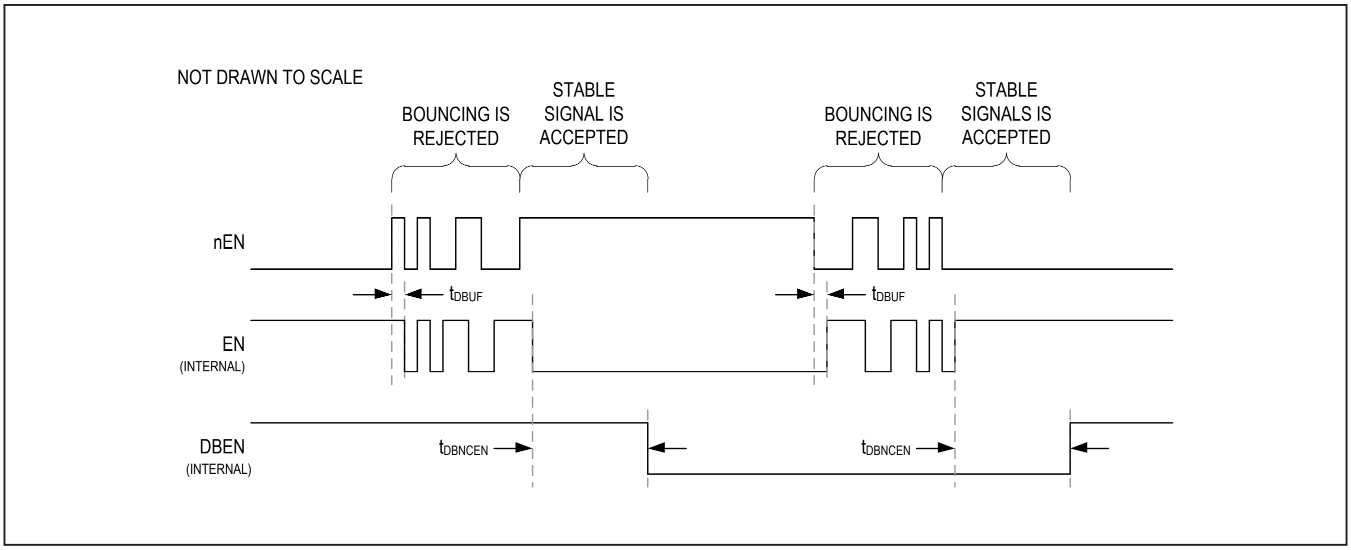


Figure 10. Debounced Inputs

Detailed Description—Smart Power Selector Charger

The linear Li+ charger features Maxim's Smart Power Selector. This allows separate input current limit and battery charge current settings. Batteries charge faster under the supervision of the Smart Power Selector because charge current is independently regulated and not shared with variable system loads. See the *Smart Power Selector* section for more information.

The programmable constant-current charge rate (7.5mA to 300mA) supports a wide range of battery capacities. The programmable input current limit (0mA to 475mA) supports a range of charge sources, including USB. The charger's programmable battery regulation voltage range (3.6V–4.6V) supports a wide variety of cell chemistries. Small battery capacities are supported; the charger accurately terminates charging by detecting battery currents as low as 0.375mA.

Additionally, the robust charger input withstands overvoltages up to 28V. To enhance charger safety, an NTC thermistor provides temperature monitoring in accordance with the JEITA recommendations. See the *Detailed Description—Adjustable Thermistor Temperature Monitors* section for more information.

Features

- 7.25V Maximum Operating Input Voltage with 28V Input Standoff
- 7.5mA to 300mA Programmable Fast-Charge Current
- Programmable Termination Current from 0.375mA to 45mA
- Programmable Battery Regulation Voltage from 3.6V to 4.6V
- < 1µA Battery-Only Supply Current
- Instant-On Functionality
- Analog Multiplexer Enables Power Monitoring
- JEITA Battery Temperature Monitor Adjusts Current and Battery Regulation Voltage for Safe Charging
- Programmable Die Temperature Regulation

Charger Symbol Reference Guide

Table 3 lists the names and functions of charger-specific signals and if they can be programmed through I^{2}C. Consult the *Electrical Characteristics—Smart Power Selector Charger* table and the *Programmer's Guide* for more information.

Figure 12 indicates the high-level functions of each control circuit within the linear charger.

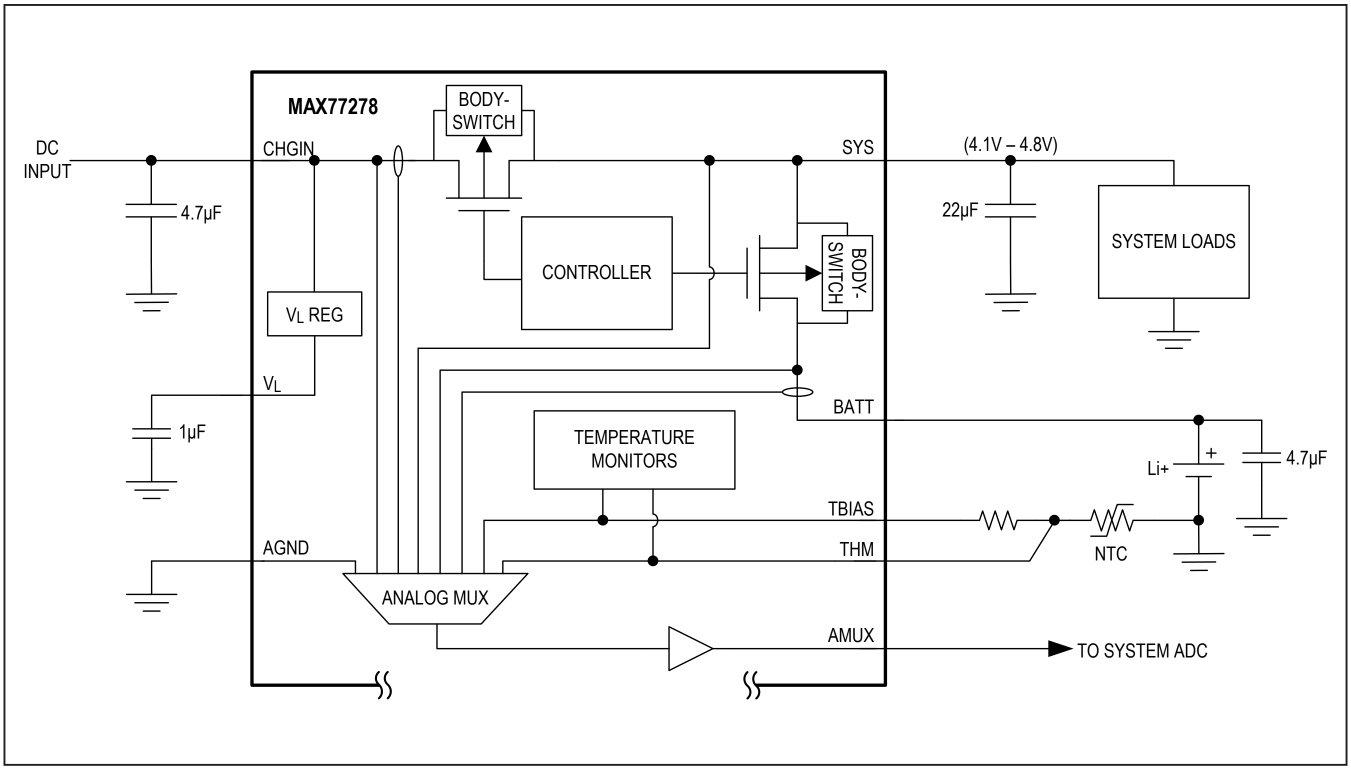


Figure 11. Linear Charger Simplified Block Diagram

Table 3. Charger Quick Symbol Reference Guide

SYMBOL	NAME	I^2C PROGRAMMABLE?
V_{CHGIN_OVP}	CHGIN overvoltage threshold	No
V_{CHGIN_UVLO}	CHGIN undervoltage-lockout threshold	No
$V_{CHGIN-MIN}$	Minimum CHGIN voltage regulation setpoint	Yes, through VCHGIN_MIN[2:0]
$I_{CHGIN-LIM}$	CHGIN input current limit	Yes, through ICHGIN_LIM[2:0]
$V_{SYS-REG}$	SYS voltage regulation target	Yes, through VSYS_REG[4:0]
$V_{SYS-MIN}$	Minimum SYS voltage regulation setpoint	No, tracks $V_{SYS-REG}$
$V_{FAST-CHG}$	Fast-charge constant-voltage level	Yes, through CHG_CV[5:0]
$I_{FAST-CHG}$	Fast-charge constant-current level	Yes, through CHG_CC[5:0]
I_{PQ}	Prequalification current level	Yes, through I_PQ
V_{PQ}	Prequalification voltage threshold	Yes, through CHG_PQ[2:0]
I_{TERM}	Termination current level	Yes, through I_TERM[1:0]
T_{J-REG}	Die temperature regulation setpoint	Yes, through TJ_REG[2:0]
t_{PQ}	Prequalification safety timer	No
t_{FC}	Fast-charge safety timer	Yes, through T_FAST_CHG[1:0]
t_{TO}	Top-off timer	Yes, through T_TOPOFF[2:0]

Smart Power Selector

The Smart Power Selector seamlessly distributes power from the input (CHGIN) to the battery (BATT) and the system (SYS). The Smart Power Selector basic functions are:

- When the system load current is less than the input current limit, the battery is charged with residual power from the input.
- When a valid input source is connected, the system regulates to $V_{SYS-REG}$ to power system loads regardless of the battery's voltage (instant on).
- When the system load current exceeds the input current limit, the battery provides additional current to the system (supplement mode).
- When the battery is finished charging and an input source is present to power the system, the battery remains disconnected from the system.
- When the battery is connected and there is no input power, the system is powered from the battery.

Input Current Limiter

The input current limiter limits CHGIN current so as not to exceed $I_{CHGIN-LIM}$ (programmed by ICHGIN_LIM[2:0]). A maskable interrupt (CHGIN_CTRL_I) is available to signal when the input current limit engages. The state of this loop is reflected by the ICHGIN_LIM_STAT bit.

The input circuit is capable of standing off 28V from ground. CHGIN suspends power delivery to the system and battery when V_{CHGIN} exceeds V_{CHGIN_OVP} (7.5V, typ). The input circuit also suspends when V_{CHGIN} falls below V_{CHGIN_UVLO} minus 500mV of hysteresis (3.5V, typ). While in OVP or UVLO, the charger remains off, and the battery provides power to the system.

When an valid charge source is connected to CHGIN, SYS begins delivering power to the system after a 120ms debounce timer ($t_{CHGIN-DB}$).

A maskable interrupt (CHGIN_I) signals changes in the state of CHGIN's voltage quality. The state of CHGIN is reflected by CHGIN_DTLS[1:0].

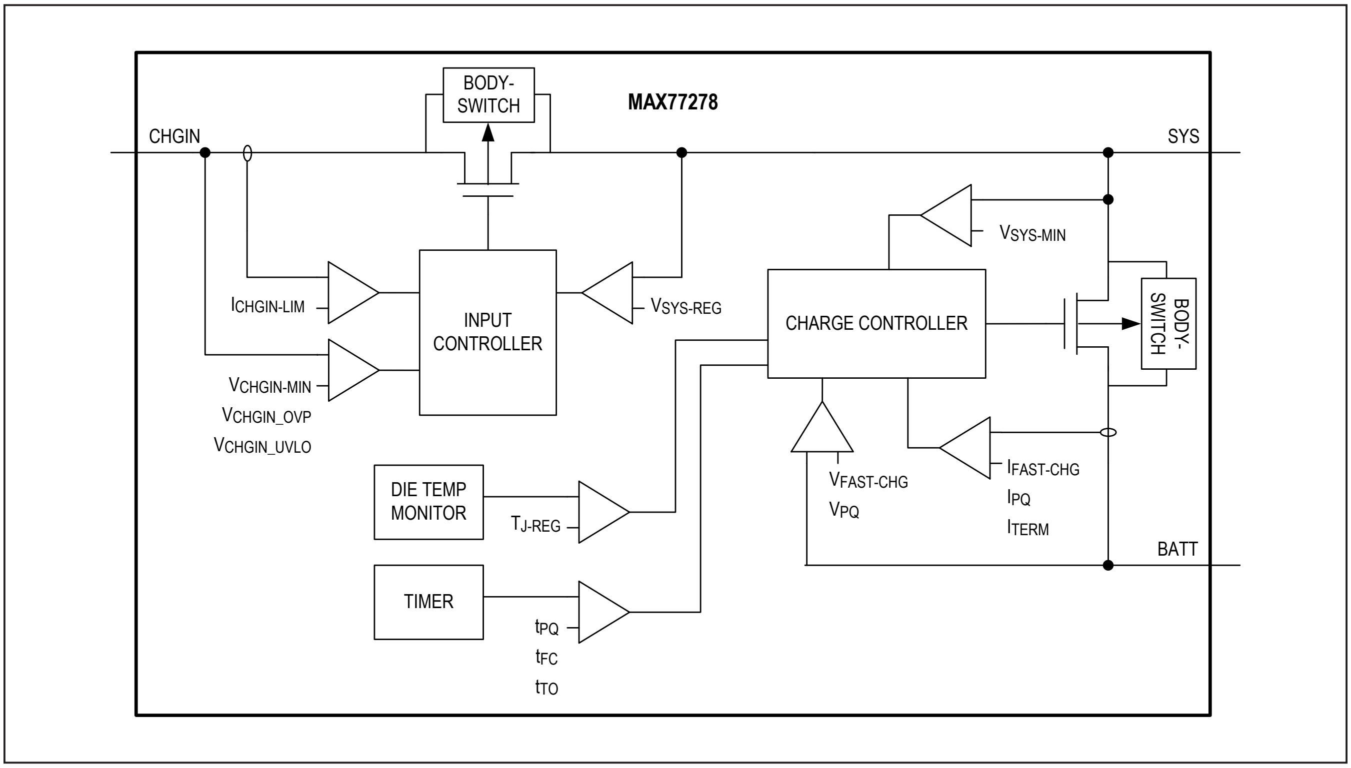


Figure 12. Charger Simplified Control Loops

Minimum Input Voltage Regulation

In the event of a poor-quality charge source, the minimum input voltage regulation loop works to reduce input current if V_{CHGIN} falls below $V_{CHGIN-MIN}$ (programmed by VCHGIN_MIN[2:0]). This is important because many commonly used charge adapters feature foldback protection mechanisms where the adapter completely shuts off if its output drops too low. The minimum input voltage regulation loop also prevents V_{CHGIN} from dropping below V_{CHGIN_UVLO} if the cable between the charge source and the charger's input is long or highly resistive.

The input voltage regulation loop improves performance with current limited adapters. If the charger’s input current limit is programmed above the current limit of the given adapter, the input voltage loop allows the input to regulate at the current limit of the adapter. The input voltage regulation loop also allows the charger to perform well with adapters that have poor transient load response times.

A maskable interrupt (CHGIN_CTRL_I) signals when the minimum input voltage regulation loop engages. The state of this loop is reflected by VCHGIN_MIN_STAT.

Minimum System Voltage Regulation

The minimum system voltage regulation loop ensures that the system rail remains close to the programmed SYS regulation voltage ($V_{SYS-REG}$) regardless of system loading. The loop engages when the combined battery charge current and system load current causes the CHGIN input to current limit at $I_{CHGIN-LIM}$. When this happens, the minimum system voltage loop reduces charge current in an attempt to keep the input out of current limit, thereby keeping the system voltage above $V_{SYS-MIN}$ ($V_{SYS-REG}$ - 100mV, typ). If this loop reduces battery current to 0 and the system is in need of more current than the input can provide, then the Smart Power Selector overrides the minimum system voltage regulation loop and allows SYS to collapse to BATT for the battery to provide supplement current to the system. The Smart Power Selector automatically reenables the minimum system voltage loop when the supplement event has ended.

A maskable interrupt (SYS_CTRL_I) asserts to signal a change in VSYS_MIN_STAT. This status bit asserts when the minimum system voltage regulation loop is active.

Die Temperature Regulation

In case the die temperature exceeds T_{J-REG} (programmed by TJ_REG[2:0]) the charger attempts to limit the temperature increase by reducing battery charge current. The TJ_REG_STAT bit asserts whenever charge current is reduced due to this loop. The charger's current sourcing capability to SYS remains unaffected when TJ_REG_STAT is high. A maskable interrupt (TJ_REG_I) asserts to signal a change in TJ_REG_STAT. It is advisable that the TJ_REG_I interrupt be used to signal the system processor to reduce loads on SYS to reduce total system temperature.

USB Suspend Mode

The USB Suspend Mode bit, USBS, controls the MOSFET between CHGIN and SYS. USBS is set to 0 by default. When USBS is 0, the system is powered from CHGIN any time a charger is present on the input. Set USBS to 1 to open the MOSFET between CHGIN and SYS. This prevents the system from drawing current from CHGIN if a charger is present and powers the system from the battery instead. USBS is reset when voltage on CHGIN is removed.

Charger State Machine

The battery charger follows a strict state-to-state progression to ensure that a battery is charged safely. The status bitfield, CHG_DTLS[3:0], reflects the charger's current operational state. A maskable interrupt (CHG_I) is available to signal a change in CHG_DTLS[3:0].

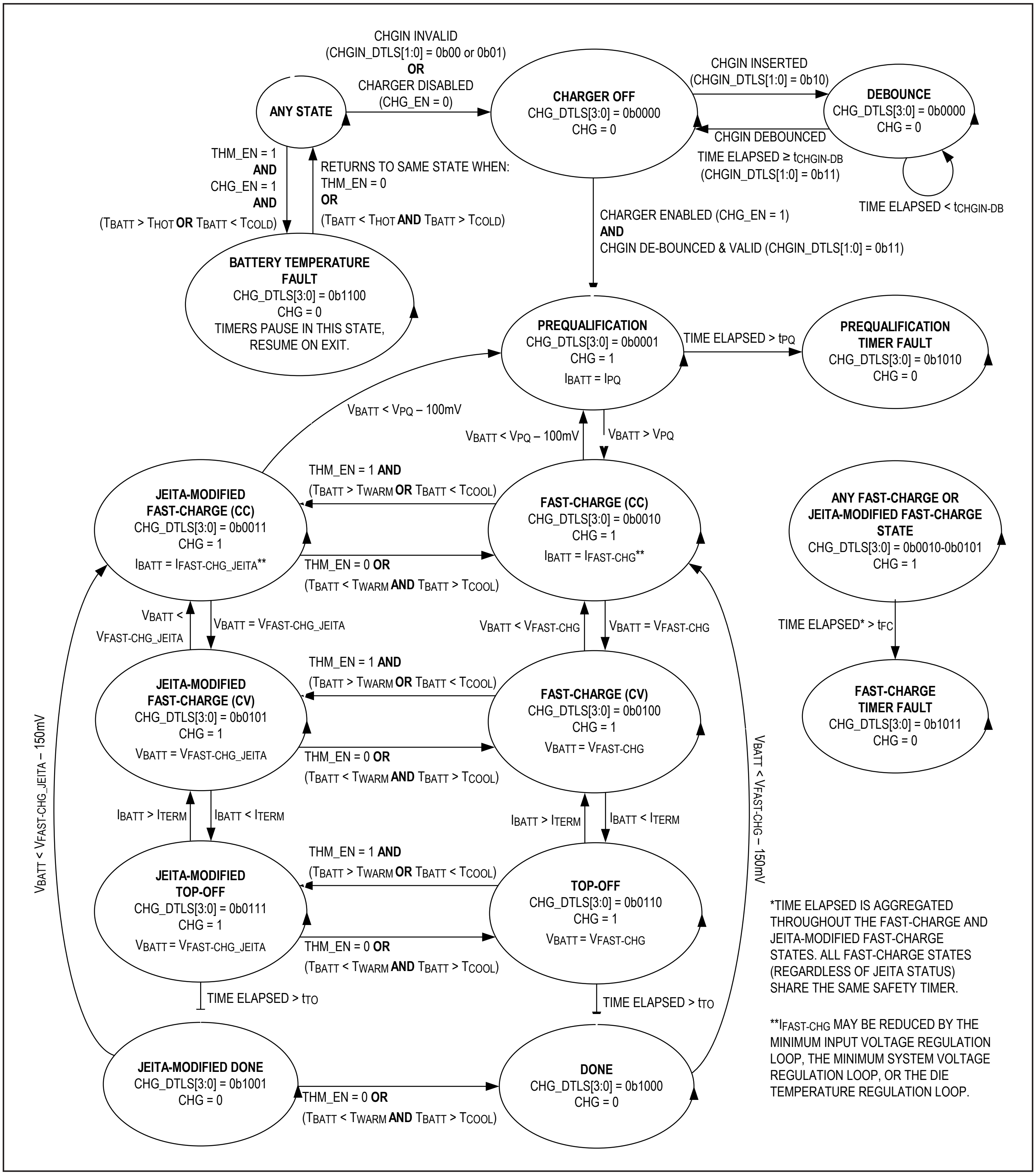
Charger Off State

The charger is off when CHGIN is invalid, the charger is disabled, or the battery is fresh.

CHGIN is invalid when the CHGIN input is invalid ($V_{CHGIN} < V_{CHGIN\_UVLO}$ or $V_{CHGIN} > V_{CHGIN\_OVP}$). While CHGIN is invalid, the battery is connected to the system. CHGIN voltage quality can be separately monitored by the CHGIN_DTLS[1:0] status bitfield. Refer to the *Programmer’s Guide* for details.

The charger is disabled when the charger enable bit is 0 (CHG_EN = 0). The battery is connected or disconnected to the system depending on the validity of V_{CHGIN} while CHG_EN = 0. See the *Smart Power Selector* section.

The battery is fresh when CHGIN is valid and the charger is enabled (CHG_EN = 1) and the battery is not low by $V_{RESTART}$ ($V_{BATT} > V_{FAST-CHG} - V_{RESTART}$). The battery is disconnected from the system and not charged while the battery is fresh. The charger state machine exits this state and begins charging when the battery becomes low by $V_{RESTART}$ (150mV, typ). This condition is functionally similar to done state. See *Done State* section.



*TIME ELAPSED IS AGGREGATED THROUGHOUT THE FAST-CHARGE AND JEITA-MODIFIED FAST-CHARGE STATES. ALL FAST-CHARGE STATES (REGARDLESS OF JEITA STATUS) SHARE THE SAME SAFETY TIMER.

**$I_{FAST-CHG}$ MAY BE REDUCED BY THE MINIMUM INPUT VOLTAGE REGULATION LOOP, THE MINIMUM SYSTEM VOLTAGE REGULATION LOOP, OR THE DIE TEMPERATURE REGULATION LOOP.

Figure 13. Charger State Diagram

Prequalification State

The prequalification state is intended to assess a low-voltage battery's health by charging at a reduced rate. If the battery voltage is less than the V_{PQ} threshold, the charger is automatically in prequalification. If the cell voltage does not exceed V_{PQ} in 30 minutes (t_{PQ}), the charger faults. The prequalification charge rate is a percentage of $I_{FAST-CHG}$ and is programmable with I_PQ. The prequalification voltage threshold (V_{PQ}) is programmable through CHG_PQ[2:0].

Fast-Charge States

When the battery voltage is above V_{PQ}, the charger transitions to the fast-charge (CC) state. In this state, the charger delivers a constant current ($I_{FAST-CHG}$) to the cell. The constant-current level is programmable from 7.5mA to 300mA by CHG_CC[5:0].

When the cell voltage reaches $V_{FAST-CHG}$, the charger state machine transitions to fast-charge (CV). $V_{FAST-CHG}$ is programmable with CHG_CV[5:0] from 3.6V to 4.6V. The charger holds the battery's voltage constant at $V_{FAST-CHG}$ while in the fast-charge (CV) state. As the battery approaches full, the current accepted by the battery reduces. When the charger detects that battery charge current has fallen below I_{TERM}, the charger state machine enters the top-off state.

A fast-charge safety timer starts when the state machine enters fast-charge (CC) or JEITA-modified fast-charge (CC) from a non-fast-charge state. The timer continues to run through all fast-charge states regardless of JEITA status. The timer length (t_{FC}) is programmable from 3 hours to 7 hours in 2 hour increments with T_FAST_CHG[1:0]. If it is desired to charge without a safety timer, program T_FAST_CHG[1:0] with 0b00 to disable the feature. If the timer expires before the fast-charge states are exited, the charger faults. See the *Fast-Charge Timer Fault State* section for more information.

If the charge current falls below 20% of the programmed value during fast-charge (CC), the safety timer pauses. The timer also pauses for the duration of supplement mode events. The TIME_SUS bit indicates the status of the fast-charge safety timer. Refer to the *Programmer's Guide* for more details.

Top-Off State

Top-off state is entered when the battery charge current falls below I_{TERM} during the fast-charge (CV) state. I_{TERM} is a percentage of $I_{FAST-CHG}$ and is programmable through I_TERM[1:0]. While in the top-off state, the battery charger continues to hold the battery's voltage at $V_{FAST-CHG}$. A programmable top-off timer starts when the charger state machine enters the top-off state. When the timer expires, the charger enters the done state. The top-off timer value (t_{TO}) is programmable from 0 minutes to 35 minutes with T_TOPOFF[2:0]. If it is desired to stop charging as soon as battery current falls below I_{TERM}, program t_{TO} to 0 minutes.

Done State

The charger enters the done state when the top-off timer expires. The battery remains disconnected from the system during done. The charger restarts if the battery voltage falls more than $V_{RESTART}$ (150mV, typ) below the programmed $V_{FAST-CHG}$ value.

Prequalification Timer Fault State

The prequalification timer fault state is entered when the battery's voltage fails to rise above V_{PQ} in t_{TO} (30 minutes, typ) from when the prequalification state was first entered. If a battery is too deeply discharged, damaged, or internally shorted, the prequalification timer fault state can occur. During the timer fault state, the charger stops delivering current to the battery and the battery remains disconnected from the system. To exit the prequalification timer fault state, toggle the charger enable (CHG_EN) bit or unplug and replug the external voltage source connected to CHGIN.

Fast-Charge Timer Fault State

The charger enters the fast-charge timer fault state if the fast-charge safety timer expires. While in this state, the charger stops delivering current to the battery and the battery remains disconnected from the system. To exit the fast-charge timer fault state, toggle the charger enable bit (CHG_EN) or unplug and replug the external voltage source connected to CHGIN.

Battery Temperature Fault State

If the thermistor monitoring circuit reports that the battery is either too hot or too cold to charge (as programmed by THM_HOT[1:0] and THM_COLD[1:0]), the state machine enters the battery temperature fault state. While in this state, the charger stops delivering current to the battery and the battery remains disconnected from the system. This state can only be entered if the thermistor is enabled (THM_EN = 1). Battery temperature fault state has priority over any other fault state, and can be exited when the thermistor is disabled (THM_EN = 0) or when the battery returns to an acceptable temperature. When this fault state is exited, the state machine returns to the last state it was in before battery temperature fault state was entered.

All active charger timers (fast-charge safety timer, prequalification timer, or top-off timer) are paused in this state. Active timers resume when the state is exited.

The THM_DTLS[2:0] bitfield reports battery temperature status. See the *Detailed Description—Adjustable Thermistor Temperature Monitors* section and refer to the *Programmer's Guide* for more information.

JEITA-Modified States

If the thermistor is enabled (THM_EN = 1), then the charger state machine is allowed to enter the JEITA-modified states. These states are entered if the charger's temperature monitors indicate that the battery temperature is either warm (greater than T_{WARM}) or cool (lesser than T_{COOL}). See the *Detailed Description—Adjustable Thermistor Temperature Monitors* section for more information about setting the temperature thresholds.

The charger's current and voltage parameters change from $I_{FAST\text{-}CHG}$ and $V_{FAST\text{-}CHG}$ to $I_{FAST\text{-}CHG\_JEITA}$ and $V_{FAST\text{-}CHG\_JEITA}$ while in the JEITA-modified states. The JEITA modified parameters can be independently set to lower voltage and current values so that the battery can charge safely over a wide range of ambient temperatures.

If the battery temperature returns to normal, or the thermistor is disabled (THM_EN = 0), the charger exits the JEITA-modified states.

Typical Charge Profile

A typical battery charge profile (and state progression) is illustrated in Figure 14.

Applications Information

Configuring a Valid System Voltage

The Smart Power Selector begins to regulate SYS to $V_{SYS\text{-}REG}$ when CHGIN is connected to a valid source. To ensure the charger's accuracy specified in the *Electrical Characteristics* table, the system voltage must always be programmed at least 200mV above the charger's constant-voltage level ($V_{FAST\text{-}CHG}$). If this condition is not met, then the charger's internal configuration logic forces $V_{FAST\text{-}CHG}$ to reduce to satisfy the 200mV requirement. If this happens, the charger asserts the SYS_CNFG_I interrupt to alert the user that a configuration error has been made and that the bits in CHG_CV[5:0] have changed to reduce $V_{FAST\text{-}CHG}$.

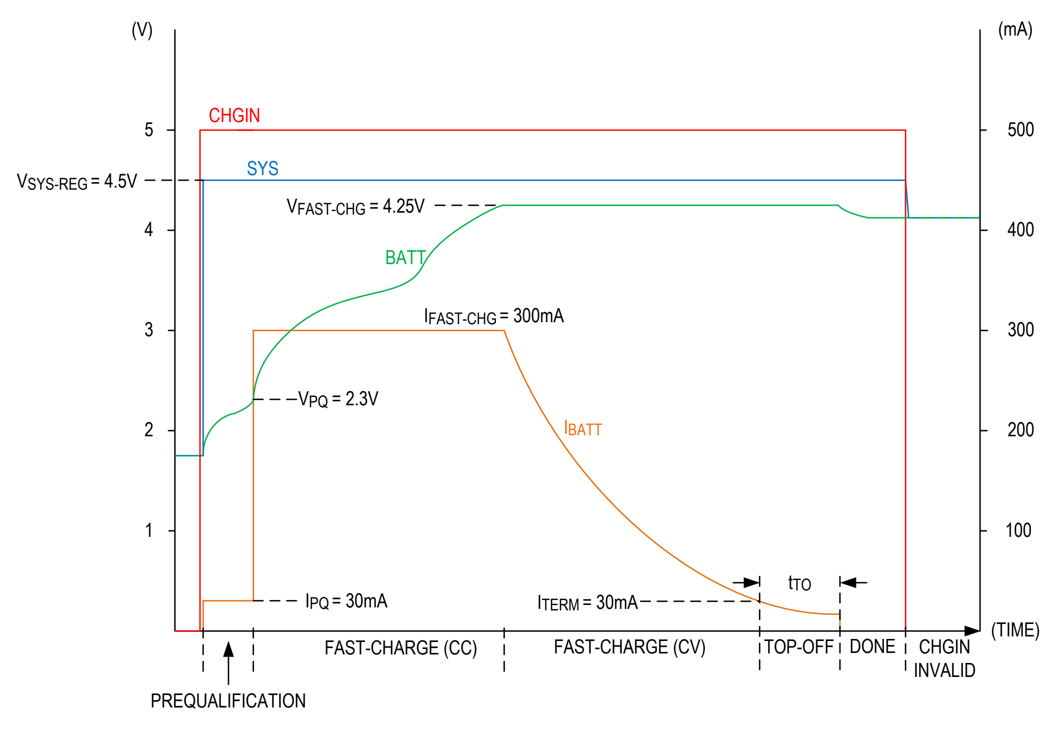


Figure 14. Example Battery Charge Profile

CHGIN/SYS/BATT Capacitor Selection

Bypass CHGIN to GND with a 4.7μF ceramic capacitor to minimize inductive kick caused by long cables between the DC charge source and the device. Larger values increase decoupling for the linear charger, but increase inrush current from the DC charge source when the device is first connected to a source through a cable/plug. If the DC charging source is an upstream USB device, limit the maximum CHGIN input capacitance based on the appropriate USB specification (i.e., typically no more than 10μF).

Bypass SYS to GND with a 22μF ceramic capacitor. This capacitor is needed to ensure stability of SYS while it is being regulated from CHGIN. Since SYS must be connected to IN_SBB, then one capacitor can be used to bypass this node as long as it is physically close to the device. Larger values of SYS capacitance increase decoupling for all SYS loads. The effective value of the SYS capacitor must be greater than 4μF and no more than 100μF.

Bypass BATT to GND with a 4.7μF ceramic capacitor. This capacitor is required to ensure stability of the BATT voltage regulation loop. The effective value of the BATT capacitor must be greater than 1μF.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

Detailed Description—Adjustable Thermistor Temperature Monitors

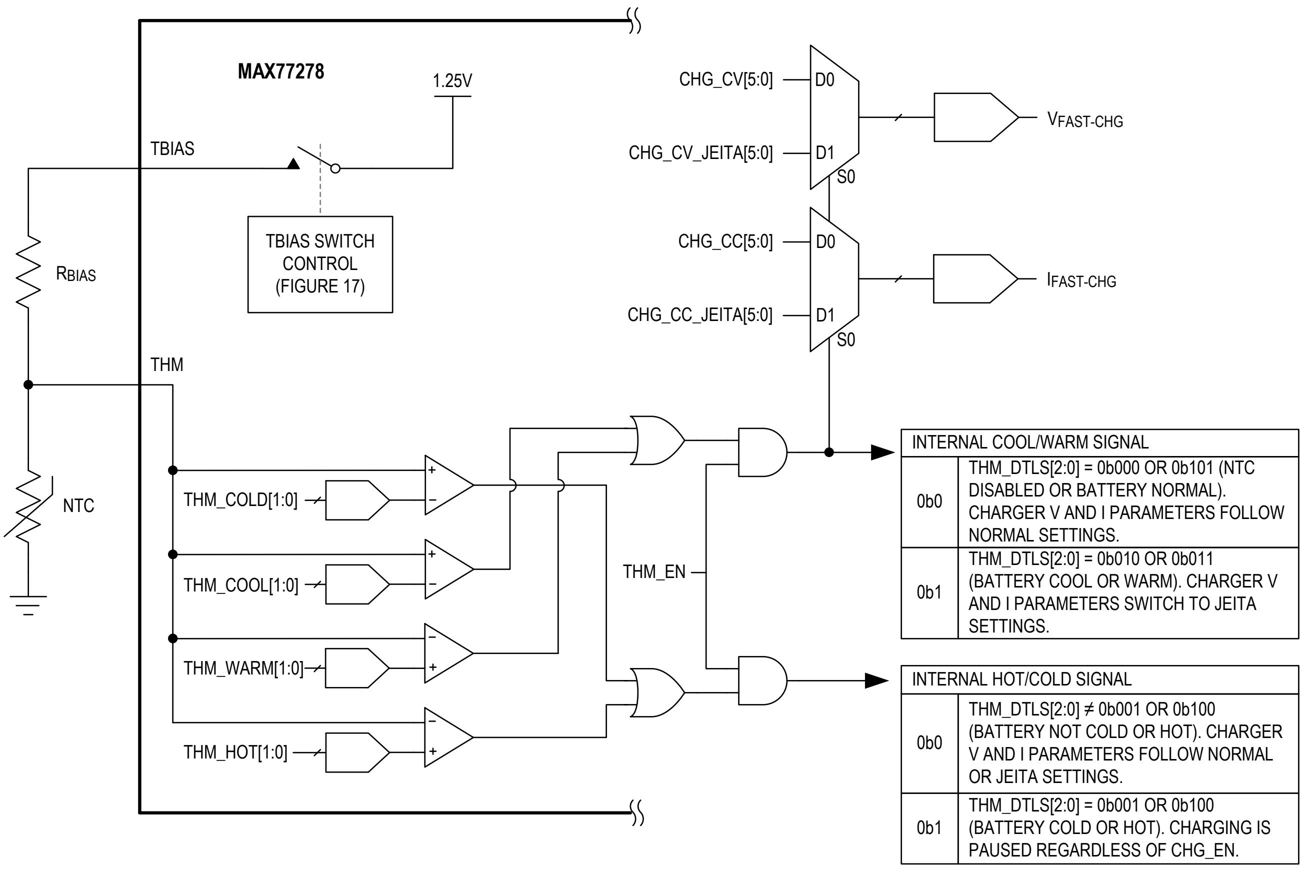
The optional use of a negative temperature coefficient (NTC) thermistor (thermally coupled to the battery) enables the charger to operate safely over the JEITA temperature range. When the thermistor is enabled (THM_EN = 1), the charger continuously monitors the voltage at the THM pin in order to sense the temperature of the battery being charged.

See Figure 15 for a visual example of the following:

- If the battery temperature is higher than T_{COOL} and lower than T_{WARM}, the battery charges normally with the normal values for $V_{FAST-CHG}$ and $I_{FAST-CHG}$. The charger state machine does not enter JEITA-modified states while the battery temperature is normal.
- If the battery temperature is either above T_{WARM} but below T_{HOT}, or below T_{COOL} but above T_{COLD}, the battery charges with the JEITA-modified voltage and current values. These modified values, $V_{FAST-CHG\_JEITA}$ and $I_{FAST-CHG\_JEITA}$, are programmable through CHG_CV_JEITA[5:0] and CHG_CC_JEITA[5:0], respectively. These values are independently programmable from the nonmodified $V_{FAST-CHG}$ and $I_{FAST-CHG}$ values and can even be programmed to the same values if an automatic response to a warm or cool battery is not desired. The charger state machine enters JEITA-modified states while the battery temperature is outside of normal.
- If the battery temperature is either above T_{HOT} or below T_{COLD}, the charger follows the JEITA recommendation and pauses charging. The charger state machine enters battery temperature fault state while charging is paused due to extreme high or low temperatures.

The battery's temperature status is reflected by the THM_DTLS[2:0] status bitfield. A maskable interrupt (THM_I) signals a change in THM_DTLS[2:0]. Refer to the *Programmer's Guide* for more information. To completely disable the charger's automatic response to battery temperature, disable the feature by programming THM_EN = 0.

The voltage thresholds corresponding to the JEITA temperature thresholds are independently programmable through THM_HOT[1:0], THM_WARM[1:0], THM_COOL[1:0], and THM_COLD[1:0]. Each threshold can be programmed to one of four voltage options spanning 15°C for an NTC beta of 3380K. See the *Configurable Temperature Thresholds* section and refer to the *Programmer's Guide* for more information.



INTERNAL COOL/WARM SIGNAL	
0b0	THM_DTLS[2:0] = 0b000 OR 0b101 (NTC DISABLED OR BATTERY NORMAL). CHARGER V AND I PARAMETERS FOLLOW NORMAL SETTINGS.
0b1	THM_DTLS[2:0] = 0b010 OR 0b011 (BATTERY COOL OR WARM). CHARGER V AND I PARAMETERS SWITCH TO JEITA SETTINGS.

INTERNAL HOT/COLD SIGNAL	
0b0	THM_DTLS[2:0] ≠ 0b001 OR 0b100 (BATTERY NOT COLD OR HOT). CHARGER V AND I PARAMETERS FOLLOW NORMAL OR JEITA SETTINGS.
0b1	THM_DTLS[2:0] = 0b001 OR 0b100 (BATTERY COLD OR HOT). CHARGING IS PAUSED REGARDLESS OF CHG_EN.

Figure 15. Thermistor Logic Functional Diagram

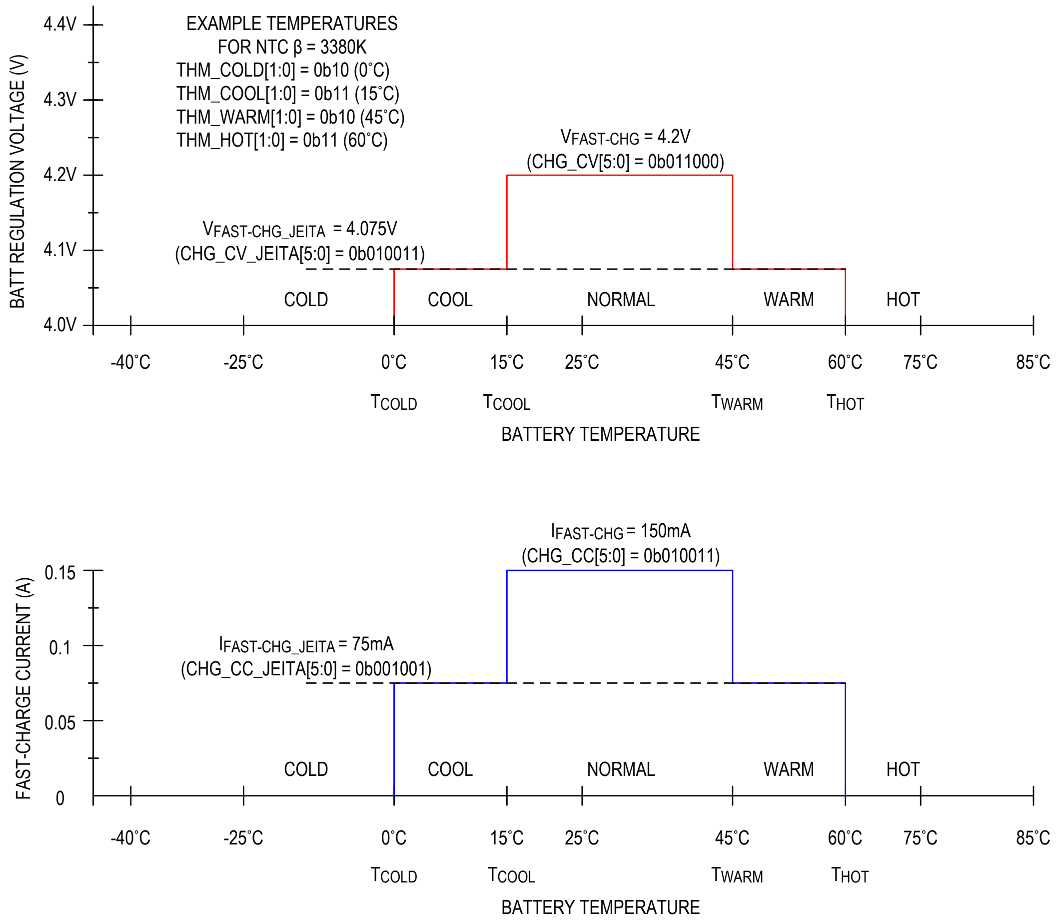


Figure 16. Safe-Charging Profile Example

Thermistor Bias

An external ADC can optionally perform conversions on the THM and TBIAS pins to measure the battery's temperature. An on-chip analog multiplexer is used to route these nodes to the AMUX pin. The operation of the analog multiplexer does not interfere with the charger's temperature monitoring comparators or the charger's automatic JEITA response. See the *Detailed Description—Analog Multiplexer and Power Monitor AFEs* section for more information.

The NTC thermistor's bias source (TBIAS) follows the simple operation outlined as follows:

- If CHGIN is valid and the thermistor is enabled (THM_EN = 1), then the thermistor is biased so the charger can automatically respond to battery temperature changes.
- If the analog multiplexer is connecting THM or TBIAS to AMUX, then the thermistor is biased so an external ADC can perform a meaningful temperature conversion.

The AMUX pin is a buffered output. The operation of the analog multiplexer and external ADC does not collide with the function of the on-chip temperature monitors. Both functions can be used simultaneously with no ill effect.

Configurable Temperature Thresholds

Temperature thresholds for different NTC thermistor beta values are listed in Table 4. The largest possible programmable temperature range can be realized by using an NTC with a beta of 3380K. Using a larger beta compresses the temperature range. The trip voltage thresholds are programmable with the THM_HOT[1:0], THM_WARM[1:0], THM_COOL[1:0], and THM_COLD[1:0] bitfields. All possible programmable trip voltages are listed in Table 4.

These are theoretical values computed by a formula. Refer to the particular NTC's data sheet for more accurate measured data. In all cases, select the value of R_{BIAS} to be equal to the NTC's effective resistance at +25°C.

Applications Information

Using Different Thermistor β

If an NTC with a beta larger than 3380K is used and the resulting available programmable temperature range is undesirably small, then two adjusting resistors can be used to expand the temperature range. R_S and R_P can be optionally added to the NTC thermistor circuit (shown in Figure 18) to expand the range of programmable temperature thresholds.

Select values for R_S and R_P based on the information shown in Table 5.

NTC Thermistor Selection

Popular NTC thermistor options are listed in Table 6.

Table 4. Trip Temperatures vs. Trip Voltages for Different NTC β

TRIP VOLTAGE (V)	TRIP TEMPERATURES (°C)					
	3380K	3435K	3940K	4050K	4100K	4250K
1.024	-10.0	-9.5	-5.6	-4.8	-4.5	-3.5
0.976	-5.0	-4.6	-1.1	-0.5	-0.2	0.6
0.923	0.0	0.3	3.3	3.8	4.1	4.8
0.867	5.0	5.3	7.7	8.1	8.3	8.9
0.807	10.0	10.2	12.0	12.4	12.5	12.9
0.747	15.0	15.1	16.4	16.6	16.7	17.0
0.511	35.0	34.8	33.5	33.3	33.2	32.9
0.459	40.0	39.8	37.8	37.4	37.3	36.8
0.411	45.0	44.7	42.0	41.5	41.3	40.7
0.367	50.0	49.6	46.2	45.6	45.3	44.6
0.327	55.0	54.5	50.4	49.7	49.3	48.4
0.291	60.0	59.4	54.6	53.7	53.3	52.2

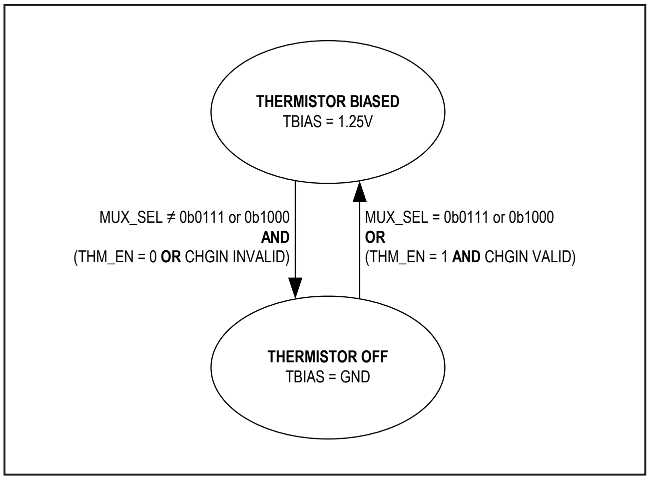


Figure 17. Thermistor Bias State Diagram

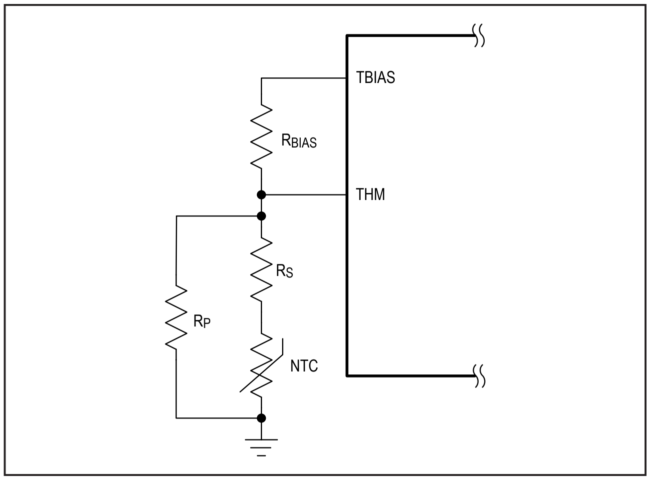


Figure 18. Thermistor Circuit with Adjusting Series and Parallel Resistors

Table 5. Example R_S and R_P Correcting Values for NTC β Above 3380K

PARAMETER	UNIT	EXAMPLES						
NTC thermistor beta	K	3380	3940	3940	4050	4050	4250	4250
25°C NTC resistance	kΩ	10	10	10	47	47	100	100
R_{BIAS}	kΩ	10	10	10	47	47	100	100
Adjusting parallel resistor, R_P	kΩ	open	open	200	open	768	open	1300
Adjusting series resistor, R_S	kΩ	short	short	0.59	short	3.32	short	8870
R_{NTC} at $1.024V_{COLD}$ threshold	kΩ	45.24	45.24	57.89	212.6	290.7	452.4	685.0
R_{NTC} at $0.867V_{COOL}$ threshold	kΩ	22.61	22.61	24.91	106.3	120.0	226.1	264.9
R_{NTC} at $0.459V_{WARM}$ threshold	kΩ	5.81	5.81	5.39	27.3	25.0	58.1	51.9
R_{NTC} at $0.291V_{HOT}$ threshold	kΩ	3.04	3.04	2.49	14.3	11.2	30.4	22.2
T_{ACTUAL} at V_{COLD} [-10°C expected]	°C	-10.03	-5.56	-9.97	-4.82	-10.27	-3.55	-10.46
T_{ACTUAL} at V_{COOL} [5°C expected]	°C	4.98	7.66	5.74	8.10	5.57	8.86	5.93
T_{ACTUAL} at V_{WARM} [40°C expected]	°C	40.02	37.79	39.63	37.43	39.55	36.82	39.37
T_{ACTUAL} at V_{HOT} [60°C expected]	°C	60.04	54.56	60.03	53.68	60.15	52.21	60.18

Table 6. NTC Thermistors

MANUFACTURER	PART	β-CONSTANT (25°C/50°C)	R (Ω) AT 25°C	CASE SIZE
TDK	NTCG063JF223HTBX	3380K	22k	0201
Murata	NCP03XH103F05RL	3380K	10k	0201
Murata	NCP15XH103F03RC	3380K	10k	0402
TDK	NTCG103JX103DT1	3380K	10k	0402
Cantherm	CMFX3435103JNT	3435K	10k	0402
Murata	NCP15XV103J03RC	3900K	10k	0402
Panasonic	ERT-JZEP473J	4050K	47k	0201
Panasonic	ABNTC-0402-473J-4100F-T	4100K	47k	0402
Murata	NCP15WF104F03RC	4250K	100k	0402

Detailed Description—Analog Multiplexer and Power Monitor AFEs

An external ADC can be used to measure the chip's various signals for general functionality or on-the-fly power monitoring. The MUX_SEL[3:0] bitfield controls the internal analog multiplexer responsible for connecting the proper channel to the AMUX pin. Each measurable signal is listed in Table 7 with its appropriate multiplexer channel. The voltage on the AMUX pin is a buffered output that ranges from 0V to V_{FS} (1.25V, typ). The buffer has a 50μA quiescent current draw and is only active when the device's main bias is active and a channel is selected (MUX_SEL[3:0] ≠ 0b0000). Disable the buffer by programming to MUX_SEL[3:0] to 0b0000 when not actively converting the voltage on AMUX.

Table 7 shows how to translate the voltage signal on the AMUX pin to the value of the parameter being measured.

See the *Electrical Characteristics* table and refer to the *Programmer's Guide* for more details.

Table 7. AMUX Signal Transfer Functions

SIGNAL	MUX_ SEL[3:0]	TRANSFER FUNCTION	FULL-SCALE SIGNAL MEANING (V_{AMUX} = 1.25V)	ZERO-SCALE SIGNAL MEANING (V_{AMUX} = 0V)
CHGIN pin voltage	0b0001	$V_{CHGIN} = \frac{V_{AMUX}}{G_{VCHGIN}}$	7.5V	0V
CHGIN pin current	0b0010	$I_{CHGIN} = \frac{V_{AMUX}}{G_{ICHGIN}}$	0.475A	0A
BATT pin voltage	0b0011	$V_{BATT} = \frac{V_{AMUX}}{G_{VBATT}}$	4.6V	0V
BATT pin charging current	0b0100	$I_{BATT(CHG)} = \frac{V_{AMUX}}{V_{FS}} \times I_{FAST-CHG}$	100% of $I_{FAST\text{-}CHG}$ (CHG_CC[5:0])	0% of $I_{FAST\text{-}CHG}$
BATT pin discharge current	0b0101	$I_{BATT(DISCHG)} = \frac{(V_{AMUX} - V_{NULL})}{(V_{FS} - V_{NULL})} \times I_{DISCHG-SCALE}$	100% of $I_{DISCHG\text{-}SCALE}$ (IMON_DISCHG_ SCALE[3:0])	0% of $I_{DISCHG\text{-}SCALE}$
BATT pin discharge current NULL	0b0110	$V_{NULL} = V_{AMUX}$	1.25V	0V
THM pin voltage	0b0111	$V_{THM} = V_{AMUX}$	1.25V	0V
TBIAS pin voltage	0b1000	$V_{TBIAS} = V_{AMUX}$	1.25V	0V
AGND pin voltage*	0b1001	$V_{AGND} = V_{AMUX}$	1.25V	0V
SYS pin voltage	0b1010	$V_{SYS} = \frac{V_{AMUX}}{G_{VSYS}}$	4.8V	0V

**AGND pin voltage is accessed through a 100Ω (typ) pulldown resistor.*

Setting MUX_SEL[3:0] to 0b0000 disables the multiplexer and changes the AMUX pin to a high-impedance state.

Measuring Battery Current

It is possible to sample the current in the BATT pin at any time or in any mode with an external ADC. For improved accuracy, the analog circuitry used for monitoring battery discharge current is different from the circuitry monitoring battery charge current. Table 8 outlines how to determine the direction of battery current.

Method for Measuring Discharging Current

1) Program the multiplexer to switch to the discharge NULL measurement by changing MUX_SEL[3:0] to 0b0110. A NULL conversion must always be performed first to cancel offsets.
2) Wait the appropriate channel switching time (0.3µs, typ).
3) Convert the voltage on the AMUX pin and store as V_{NULL}.
4) Program the multiplexer to switch to the battery discharge current measurement by changing MUX_SEL[3:0] to 0b0101. A nonnulling conversion should be done immediately after a NULL conversion.
5) Wait the appropriate channel switching time (0.3µs, typ).
6) Convert the voltage on AMUX pin and use the following transfer function to determine the discharge current:

$$I_{BATT(DISCHG)} = \frac{(V_{AMUX} - V_{NULL})}{(V_{FS} - V_{NULL})} \times I_{DISCHG-SCALE}$$

V_{FS} is 1.25V typical. $I_{DISCHG\text{-}SCALE}$ is programmable through IMON_DISCHG_SCALE[3:0]. The default value is 300mA. If smaller currents are anticipated, then $I_{DISCHG\text{-}SCALE}$ can be reduced for improved measurement accuracy.

Method for Measuring Charging Current

1) Program the multiplexer to switch to the charge current measurement by changing MUX_SEL[3:0] to 0b0100.
2) Wait the appropriate channel switching time (0.3µs, typ).
3) Convert the voltage on the AMUX pin and use the following transfer function to determine charging current:

$$I_{BATT(CHG)} = \frac{V_{AMUX}}{V_{FS}} \times I_{FAST-CHG}$$

V_{FS} is 1.25V typical. $I_{FAST\text{-}CHG}$ the charger's fast-charge constant-current setting and is programmable through CHG_CC[5:0].

Detailed Description—SIMO Buck-Boost

The device has a micropower single-inductor, multiple-output (SIMO) buck-boost DC-to-DC converter designed for applications that emphasize low supply current and small solution size. A single inductor is used to regulate three separate outputs, saving board space while delivering better total system efficiency than equivalent power solutions using one buck and linear regulators.

The SIMO configuration utilizes the entire battery voltage range due to its ability to create output voltages that are above, below, or equal to the input voltage. Peak inductor current for each output is programmable to optimize the balance between efficiency, output ripple, EMI, PCB design, and load capability.

Table 8. Battery Current Direction Decode

MEASUREMENT	CHARGING OR DISCHARGING INDICATORS		
	CHG BIT	**CHG_DTLS[3:0]**	**CHGIN_DTLS[1:0]**
Discharging Battery Current (Positive Battery Terminal Sourcing Current)	*Don't care*	*Don't care*	0b00 0b01 0b10
Charging Battery Current (Positive Battery Terminal Sinking Current)	1	0b0001 - 0b0111	0b11

SIMO Features and Benefits

- Three Output Channels
- Ideal for Low-Power Designs
  - Delivers > 300mA at 1.8V from a 3.7V Input
  - ±4% Accurate Output Voltage
- Small Solution Size
  - Multiple Outputs from a Single 1.5µH (0603) Inductor
  - Small 10µF (0402) Output Capacitors
- Flexible and Easy to Use
  - Single Mode of Operation
  - Glitchless Transitions Between Buck, Buck-Boost, and Boost Scenarios
  - Programmable Peak Inductor Current
  - Programmable On-Chip Active Discharge
- Long Battery Life
  - High Efficiency, > 87% at 3.3V Output
  - Better Total System Efficient than Buck + LDOs
  - Low Quiescent Current, 1µA per Output
  - Low Input Operating Voltage, 2.7V (min)

SIMO Control Scheme

The SIMO buck-boost is designed to service multiple outputs simultaneously. A proprietary controller ensures that all outputs get serviced in a timely manner, even while multiple outputs are contending for the energy stored in the inductor. When no regulator needs service, the state machine rests in a low-power rest state. See Figure 19.

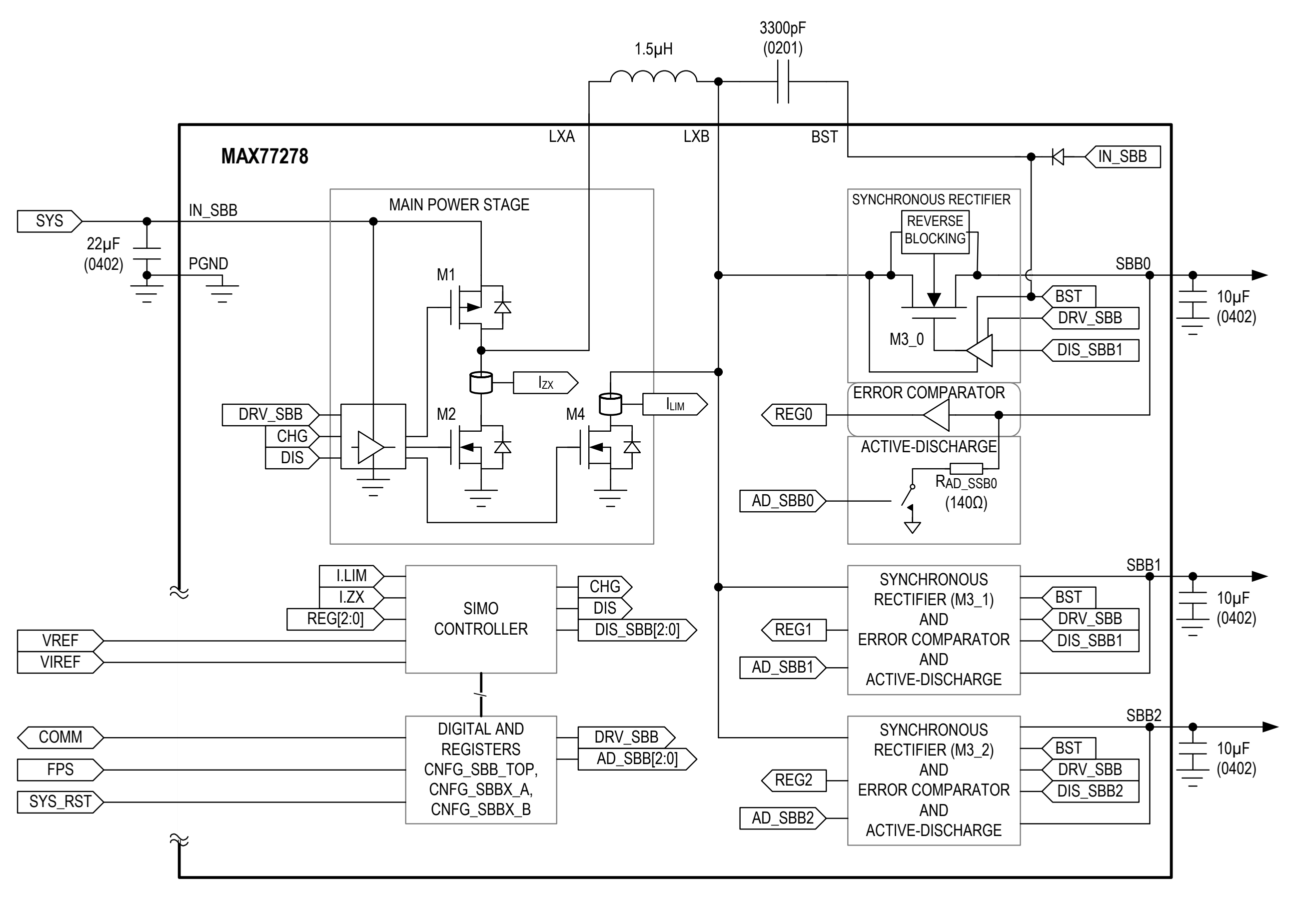


Figure 19. SIMO Detailed Block Diagram

When the controller determines that a regulator requires service, it charges the inductor (M1 + M4) until the peak current limit is reached (I_{LIM} = IP_SBB). The inductor energy then discharges (M2 + M3_x) into the output until the current reaches zero (I_{ZX}). In the event that multiple output channels need servicing at the same time, the controller ensures that no output utilizes all of the switching cycles. Instead, cycles interleave between all the outputs that are demanding service, while outputs that do not need service are skipped.

SIMO Soft-Start

The soft-start feature of the SIMO limits inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup (dV/dt_{SS}).

More output capacitance results in higher input current surges during startup. The following set of equations and example describes the input current surge phenomenon during startup.

The current into the output capacitor (I_{CSBB}) during soft-start is:

$$I_{CSBB} = C_{SBB}\frac{dV}{dt_{SS}} \quad \text{(Equation 1)}$$

where:

- C_{SBB} is the capacitance on the output of the regulator
- dV/dt_{SS} is the voltage change rate of the output

The input current (I_{IN}) during soft-start is:

$$I_{IN} = \frac{\left(I_{CSBB} + I_{LOAD}\right)\frac{V_{SBBx}}{V_{IN}}}{\xi} \quad \text{(Equation 2)}$$

where:

- I_{CSBB} is from the calculation above
- I_{LOAD} is current consumed from the external load
- V_{SBBx} is the output voltage
- V_{IN} is the input voltage
- ξ is the efficiency of the regulator

For example, given the following conditions, the peak input current (I_{IN}) during soft-start is ~71mA:

Given:

- V_{IN} is 3.5V
- V_{SBB2} is 3.3V
- C_{SBB2} = 10µF
- dV/dt_{SS} = 5mV/µs
- R_{LOAD2} = 330Ω (I_{LOAD2} = 3.3V/330Ω = 10mA)
- ξ is 80%

Calculation:

- I_{CSBB} = 10µF x 5mV/µs (from Equation 1)
- I_{CSBB} = 50mA
- $I_{IN} = \frac{(50mA + 10mA)\frac{3.3V}{3.5V}}{0.85}$ (from Equation1)
- I_{IN} ~ 71mA

SIMO Configuration

Each SIMO buck-boost channel has a dedicated register to program its target output voltage (TV_SBBx) and its peak current limit (IP_SBBx). Additional controls are available for enabling/disabling the active discharge resistors (ADE_SBBx), as well as enabling/disabling the SIMO buck-boost channels (EN_SBBx). For a full description of bits, registers, default values, and reset conditions, refer to the *Programmer's Guide*.

SIMO Active Discharge Resistance

Each SIMO buck-boost channel has an active-discharge resistor (R_{AD_SBBx}) that is automatically enabled/disabled based on a ADE_SBBx and the status of the SIMO regulator. The active discharge feature can be enabled (ADE_SBBx = 1) or disabled (ADE_SBBx = 0) independently for each SIMO channel. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. If the active-discharge resistor is enabled by default, then the active-discharge resistor is on whenever V_{SYS} is below $V_{SYSUVLO}$ and above V_{POR}.

These resistors discharge the output when ADE_SBBx = 1, and their respective SIMO channel is off. Note if the regulator is forced on through EN_SBBx = 0b110 or 0b111, then the resistors do not discharge the output even if the regulator is disabled by the main-bias.

Note that when V_{SYS} is less than 1.0V, the NMOS transistors that control the active discharge resistors lose their gate drive and become open.

When the active discharge resistor is engaged, limit its power dissipation to an average of 10mW. For example, consider the case where the active discharge resistance is discharging the output capacitor each time the regulator turns off; the 10mW limit allows discharge of 80µF of capacitance charged to 5V every 100ms (P = [0.5xCxV^2]/t = [0.5x80µFx5V^2]/100ms = 10mW).

Applications Information

SIMO Available Output Current

The available output current on a given SIMO channel is a function of the input voltage, output voltage, the peak current-limit setting, and the output current of the other SIMO channels. Maxim offers a calculator that outlines the available capacity for specific conditions. Table 9 is an extraction from the calculator.

Inductor Selection

Choose an inductance from 1.0µH to 2.2µH; 1.5µH inductors work best for most designs. Larger inductance transfers more energy to the output for each cycle and typically results in larger output voltage ripple and better efficiency. See the *Output Capacitor Selection* section for more information on how to size your output capacitor in order to control ripple.

Choose the inductor saturation current to be greater than or equal to the maximum peak current-limit setting that is used for all of the SIMO buck-boost channels (I_{P_SBB}). For example, if SBB0 is set for 0.5A, SBB1 is set for 0.866A, and SBB2 is set for 1.0A, then choose the saturation current to be greater than or equal to 1A.

Choose the RMS current rating of the inductor (typically the current at which the temperature rises appreciably) based on the expected load currents for the system.

Consider the DC-resistance (DCR), AC-resistance (ACR), and physical size of the inductor. Smaller size inductors tend to have larger DCR and ACR that reduce SIMO efficiency and available output current. For this SIMO regulator, inductors with the lowest ACR in the 1.0MHz to 2.0MHz region tend to provide the best efficiency.

Table 9. SIMO Available Output Current for Common Applications

PARAMETERS	EXAMPLE 1	EXAMPLE 2	EXAMPLE 3
V.IN.MIN	3V	3.2V	3.4V
R.L.DCR	0.1Ω	0.1Ω	0.1Ω
SBB0	5.3V at 40mA	5.0V at 25mA	3.3V at 10mA
SBB1	1.9V at 100mA	1.8V at 150mA	1.5V at 40mA
SBB2	3.2V at 50mA	3.3V at 25mA	1.2V at 80mA
IP_SBB0	1A	0.866A	0.5A
IP_SBB1	1A	1A	0.5A
IP_SBB2	1A	0.866A	0.5A
Utilized Capacity	82%	81%	78%

**R.C.IN = R.C.OUT = 5mΩ, L = 1.5µH*

See Table 10 for examples of inductors that work well with this device. This table was created in 2016. Inductor technology advances rapidly. Always consider the most current inductor technology for new designs to achieve the best possible performance.

Input Capacitor Selection

Bypass IN_SBB to GND with a minimum 10µF ceramic capacitor (C_{IN_SBB}). Larger values of C_{IN_SBB} improve the decoupling for the SIMO regulator.

C_{IN_SBB} reduces the current peaks drawn from the battery or input power source during SIMO regulator operation and reduces switching noise in the system. The ESR/ESL of the input capacitor should be very low (i.e., ≤ 5mΩ + ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

To fully utilize the available input voltage range of the SIMO (5.5V, max), use a 6.3V capacitor voltage rating.

In the PCB layout, place C_{IN_SBB} as close as possible to the power pins (IN_SBB and PGND) to minimize parasitic inductance. If making connections to the input capacitor through vias, ensure that the vias are rated for the expected input current so they do not contribute excess inductance and resistance between the bypass capacitor and the power pins.

Boost Capacitor Selection

Choose the boost capacitance (C_{BST}) to be 3.3nF. Smaller values of C_{BST} (<1nF) result in insufficient gate drive for M3. Larger values of C_{BST} (>10nF) have the potential to degrade the startup performance. Ceramic capacitors with 0201 or 0402 case size are recommended.

Output Capacitor Selection

Choose each output bypass capacitance (C_{SBBx}) based on the desired output voltage ripple (10µF, typ). Larger values of C_{SBBx} improve the output voltage ripple but increase the input surge currents during soft-start and output voltage changes. The output voltage ripple is a function of the inductance, the output voltage, and the peak current-limit setting. Refer to the *SIMO calculator* to aid in the selection of the output capacitance.

The impedance of the output capacitor (ESR, ESL) should be very low (i.e., ≤ 5mΩ + ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

Table 10. Example Inductors

MANUFACTURER	PART	L (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (Ω)	X (mm)	Y (mm)	Z (mm)
Toko	DFE201610E-2R2M	2.2	2.6	1.9	0.117	2.0	1.6	1.0
Toko	DFE201610E-1R5M	1.5	2.4	3.2	0.076	2.0	1.6	1.0
Toko	DFE201210S-2R2M	2.2	2.3	1.80	0.127	2.0	1.2	1.0
Toko	DFE201210S-1R5M	1.5	2.2	2.6	0.086	2.0	1.2	1.0
Toko	DFE201208S-1R5M	1.5	2.4	2.0	0.110	2.0	1.2	0.8
Toko	DFE201208S-2R2M	2.2	2.0	1.6	0.170	2.0	1.2	0.8
TDK	MLP2012V1R5T	1.5	0.5	0.55	0.4	1.0	1.2	0.55

In the PCB layout, place C_{SBBx} as close as possible to SBBx and PGND to minimize parasitic inductance. If making connections to the output capacitor through vias, ensure that the vias are rated for the expected output current so they do not contribute excess inductance and resistance.

Unused Outputs

Do not leave unused outputs unconnected. If an output left unconnected is accidentally enabled, inductor current dumps into an open pin, and the output voltage soars above the absolute maximum rating, potentially causing damage to the device. If the unused output is always disabled (EN_SBBx = 0x4 or 0x5), connect that output to ground. If an unused output can be enabled at any point during operation (such as startup or accidental software access), then implement one of the following:

1) Bypass the unused output with a 1μF ceramic capacitor to ground.
2) Connect the unused output to the power input (IN_SBB). This connection is beneficial because it does not require an external component for the unused output. The power input and its capacitance receives the energy packets when the regulator is enabled and V_{IN_SBB} is below the target output voltage of the unused output. Circulating the energy back to the power input ensures that the unused output voltage does not fly high.

   Note that some OTP options of the device have the active-discharge resistors enabled by default (ADE_SBBx) such that connecting an unused output SBBx to IN_SBB creates a 140Ω (R_{AD_SBBx}) to ground until software can be ran to disable the active-discharge resistor. Connecting an unused SBBx to IN_SBB is not recommended if the regulator's active-discharge resistor is enabled by default.
3) Connect the unused output to another power output that is above the target voltage of the unused output. In the same way as the option listed above, this connection is beneficial because it does not require an external component for the unused output. Unlike the option above, this connection is preferred in cases where the unused output voltage bias level is always above the unused output voltage target because no energy packages are provided to the unused output.

   Note that some OTP options of the device have the active-discharge resistors enabled by default (ADE_SBBx). If the other power output used to bias the unused output is normally off, then the active-discharge resistor of the unused output does not create a continuous current draw. Once the system is enabled, it should turn off the unused output's active-discharge resistor (ADE_SBBx = 0).

Detailed Description—LDO

The device includes one on-chip low-dropout linear regulator (LDO). This LDO is optimized to have low-quiescent current and low-dropout voltage. The input voltage range of this LDO (V_{IN_LDO}) allows it to be powered directly from the main energy source such as a Li-Poly battery or from an intermediate regulator. The linear regulator delivers up to 50mA.

Features and Benefits

- 50mA LDO
- Class A/B Output Stage
- Maximum of 2.75mVpp Output Ripple
- 1.7V to 5.5V Input Voltage Range
- Adjustable Output Voltage
- 150mV Maximum Dropout Voltage (over PVT) at 50mA
- Short Circuit Current Limited to 320mA (Provides Soft-Start Function)

LDO Simplified Block Diagram

The LDO has one input (IN_LDO) and one output (LDO) and several ports that exchange information with the rest of the device (VREF, EN_LDO, ADE_LDO). VREF comes from the main bias circuits. EN_LDO and ADE_LDO are register bits for controlling the enable and active-discharge feature of the LDO. Refer to the *Programmer's Guide* for more information.

LDO Active Discharge Resistor and Typical Use

The LDO has an active-discharge resistor (R_{AD_LDO}) that automatically enables/disables based on a configuration bit (ADE_LDO) and the status of the LDO regulator. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. The default condition of the active-discharge resistor feature is enabled such that whenever V_{SYS} is above V_{POR} and V_{IN_LDO} is above 1.0V, the LDO active discharge resistor is turned on. Note that when V_{IN_LDO} is less than 1.0V, the NMOS transistor that controls the LDO active discharge resistor loses its gate drive and becomes open.

LDO Soft-Start

The soft-start feature of the LDO limits inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup (dV/dt_{SS}). More output capacitance results in higher input current surges during startup. The equation and example describes the input current surge phenomenon during startup.

The input current (I_{IN}) during soft-start is:

$$I_{IN} = C_{LDO}\frac{dV}{dt_{SS}} + I_{LDO}$$

where:

- C_{LDO} is the capacitance on the output of the regulator
- dV/dt_{SS} is the voltage change rate of the output

For example, given the following conditions, the input current (I_{IN}) during soft-start is 22.5mA:

Given:

- C_{LDO} = 10µF
- dV/dt_{SS} = 1.25mV/µs
- R_{LDO} = 185Ω (I_{LDO} = 1.85V/185Ω = 10mA)

Calculation:

- I_{IN} = 10µF x 1.25mV/µs + 10mA
- I_{IN} = 22.5mA

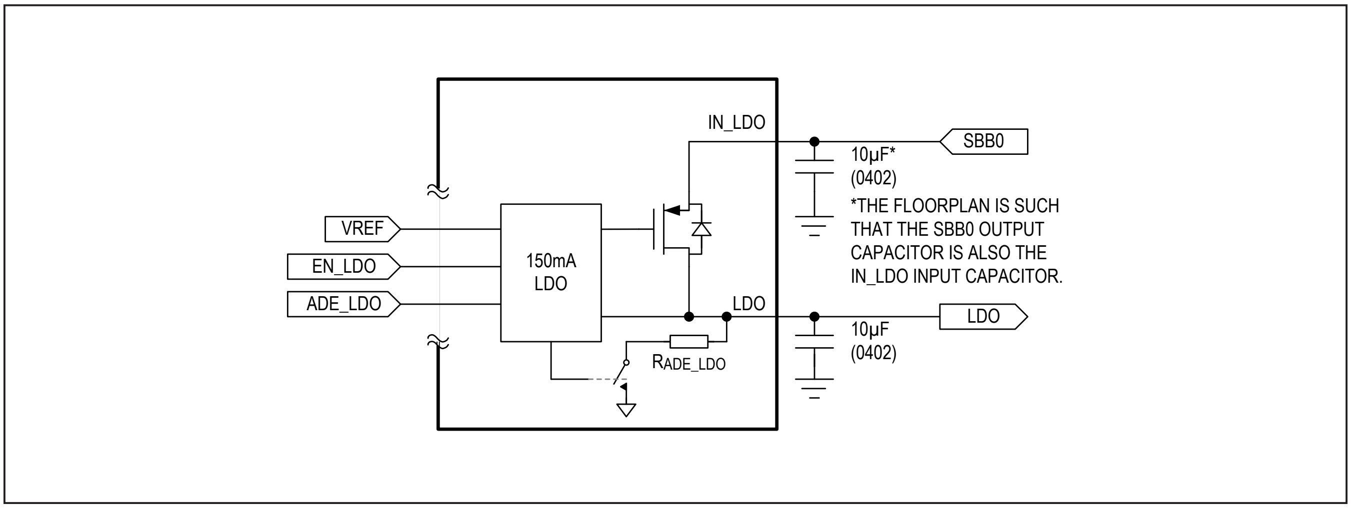


Figure 20. LDO Simplified Block Diagram

Fixed Headroom Controller (FHC)

The LDO features a FHC intended for use when the input of the LDO (IN_LDO) is powered from SBB0. The FHC regulates the output voltage of SBB0 to be V_{HDRM} (150mV to 225mV) above V_{LDO}. This feature allows the LDO to operate close to its minimum headroom voltage to reduce power dissipation in the LDO. This system maximizes the benefit of the SIMO's efficiency to create a low noise output from the LDO.

Connect SBB0 to IN_LDO to make use of the FHC. The output capacitors of SBB0 double as the input capacitors of the LDO. SBB0 regulates to the voltage defined by TV_SBB0[5:0] if the FHC is disabled, or if the LDO output is disabled. When the FHC is enabled, the SBB0 output voltage remains at its own regulation target until the output voltage of the LDO rises above the LDO POK threshold. Once the LDO output rises above the LDO POK threshold, SBB0 regulates to the voltage defined by TV_LDO[6:0] plus the headroom voltage define by V_HDRM[1:0]. TV_SBB0[5:0] is ignored when the FHC is active.

The SBB0 and LDO outputs are tightly coupled together when the FHC is enabled. The LDO_POK_R interrupt asserts if the LDO output drops below the LDO POK threshold to alert the system that the LDO is being pulled low. The outputs of the SBB0 and LDO both collapse to ground if the LDO is heavily overloaded. The SBB0 and LDO output remains latched at ground until the FHC is disabled. Monitor the LDO_POK_R interrupt to detect when the LDO output collapses to ground. Once the LDO_POK_R interrupt asserts, toggle the FHC off and back on to restart the SBB0 and LDO outputs and recover from the overcurrent situation.

The FHC is enabled by default, but is disabled by setting EN_FHC to 0. Systems that don't use SBB0 to power the LDO must disable the FHC after startup.

Applications Information

Input Capacitor Selection

Choose the input bypass capacitance (C_{IN_LDO}) to be 10µF. Larger values of C_{IN_LDO} improve the decoupling for the LDO regulator. The floorplan of the device is such that SBB0 is adjacent to IN_LDO and if the SIMO channel 0 output powers the input of the LDO, then its output capacitor (C_{SBB0}) can also serve as C_{IN_LDO} such that only one capacitor is required.

C_{IN_LDO} reduces the current peaks drawn from the battery or input power source during LDO regulator operation. The impedance of the input capacitor (ESR, ESL) should be very low (i.e., ≤ 50mΩ + ≤ 5nH) for frequencies up to 0.5MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

Output Capacitor Selection

Choose the output bypass capacitance (C_{LDO}) to be 10µF. Larger values of C_{LDO} improve output PSRR, but increases the input surge currents during soft-start and output voltage changes. The effective output capacitance should not exceed 100µF to maintain LDO stability.

C_{LDO} is required to keep the LDO stable. The impedance of the output capacitor should be very low (i.e., ≤ 50mΩ + ≤ 5nH) for frequencies up to 0.5MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

A capacitor's effective capacitance decreases with increased DC bias voltage. This effect is more pronounced as capacitor case sizes decrease. Due to this characteristic, it is possible for 0603 case size capacitors to perform well while 0402 case size capacitors of the same value perform poorly. The LDO is stable with 4µF of effective output capacitance; consider the input capacitance value after initial tolerance, bias voltage, aging, and temperature derating.

Detailed Description—Current Sink

General Description

The device has a current sink driver designed to drive infrared LEDs in portable devices. This block can also be used as a general-purpose current sink driver for other applications. The driver's on-time and frequency are set by directly driving CS_EN high or low. The current sink value is I^{2}C programmable from 250mA to 425mA in 25mA increments.

Features and Benefits

- High Level, Programmable Current Sink
- Programmable from 250mA to 425mA
- High-Speed Current Pulse Rate (up to 500KHz)
- Fast Rise Time Pulse Response (75ns, typ)
- Ideal for IR LED Applications
- Watch-Dog Timer
- Wide Operating Voltage Range
  - 2.7V to 5.5V Operation
  - Low-Dropout Voltage (400mV min)
- Highly Customizable
  - I^{2}C Programmable

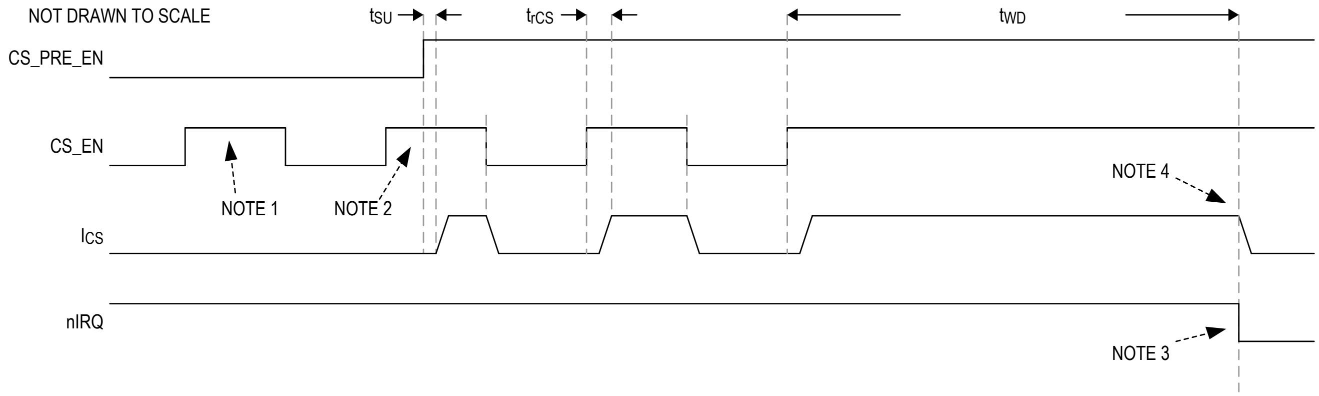
Detailed Description

The current sink is configured to be disabled by default (CS_PRE_EN = 0). Pulses on CS_EN are ignored when CS_PRE_EN is set to 0. Set CS_PRE_EN to 1 to preenable the current sink's bias circuitry. The bias circuitry requires a set up time (t_{SU}) before the output can be controlled by CS_EN.

Once the current sink is preenabled with CS_PRE_EN, it is enabled by pulling CS_EN above its logic high threshold and turned off by pulling CS_EN below its logic low threshold. Modulate the CS_EN pin with the desired control signal to modulate the current in the load attached to the current sink.

The current sink employs a watchdog timer intended to protect the device from fault conditions that leave CS_EN tied high indefinitely. Such a condition could cause damage to the device or the load being driven by the current sink. The watchdog timer starts on the rising edge of a pulse on CS_EN. The watchdog timer expires if CS_EN is held high for longer than 12.8ms. Upon watchdog timer expiration, the CS_WD_R interrupt is tripped as a signal to the system that CS_EN has been held high for too long.

The CS_WD bit controls whether or not the current sink is forcibly disabled upon expiration of the current sink watchdog timer. If CS_WD is set to 0, the CS_WD_R interrupt trips, but the current sink remains active if the watchdog timer expires. If CS_WD is set to 1, the CS_WD_R interrupt trips, and the current sink is forcibly disabled if the watchdog timer expires. A subsequent rising edge on CS_EN reactivates the current sink and restarts the watchdog timer while the CS_WD_R interrupt is still active. If the system is flagged by the CS_WD_R interrupt, it is advisable to set CS_PRE_EN low to disable the current sink. Once the current sink is disabled, the system can determine the source of the fault condition without the possibility of the current sink getting unintentionally forced on again.



NOTES:

1 – CS_EN PULSES ARE IGNORED WHILE CS_PRE_EN IS LOW.

2 – IF CS_EN IS HIGH WHEN CS_PRE_EN IS SET HIGH, THE CURRENT SINK WILL TURN ON AFTER THE CURRENT SINK BIAS CIRCUIT SETUP TIME (t_{SU}).

3 – nIRQ ASSERTS DUE TO THE CS_WD_R INTERRUPT IF CS_EN IS HELD HIGH FOR LONGER THAN THE CURRENT SINK WATCHDOG TIMER (t_{WD}).

4 – IF CS_WD IS SET TO 1, THE CURRENT SINK IS DISABLED UPON ASSERTION OF THE CS_WD_R INTERRUPT.

Figure 21. Current Sink Timing Diagram

Unused Current Sink

If the current sink is not utilized in a given application, connect CS and CS_EN to ground. Additionally, software should ensure that the unused current sink is not enabled (CS_PRE_EN = 0).

Current Sink Simplified Block Diagram

The current sink has one input (CS_EN), one output (CS), one dedicated ground (CS_GND), and several ports that exchange information with the rest of the device (CS_CURR, CS_PRE_EN, CS_WD, CS_WD_R). CS_CURR, CS_PRE_EN, and CS_WD are register bits for controlling the operation of the current sink. CS_WD_R is an interrupt dedicated to the current sink watchdog timer.

Detailed Description—I^{2}C

The device features a revision 3.0 I^{2}C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The IC is a slave-only device that relies on an external bus master to generate SCL. SCL clock rates from 0Hz to 3.4MHz are supported. I^{2}C is an open-drain bus and therefore SDA and SCL require pullups.

The device's I^{2}C communication controller implements 7-bit slave addressing. An I^{2}C bus master initiates communication with the slave by issuing a START condition followed by the slave address. The OTP address is factory programmable for one of two options (see Table 11). All slave addresses not mentioned in Table 11 are not acknowledged.

The device uses 8-bit registers with 8-bit register addressing. They support standard communication protocols: (1) Writing to a single register (2) Writing to multiple sequential registers with an automatically incrementing data pointer (3) Reading from a single register (4) Reading from multiple sequential registers with an automatically incrementing data pointer. For additional information on the I^{2}C protocols, refer the *I^{2}C-Compatible Serial Interface Implementation Guide*, or the I^{2}C specification that is freely available on the Internet.

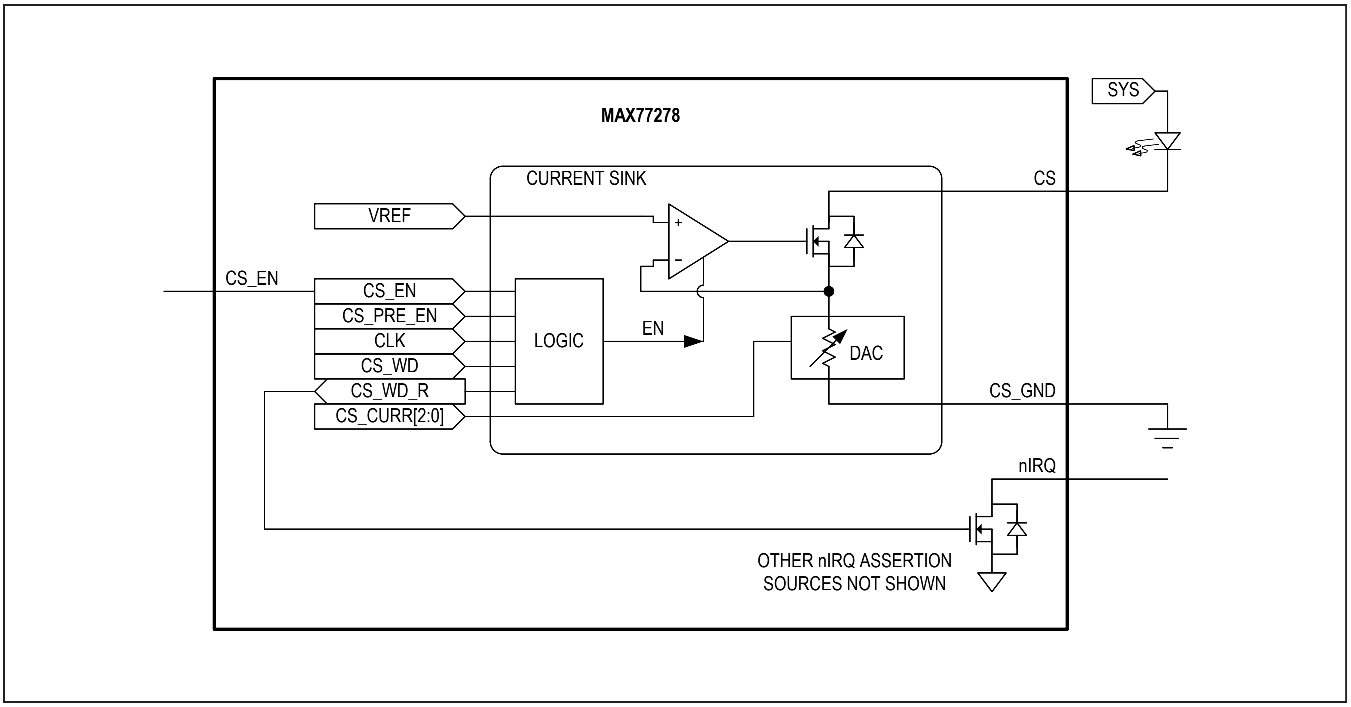


Figure 22. Current Sink Simplified Block Diagram

Table 11. I²C Slave Address Options

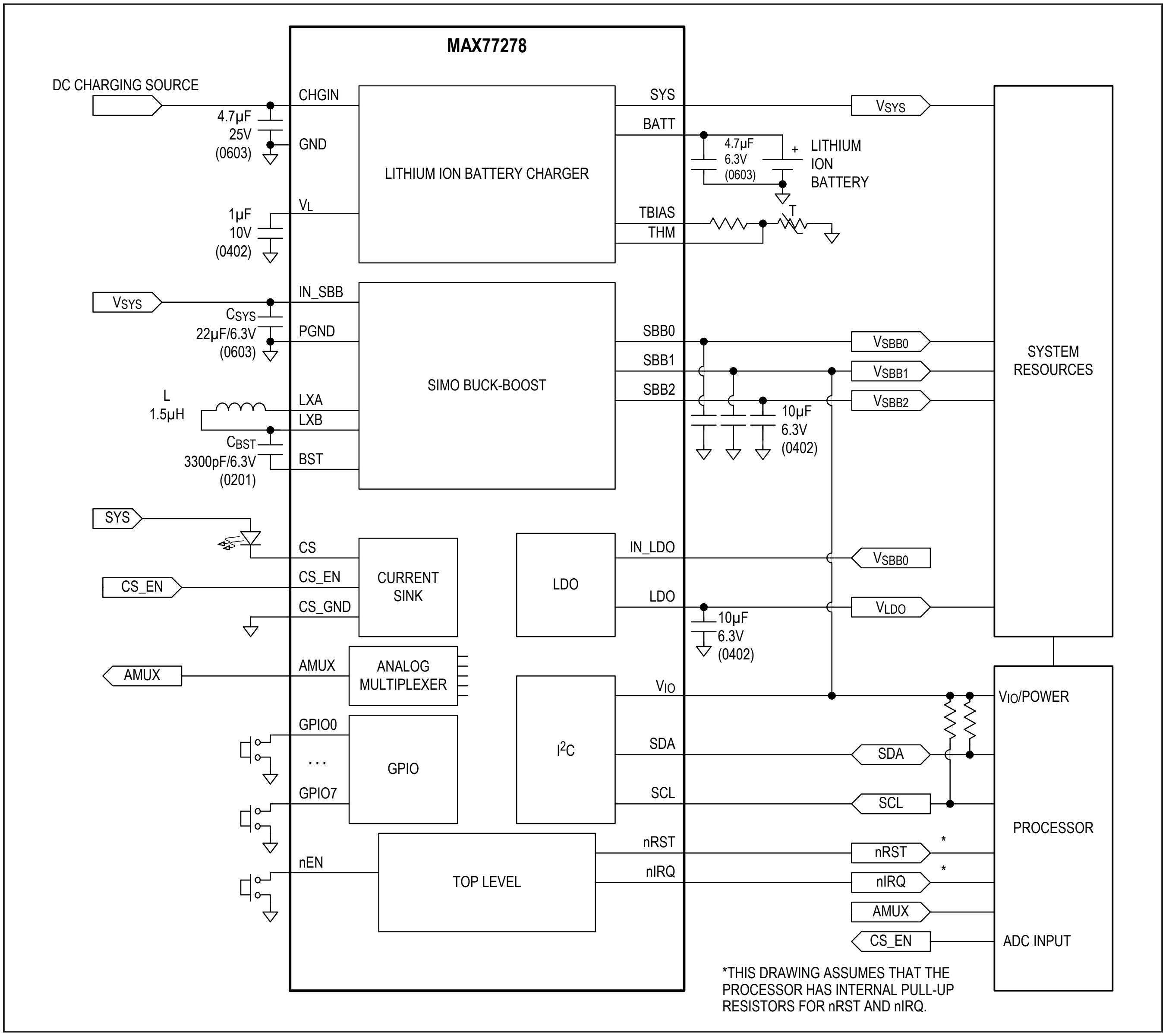
ADDRESS	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
Main Address (ADDR = 1)*	0x48, 0b 100 1000	0x90, 0b 1001 0000	0x91, 0b 1001 0001
Main Address (ADDR = 0)*	0x40, 0b 100 0000	0x80, 0b 1000 0000	0x81, 0b 1000 0001
Other Acknowledges**	0x25, 0b 010 0101 0x50, 0b 101 0000	0x4A, 0b 0100 1010 0xA0, 0b 1010 0000	0x4B, 0b 0100 1011 0xA1, 0b 1010 0001
Test Mode***	0x49, 0b 100 1001 0x5A, 0b 101 1001 0x68, 0b 110 1000	0x92, 0b 1001 0010 0xB2, 0b 1011 0010 0xD0, 0b 1101 0000	0x93, 0b 1001 0011 0xB3, 0b 1011 0011 0xD1, 0b 1101 0001

**Perform all reads and writes on the main address. ADDR is a factory one-time programmable (OTP) option, allowing for address changes in the event of a bus conflict. Contact Maxim for more information.*

***The device acknowledges other addresses. There is no functionality associated with these addresses. Do not use other I²C devices with these addresses on the same bus.*

****When test mode is unlocked, the additional address is acknowledged. Test mode details are confidential. If possible, leave the test mode address unallocated to allow for the rare event that debugging needs to be performed in cooperation with Maxim.*

Typical Application Circuit



*THIS DRAWING ASSUMES THAT THE PROCESSOR HAS INTERNAL PULL-UP RESISTORS FOR nRST AND nIRQ.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX77278EWB+T	-40°C to +85°C	35 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
***Note:** See the Programmer’s Guide for the options associated with a specified DIDM and CID.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/17	Initial release	—
1	11/17	Updated title, *Applications* section, and *Benefits and Features* section, added *Support Materials* section, updated *Detailed Description—SIMO Buck-Bost* section, updated *Ordering Information* table	1, 6, 18, 30, 33, 57, 59, 60, 67
2	7/18	Updated *Ordering Information* table	67