Dual Sigma-Delta ADC with Auxiliary DAC

AD7729

FEATURES
+3 V Supply Voltage
Baseband Serial Port (BSPORT)
Differential IRx and QRx
ADC Channels
Two 15-Bit Sigma-Delta A/D Converters
FIR Digital Filters
64 dB SNR
Output Word Rate 270.83 kHz
Twos Complement Coding
On-Chip Offset Calibration
Power-Down Mode
Auxiliary D/A Converter
Auxiliary Serial Port (ASPORT)
On-Chip Voltage Reference
Low Power
28-Lead TSSOP/28-Lead SOIC

APPLICATIONS
GSM Basestations
Pagers

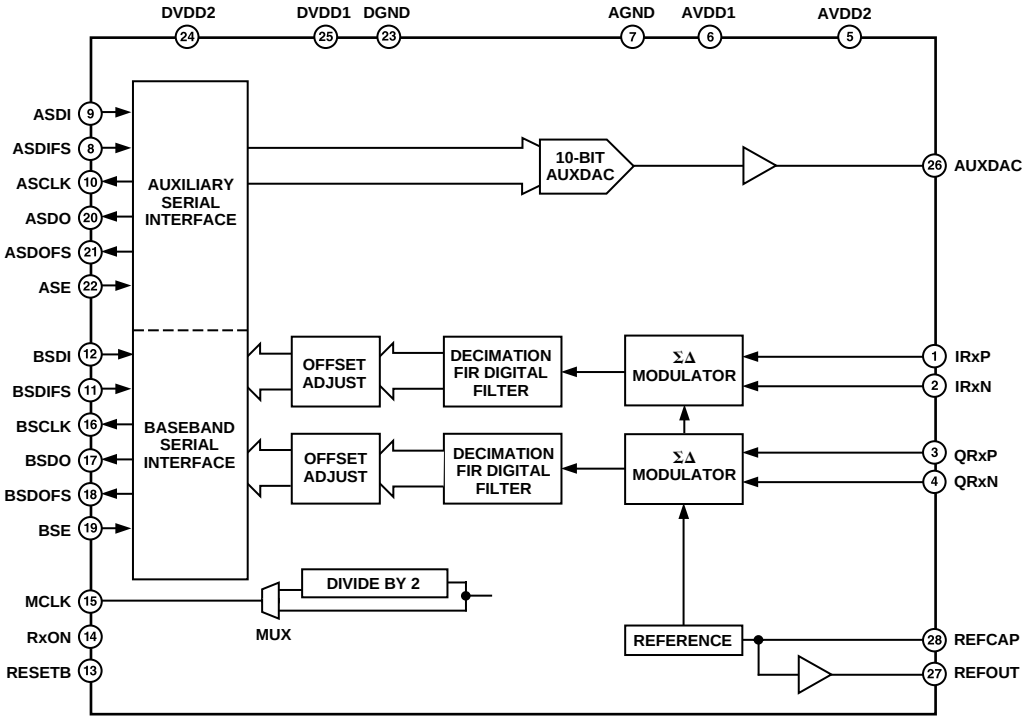
GENERAL DESCRIPTION

This monolithic 3 V CMOS device is a low power, two-channel, input port with signal conditioning. The receive path is composed of two high performance sigma-delta ADCs with digital filtering. A common bandgap reference feeds the ADCs.

A control DAC is included for such functions as AFC. The auxiliary functions can be accessed via the auxiliary port (ASPORT).

This device is available in a 28-lead TSSOP package or a 28-lead SOIC package.

FUNCTIONAL BLOCK DIAGRAM



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Data Sheet

- AD7729: Dual Sigma-Delta ADC with Auxiliary DAC Data Sheet

TOOLS AND SIMULATIONS

- Sigma-Delta ADC Tutorial

REFERENCE MATERIALS

Technical Articles

- Delta-Sigma Rocks RF, As ADC Designers Jump On Jitter
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7729 Material Declaration
- PCN-PDN Information
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AD7729–SPECIFICATIONS[1] (AVDD1 = AVDD2 = +3 V ± 10%; DVDD1 = DVDD2 = +3 V ± 10%; DGND = AGND = 0 V, f_{CLK} = 13 MHz; RxPOWER1 = 0; RxPOWER0 = 1; MCLKDIV = 0; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	AD7729A	Units	Test Conditions/Comments
REFERENCE			
REFCAP			
Absolute Voltage, V_{REFCAP}	1.3 ± 5%	V min/max	
REFCAP TC	50	ppm/°C typ	0.1 µF Capacitor Required from REFCAP to AGND
REFOUT			
Absolute Voltage, V_{REFOUT}	1.3 ± 10%	V min/max	
REFOUT TC	50	ppm/°C typ	0.1 µF Capacitor Required from REFOUT to AGND
ADC CHANNEL SPECIFICATIONS			RxON = 1
Resolution	15	Bits	
ADC Signal Range	2 V_{REFCAP}	V p-p	
V_{BIAS}	$V_{REFCAP}/2$ to (AVDD – $V_{REFCAP}/2$)	Volts	Differential
	V_{REFCAP} to (AVDD – V_{REFCAP})	Volts	Single-Ended
Differential Signal Range	$V_{BIAS} \pm V_{REFCAP}/2$	V min/max	For Both Positive and Negative Analog Inputs
Single-Ended Signal Range	$V_{BIAS} \pm V_{REFCAP}$	V min/max	For Positive Analog Inputs; Negative Analog Inputs = V_{BIAS}
Input Sample Rate	13	MSPS	
Output Word Rate	270.83	kHz	
DC Accuracy			
Precalibration Offset Error	±45	mV typ	
Post Calibration Offset Error	±10	mV max	
Post Calibration Offset Error TC	50	µV/°C typ	TC = Temperature Coefficient
Input Resistance (DC)	1.23	MΩ typ	
Input Capacitance	10	pF typ	
Dynamic Specifications			Input Frequency = 67.7 kHz
Dynamic Range	67	dB typ	
Signal to (Noise + Distortion)	64	dB min	
Gain Error	±1	dB max	Input Frequency = 67.7 kHz, wrt 1.3 V
	±0.5	dB max	Input Frequency = 67.7 kHz, wrt V_{REFCAP}
Gain Match Between Channels	±0.2	dB max	
Filter Settling Time	47	µs typ	
Frequency Response			Does Not Include Input Antialias RC Circuit
0 kHz–70 kHz	±0.05	dB max/min	
85 kHz	–1	dB max	
96 kHz	–3.0	dB max	
135 kHz	–55	dB max	
>170 kHz	–55	dB max	
Absolute Group Delay	23	µs typ	
Group Delay Between Channels			
(0 kHz–96 kHz)	5	ns typ	
Coding	Twos Complement		
AUXILIARY CONVERTER[2]			
Resolution	10	Bits	
Output Range			
Code 000	2/32 × V_{REFCAP}	V	
Offset Error	±35	mV max	
Code 3FF	2 V_{REFCAP}	V	
Gain Error	–60	mV min	
	+100	mV max	
DC Accuracy			Maximum Output for Specified Accuracy = AVDD – 0.2 V or 2.6 V, Whichever Is Lower
Integral Nonlinearity	±4	LSB max	
Differential Nonlinearity	±2	LSB max	Guaranteed Monotonic to 9 Bits
Update Rate	540	kHz max	
Load Resistance	10	kΩ min	See Figure 1
Load Capacitance	50	pF max	See Figure 1
I_{SINK}	50	µA typ	
Full-Scale Settling Time	4	µs typ	
LSB Settling Time	2	µs typ	
Coding	Binary		

Parameter	AD7729A	Units	Test Conditions/Comments
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD} – 0.8	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{IH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	V_{DD} – 0.4	V min	$\|I_{OUT}\| \leq 100$ μA
V_{OL}, Output Low Voltage	0.4	V max	$\|I_{OUT}\| \leq 100$ μA
I_{OZL}, Low Level Output Three-State Leakage Current	10	μA max	
I_{OZH}, High Level Output Three-State Leakage Current	10	μA max	
POWER SUPPLIES			
AVDD1, AVDD2	2.7/3.3	V min/max	
DVDD1, DVDD2	2.7/3.3	V min/max	
I_{DD}			See Table I

NOTES
[1]Operating Temperature Range: –40°C to +105°C. Therefore, T_{MIN} = –40°C and T_{MAX} = +105°C.
[2]During power-down, the AUXDAC has an output resistance of 30 kΩ approximately to AGND.
Specifications subject to change without notice.

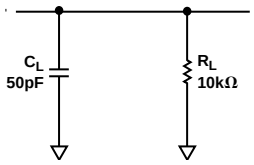


Figure 1. AUXDAC Load Equivalent Circuit

Table I. Current Summary (AVDD1 = AVDD2 = DVDD1 = DVDD2 = +3.3 V, RxPOWER1 = 0, RxPOWER0 = 1)

Conditions	Analog Current (typ)	Internal Digital Current (typ)	External Interface Current (typ)	Total Current (max)	BSE	ASE	MCLK ON	Comments
ADCs On Only	4.2	3.4	4	13.5	1	0	YES	REFOUT Enabled, BSCLK = MCLK
AUXDAC On Only	2	0.86	0.1	3.4	0	1	YES	REFOUT Disabled, ASCLK = MCLK/48
REFCAP On Only	0.7	0.0001	0.002	1.1	0	0	NO	REFOUT Disabled
REFCAP and REFOUT On Only	1	0.0001	0.002	1.7	0	0	NO	REFOUT Enabled
All Sections Off	0.0001	0.04	0.015	0.1	0	0	YES	MCLK Active Levels Equal to 0 V and DVDD
All Sections Off	0.0001	0.0001	0.005	0.05	0	0	NO	Digital Inputs Static and Equal to 0 V or DVDD

The above values are in mA.

Table II. Receive Section Signal Ranges

Baseband Section	Signal Range
V_{REFCAP}	1.3 V ± 5%
V_{REFOUT}	1.3 V ± 10%
ADC	
ADC Signal Range	2 V_{REFCAP}
V_{BIAS}	
Differential Input	$V_{REFCAP}/2$ to (AVDD1 – $V_{REFCAP}/2$)
Single-Ended Input	V_{REFCAP} to (AVDD1 – V_{REFCAP})
Signal Range	
Differential	$V_{BIAS} \pm V_{REFCAP}/2$
Single-Ended	$V_{BIAS} \pm V_{REFCAP}$

Table III. Auxiliary Section Signal Ranges

AUXDAC	Signal Range
Output Code	
Code 000	$2/32 \times V_{REFCAP}$
Code 3FF	2 V_{REFCAP}

TIMING CHARACTERISTICS

(AVDD1 = AVDD2 = +3 V ± 10%; DVDD1 = DVDD2 = +3 V ± 10%; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_A = –40°C to +105°C	Units	Description
AUXILIARY FUNCTIONS			
Clock Signals			See Figure 2.
t_1	76	ns min	MCLK Period
t_2	30.4	ns min	MCLK Width Low
t_3	30.4	ns min	MCLK Width High
t_4	t_1	ns min	ASCLK Period. See Figures 4 and 6.
t_5	$0.4 \times t_1$	ns min	ASCLK Width Low
t_6	$0.4 \times t_1$	ns min	ASCLK Width High
t_{10}	20	ns min	ASDI/ASDIFS Setup Before ASCLK Low
t_{11}	10	ns min	ASDI/ASDIFS Hold After ASCLK Low
t_{12}	15	ns max	ASDOFS Delay from ASCLK High
t_{13}	0	ns min	ASDOFS Hold After ASCLK High
t_{14}	0	ns min	ASDO Hold After ASCLK High
t_{15}	15	ns max	ASDO Delay from ASCLK High
t_{16}	10	ns min	ASDIFS Low to ASDI LSB Read by ASPORT
t_{17}	t_4 + 15	ns min	Interval Between Consecutive ASDIFS Pulses
Receive Section			
Clock Signals			See Figures 5 and 7.
t_7	t_1	ns min	BSCLK Period
t_8	$0.4 \times t_1$	ns min	BSCLK Width Low
t_9	$0.4 \times t_1$	ns min	BSCLK Width High
t_{18}	20	ns min	BSDI/BSDIFS Setup Before BSCLK Low
t_{19}	10	ns min	BSDI/BSDIFS HoldAfter BSCLK Low
t_{20}	15	ns max	BSDOFS Delay from BSCLK High
t_{21}	0	ns min	BSDOFS Hold After BSCLK High
t_{22}	0	ns min	BSDO Hold After BSCLK High
t_{23}	15	ns max	BSDO Delay from BSCLK High
t_{24}	10	ns min	BSDIFS Low to ASDI LSB Read by BSPORT
t_{25}	t_7 + 15	ns min	Interval Between Consecutive BSDIFS Pulses

ASCLK = MCLK/(2 × ASCLKRATE). ASCLKRATE can have a value from 0 . . . 1023. When ASCLKRATE = 0, ASCLK = 13 MHz.
BSCLK = MCLK/(2 × BSCLKRATE). BSCLKRATE can have a value from 0 . . . 1023. When BSCLKRATE = 0, BSCLK = 13 MHz.

Specifications subject to change without notice.

TIMING DIAGRAMS

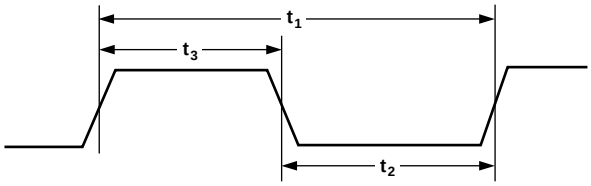


Figure 2. Clock Timing

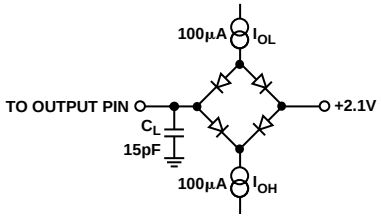
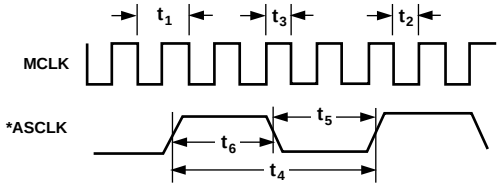
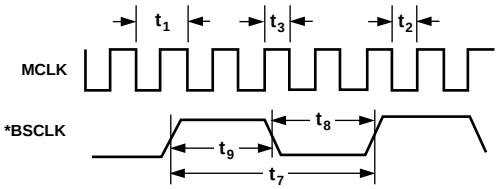


Figure 3. Load Circuit for Timing Specifications



*ASCLK IS INDIVIDUALLY PROGRAMMABLE IN FREQUENCY (MCLK/4 SHOWN HERE).

Figure 4. ASCLK



*BSCLK IS INDIVIDUALLY PROGRAMMABLE IN FREQUENCY (MCLK/4 SHOWN HERE).

Figure 5. BSCLK

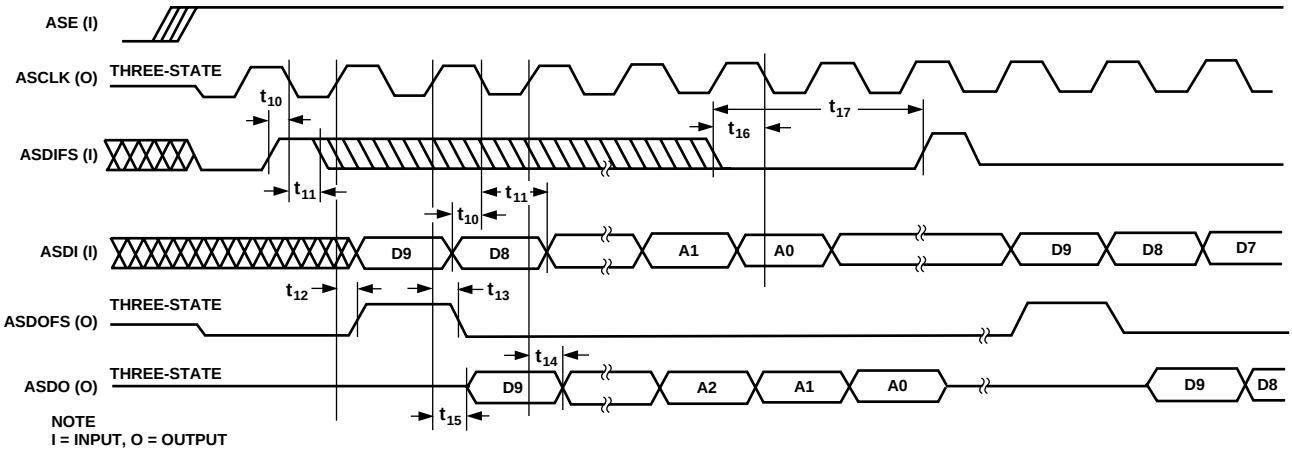


Figure 6. Auxiliary Serial Port ASPORT

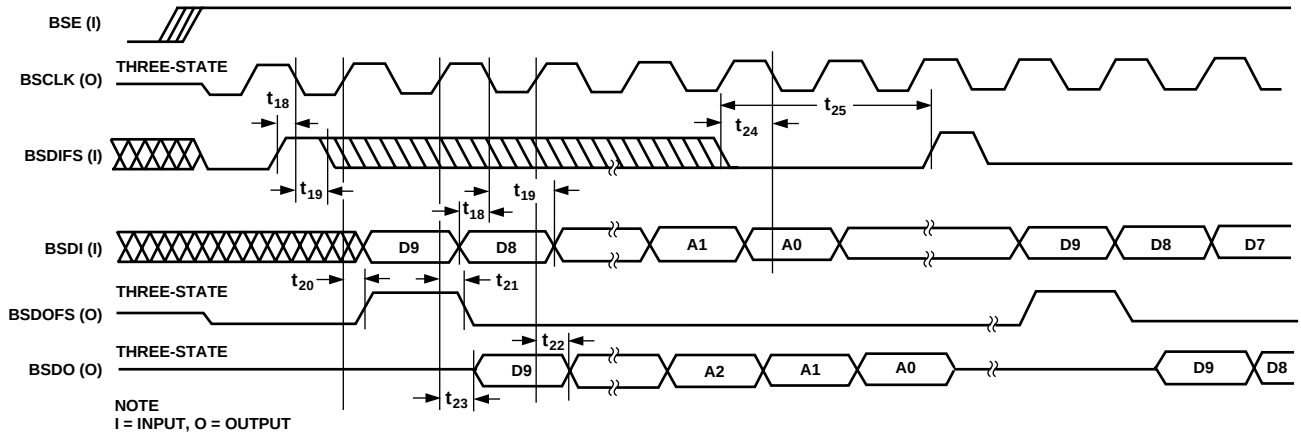


Figure 7. Baseband Serial Port BSPORT

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

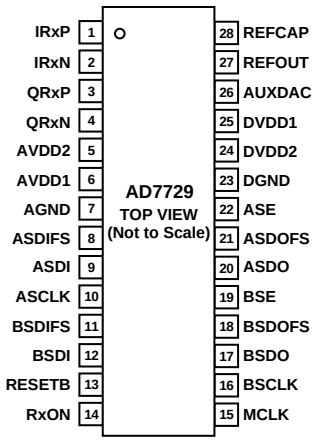
AVDD, DVDD to GND . . . . . –0.3 V to +7 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . –0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND . . . . –0.3 V to AVDD + 0.3 V
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +105°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . +150°C
TSSOP
  θ_{JA} Thermal Impedance . . . . . +122°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C
SOIC
  θ_{JA} Thermal Impedance . . . . . +72°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Options
AD7729AR	–40°C to +105°C	Small Outline IC (SOIC)	R-28
AD7729ARU	–40°C to +105°C	Thin Shrink Small Outline (TSSOP)	RU-28

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7729 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Function
15	MCLK	Master Clock Input. MCLK is driven from a 13 MHz crystal. The active levels for MCLK are determined by the value of DVDD2.
13	RESETB	Active Low Reset Signal. This input resets the entire AD7729 chip, resetting the control registers and clearing the digital filters. The logic input levels (V_{INH} and V_{INL}) for RESETB are determined by the value of DVDD2.
Power Supply		
6	AVDD1	Analog Power Supply Connection for the Rx Section and the Bandgap Reference.
5	AVDD2	Analog Power Supply Connection for the Auxiliary Section.
7	AGND	Analog Ground Connection.
25	DVDD1	Digital Power Supply Connection.
24	DVDD2	Digital Power Supply Connection for the Serial Interface Section. This power supply also sets the threshold voltages for RxON, RESETB and MCLK.
23	DGND	Digital Ground Connection.
Analog Signal and Reference		
1, 2	IRxP, IRxN	Differential Analog Input for I Receive Channel.
3, 4	QRxP, QRxN	Differential Analog Input for Q Receive Channel.
26	AUXDAC	Analog Output Voltage from the 10-Bit Auxiliary DAC AUXDAC. This DAC is used for functions such as Automatic Gain Control (AGC). The DAC possesses a register that is accessible via the ASPORT or BSPORT. The DAC may be individually powered down.
28	REFCAP	A bypass capacitor to AGND of 0.1 μF is required for the on-chip reference. The capacitor should be fixed to this pin.
27	REFOUT	Buffered Reference Output, which has a nominal value of 1.3 V. A bypass capacitor (to AGND) of 0.1 μF is required on this pin.
Auxiliary Serial Port (ASPORT)		
10	ASCLK	Serial Clock used to clock data or control bits to and from the auxiliary serial port (ASPORT). The frequency of ASCLK is programmable and is equal to the frequency of the master clock (MCLK) divided by an integer number.
9	ASDI	Serial Data Input of ASPORT. Both data and control information are input on this pin.
8	ASDIFS	Input Framing Signal for ASDI Serial Transfers.
20	ASDO	Serial Data Output of ASPORT. Both data and control information are output on this pin. ASDO is in three-state when no information is being transmitted, thereby allowing external control.
21	ASDOFS	Output Framing Signal for ASDO Serial Transfers.
22	ASE	ASPORT Enable. When ASE is low, the ASPORT is put into three-state thereby allowing external control of the serial bus.
Baseband Serial Port (BSPORT)		
16	BSCLK	Output serial clock used to clock data or control bits to and from the baseband serial port (BSPORT). The frequency of BSCLK is programmable and is equal to the frequency of the master clock (MCLK) divided by an integer number.
12	BSDI	Serial Data Input of BSPORT. Both data and control information are input on this pin.
11	BSDIFS	Input Framing Signal for BSDI Serial Transfers.
17	BSDO	Serial Data Output of BSPORT. Both data and control information are output on this pin. BSDO is in three-state when no information is being transmitted, thereby allowing external control.
18	BSDOFS	Output Framing Signal for BSDO Serial Transfers.
19	BSE	BSPORT Enable. When BSE is low, the BSPORT is put into three-state thereby allowing external control of the serial bus.
ADCs		
14	RxON	Receive Section Power-On Digital Input. The receive section is powered up by taking pin RxON high. The receive section can alternatively be powered up by programming bit RxON in baseband control register BCRA. When the powering up/down of the receive section is being controlled by pin RxON, bit RxON should equal zero. Similarly, when the powering up/down of the receive section is being controlled by bit RxON, pin RxON should be tied low. The logic input levels (V_{INH} and V_{INL}) for RxON are determined by the value of DVDD2.

TERMINOLOGY

Absolute Group Delay
Absolute group delay is the rate of change of phase versus frequency, dø/df. It is expressed in microseconds.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the DAC or ADC.

Dynamic Range
Dynamic Range is the ratio of the maximum output signal to the smallest output signal the converter can produce (1 LSB), expressed logarithmically, in decibels (dB = $201og_{10}$ (ratio)). For an N-bit converter, the ratio is theoretically very nearly equal to 2^N (in dB, 20Nlog10(2) = 6.02N). However, this theoretical value is degraded by converter noise and inaccuracies in the LSB weight.

Gain Error
This is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out. In the AD7729, gain error is specified for the auxiliary section.

Gain Matching Between Channels
This is the gain matching between the IRx and QRx channel and is expressed in dBs.

Group Delay Between Channels
This is the difference between the group delay of the I and Q channels and is a measure of the phase matching characteristics of the two.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the auxiliary DAC transfer function.

Output Rate
This is the rate at which data words are made available (270.833 kHz).

Offset Error
This is the amount of offset, wrt V_{REF} in the auxiliary DAC and is expressed in mVs.

Output Signal Span
This is the output signal range for the auxiliary DAC section.

Sampling Rate
This is the rate at which the modulators on the receive channels sample the analog input.

Settling Time
This is the digital filter settling time in the AD7729 receive section. On initial power-up or after returning from the power-down mode, it is necessary to wait this amount of time to get useful data.

Signal Input Span
The input signal range for the I and Q channels is biased about V_{REF}.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the receive channel. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for a sine wave is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ dB$$

FUNCTIONAL DESCRIPTION

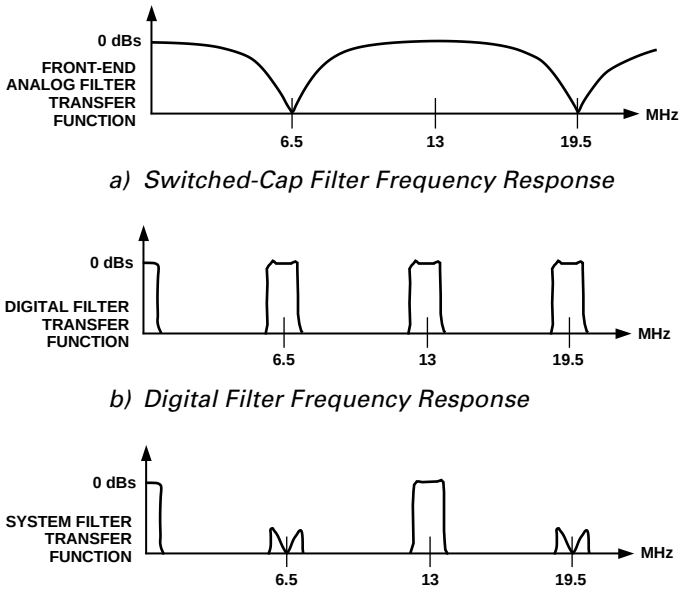
BASEBAND CODEC

Receive Section

The receive section consists of I and Q receive channels, each comprising of a simple switched-capacitor filter followed by a 15-bit sigma-delta ADC. On-board digital filters, which form part of the sigma-delta ADCs, also perform critical system-level filtering. Their amplitude and phase response characteristics provide excellent adjacent channel rejection. The receive section is also provided with a low power sleep mode to place the receive section on standby between receive bursts, drawing only minimal current.

Switched Capacitor Input

The receive section analog front-end is sampled at 13 MHz by a switched-capacitor filter. The filter has a zero at 6.5 MHz as shown in Figure 8a. The receive channel also contains a digital low-pass filter (further details are contained in the following section) which operates at a clock frequency of 6.5 MHz. Due to the sampling nature of the digital filter, the passband is repeated about the operating clock frequency and at multiples of the clock frequency (Figure 8b). Because the first null of the switched-capacitor filter coincides with the first image of the digital filter, this image is attenuated by an additional 30 dBs (Figure 8c), further simplifying the external antialiasing requirements (see Figures 9 and 10).



a) Switched-Cap Filter Frequency Response

b) Digital Filter Frequency Response

c) Overall System Response of the Receive Channel

Figure 8.

The circuitry of Figure 9 implements first-order low-pass filters with a 3 dB point at 338 kHz; these are the only filters that must be implemented external to the baseband section to prevent aliasing of the sampled signal.

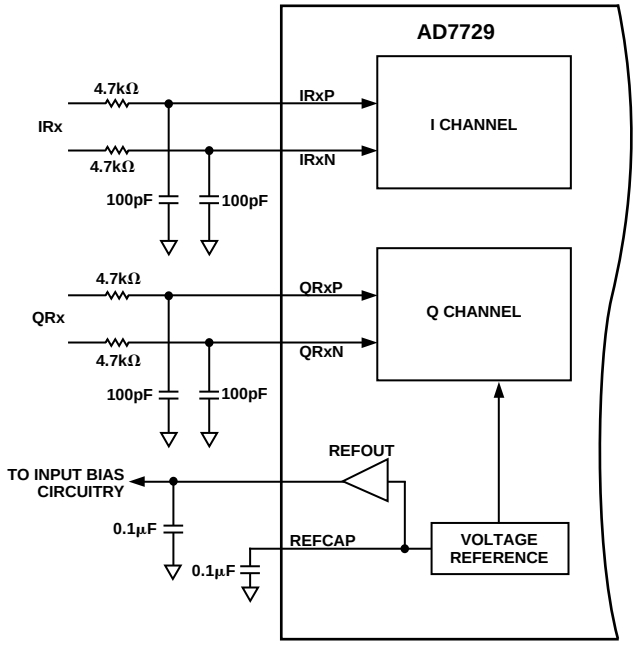


Figure 9. Example Circuit for Differential Input

Figure 10 shows the recommended single-ended analog input circuit.

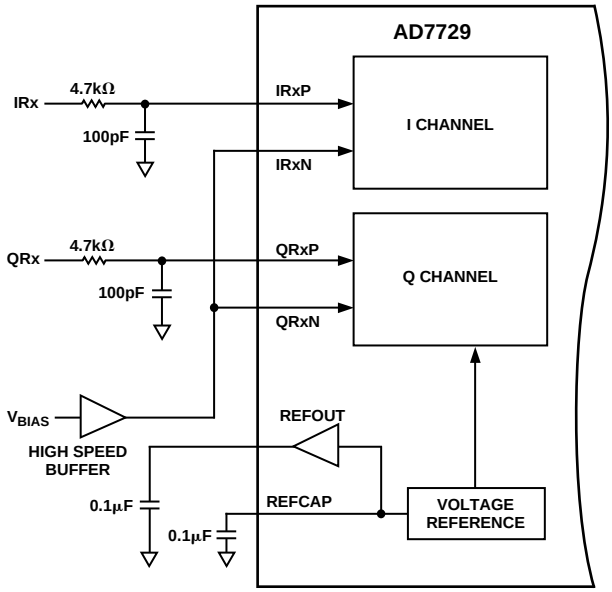


Figure 10. Example Circuit for Single-Ended Input

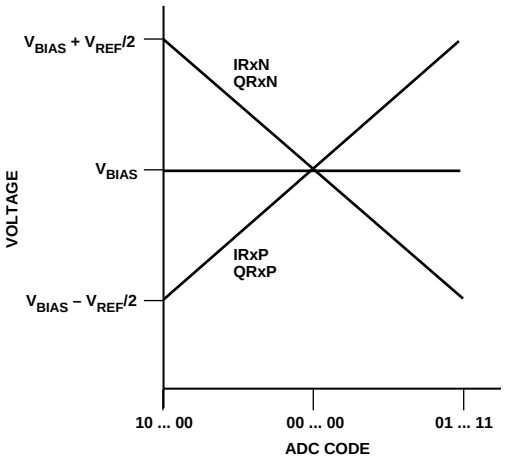


Figure 11. ADC Transfer Function for Differential Operation

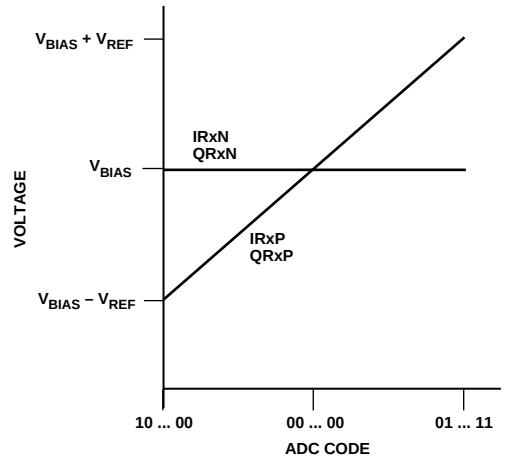


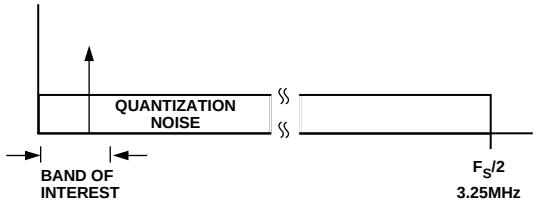
Figure 12. ADC Transfer Function for Single-Ended Operation

Sigma-Delta ADC

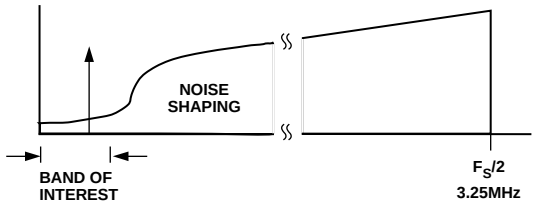
The AD7729 receive channels employ a sigma-delta conversion technique, which provides a high-resolution 15-bit output for both I and Q channels with system filtering being implemented on-chip.

The output of the switched-capacitor filter is continuously sampled at 6.5 MHz (master clock/2), by a charge-balanced modulator, and is converted into a digital pulse train whose duty cycle contains the digital information. Due to the high oversampling rate, which spreads the quantization noise from 0 MHz to 3.25 MHz ($F_S/2$), the noise energy contained in the band of interest is reduced (Figure 13a). To reduce the quantization noise still further, a high order modulator is employed to shape the noise spectrum, so that most of the noise energy is shifted out of the band of interest (Figure 13b).

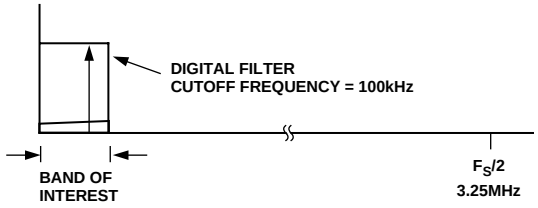
The digital filter that follows the modulator removes the large out-of-band quantization noise (Figure 13c), while converting the digital pulse train into parallel 15-bit-wide binary data. The 15-bit I and Q data, which is in twos complement format, is made available via a serial port.



a) Effect of High Oversampling Ratio



b) Use of Noise Shaping to Further Improve SNR



c) Use of Digital Filtering to Remove the Out-of-Band Quantization Noise

Figure 13.

Digital Filter

The digital filters used in the AD7729 receive section carry out two important functions. Firstly, they remove the out-of-band quantization noise which is shaped by the analog modulator. Secondly, they are also designed to perform system level filtering, providing excellent rejection of the neighboring channels. Digital filtering has certain advantages over analog filtering. Firstly, since digital filtering occurs after the A/D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this. Secondly, the digital filter combines low passband ripple with a steep roll-off, while also maintaining a linear phase response. This is very difficult to achieve with analog filters.

However, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full-scale have the potential to saturate the analog modulator, even though the average value of the signal is within limits. To alleviate this problem, the AD7729 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 100 mV.

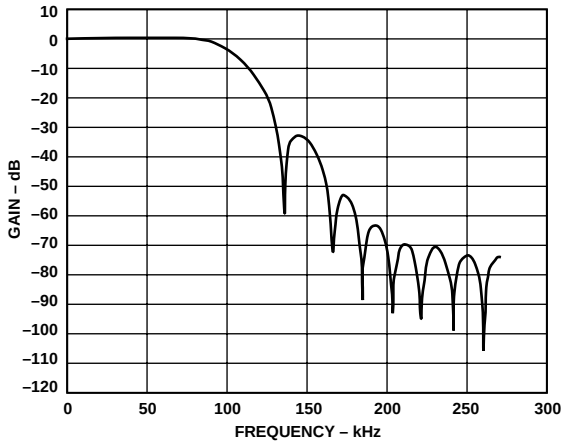


Figure 14. Digital Filter Frequency Response

Filter Characteristics

The digital filter is a 288-tap FIR filter, clocked at half the master clock frequency. The 3 dB point is at 96 kHz.

Due to the low-pass nature of the receive filters, a settling time is associated with step input functions. Output data will not be meaningful until all the digital filter taps have been loaded with data samples taken after the step change. Hence the AD7729 digital filters have a settling time of 44.7 μs ($288 \times 2t_1$).

Receive Offset Calibration

Included in the digital filter is a means by which receive offsets may be calibrated out. Each channel of the digital low-pass filter section has an offset register. The offset register can be made to contain a value representing the dc offset of the preceding analog circuitry. In normal operation, the value stored in the offset register is subtracted from the filter output data before the data appears on the serial output pin. By so doing, dc offsets in the I and Q channels are calibrated out. Autocalibration or user-calibration can be selected. Internal autocalibration will remove internal offsets only while user calibration allows the user to write to the offset register in order to also remove external offsets.

The offset registers have enough resolution to hold the value of any dc offset between ±162.5 mV (1/8th of the input range). Offsets larger than ±162.5 mV will cause a spurious result due to calibration overrange. However, the performance of the sigma-delta modulators will degrade if full-scale signals with more than 100 mV of offset are experienced. The 10-bit offset register represents a twos complement value. The LSB of the offset registers corresponds to Bit 3 of the Rx words while the MSB of the offset registers corresponds to Bit 12 of the Rx words (see Figure 15).

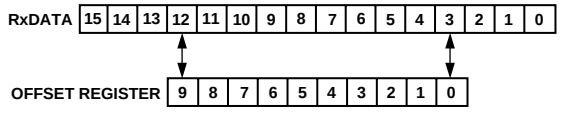


Figure 15. Position of the 10-Bit Offset Word

Receive Offset Adjust: Autocalibration

If receive autocalibration is selected, the AD7729 will initiate an autocalibration routine each time the receive path is brought out of the low power sleep mode. After RxON is asserted, by taking the RxON bit or the RxON pin high, 36 symbol periods are allowed for the analog and digital circuitry to settle. An internal timer then times out a time equal to RxDELAY1.

When RxDELAY1 has expired, the AD7729 offset calibration routine begins, assuming the RxAUTOCAL bit in control register BCRA is equal to 1. If RxAUTOCAL equals zero, no calibration occurs and T2 in Figure 16 equals zero. In internal autocalibration mode, the AD7729 internally disconnects the differential inputs from the input pins and shorts the inputs to measure the resulting ADC offset. In external autocalibration mode, the inputs remain connected to the pins, allowing system offsets along with the AD7729 internal offsets to be evaluated. This is then averaged 16 times to reduce noise and the averaged result is then placed in the offset register. The input to the ADC is then switched back for normal operation and the analog circuitry and digital filter are permitted to settle. This time period is included in $T_{CALIBRATE}$, which equals 40 × 48 MCLK cycles.

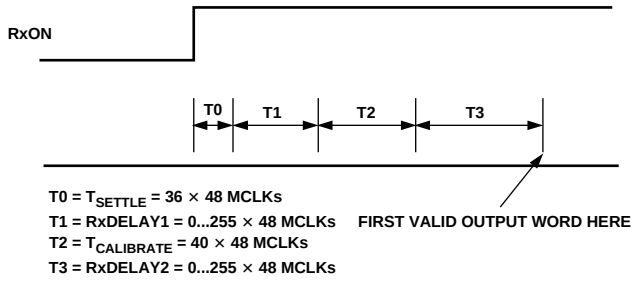


Figure 16. Data Rx Procedure

After calibration is complete, a second timer is started which times out a time equal to RxDELAY2. The range of both RxDELAY1 and RxDELAY2 is 0 to 255 units where each unit equals one bit time. Therefore, the maximum delay time is 255 × 1/270 kHz = 941.55 μs.

As soon as RxDELAY2 has expired, valid output words appear at the output. The Rx data will be 15 bits wide.

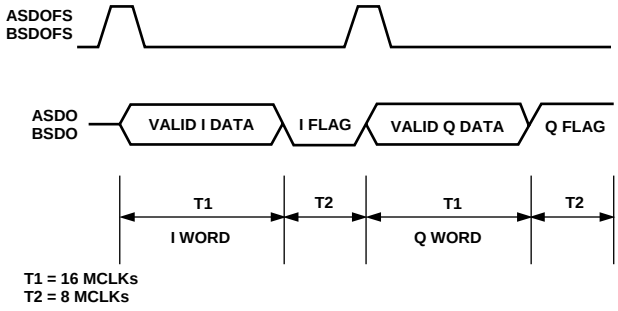


Figure 17. ASDO/BSDO in Rx Mode

Receive Offset Adjust: User Calibration

When user calibration is selected, the receive offset register can be written to, allowing offsets in the IF/RF demodulation circuitry to be calibrated out also. However, the user is now responsible for calibrating out receive offsets belonging to the AD7729. When the receive path enters the low power mode, the registers remain valid. After powering up, the first IQ sample pair is output once time has elapsed for both the analog circuitry to settle and also for the output of the digital filter to settle.

Figure 18 shows a flow diagram for calibration of the receive section.

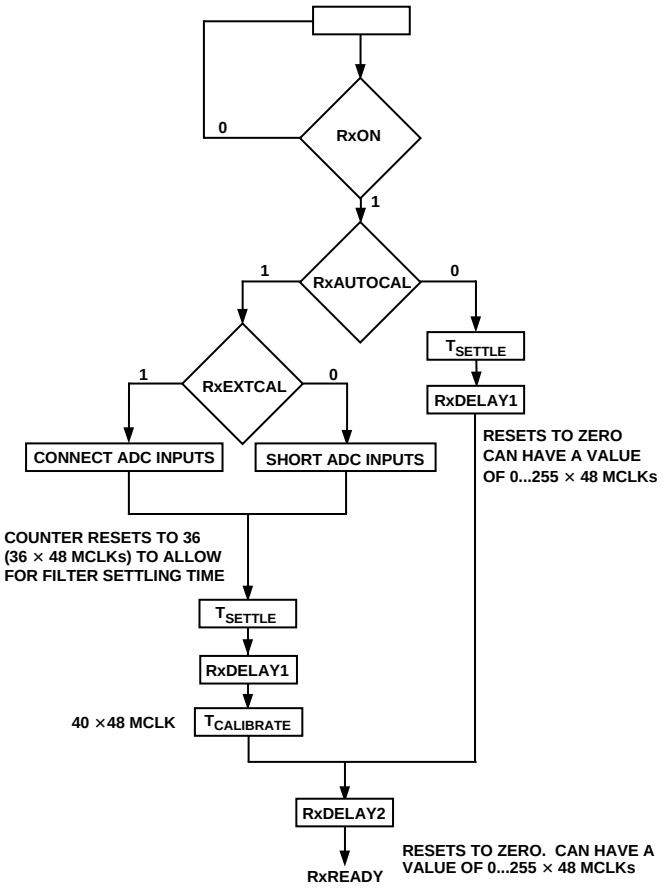


Figure 18. Receive Offset Adjust

Auxiliary Control Functions

The AD7729 also contains an auxiliary DAC that may be used for AGC. This 10-bit DAC consists of high impedance current sources, designed to operate at very low currents while maintaining its dc accuracy. The DAC is buffered by an output amplifier and allows a load of 10 kΩ.

The DAC has a specified output range of $2 \times V_{REFCAP}/32$ to $2 \times V_{REFCAP}$. The analog output is:

$$2\ V_{REFCAP}/32 + (2\ V_{REFCAP} - 2\ V_{REFCAP}/32) \times DAC/1023$$

where *DAC* is the 10-bit digital word loaded into the DAC register.

To perform a conversion, the DAC is first powered up using the AUXDACON bit in control register ACRA. After power-up, 10 µs are required for the AUXDAC circuitry to settle. The AUXDAC is loaded by writing to register AUXDAC. When the AUXDAC is in power-down mode, the AUXDAC register will retain its contents. When the AUXDAC is reset, the AUXDAC register will be set to all zeroes, leading to a voltage of $2 \times V_{REFCAP}/32$ on the analog output.

Voltage Reference

The reference of the AD7729, REFCAP, is a bandgap reference which provides a low noise, temperature compensated reference to the IQ receive ADCs and the AUXDAC. The reference is also made available on the REFOUT pin. The reference has a value of 1.3 V nominal.

When the AD7729 is powered down, the reference can also be powered down. Alternatively, by setting bit LP to 1, the reference remains powered up. This is useful as the power-up time for the receive section and auxiliary converter is reduced since the reference does not require time to power up and settle.

Baseband and Auxiliary Serial Ports (BSPORT and ASPORT)

Both the baseband and auxiliary SPORTs are DSP compatible serial ports which provide access to the 27 on-chip registers as illustrated in Table IV.

Since some registers are accessible over both the auxiliary and baseband SPORTs, the user can decide which registers will be accessible over which SPORT, this feature providing maximum flexibility for the system designer. The user also has the ability to adjust the frequency of the SCLKs in each SPORT, which is useful for power dissipation minimization. Furthermore, it is possible for the user to access all the ADC and AUXDAC control registers over one SPORT, the other SPORT being disabled by tying its serial port enable (SE) low. This feature is useful when the user has only one SPORT available for communication with the AD7729.

Resetting the AD7729

The pin RESETB resets all the control registers. All registers except ASCLKRATE and BSCLKRATE are reset to zero. On reset, ASCLKRATE and BSCLKRATE are set to 4 so that the frequency of ASCLK and BSCLK is MCLK/8. As well as resetting the control registers using the reset pin, these registers can be reset using the reset bits in the baseband and auxiliary registers. All the auxiliary registers can be reset by taking the bit ARESET in control register ACRB high. The baseband registers can be reset by taking bit BRESET in baseband control register BCRA high. This is illustrated in Table IV. After resetting, the bits ARESET and BRESET will reset to zero. A reset using ARESET or BRESET requires 4 MCLK cycles. The registers ARDADDR, BRDADDR, ASCLKRATE, and BSCLKRATE can only be reset using the reset pin RESETB—these registers cannot be reset using the above mentioned bits. A system reset (using BRESET) requires eight MCLK cycles.

The functions of the control register bits are summarized in Table IV to Table X.

Table IV. Baseband and Auxiliary Registers

Name	R/W	Address	Reset
Reserved		000000 (0)	
Reserved		000001 (1)	
Reserved		000010 (2)	
IRxOFFSET	R/W	000011 (3)	BRESET
QRxOFFSET	R/W	000100 (4)	BRESET
Reserved		000101 (5)	
Reserved		000110 (6)	
RxDELAY1	R/W	000111 (7)	BRESET
RxDELAY2	R/W	001000 (8)	BRESET
ARDADDR	R/W	001001 (9)	SRESET
BRDADDR	R/W	001010 (10)	SRESET
Reserved		001011 (11)	
AUXDAC	R/W	001100 (12)	ARESET
Reserved		001101 (13)	
Reserved		001110 (14)	
Reserved		001111 (15)	
Reserved		010000 (16)	
Reserved		010001 (17)	
ACRA	R/W	010010 (18)	ARESET
ACRB	R/W	010011 (19)	ARESET
BCRA	R/W	010100 (20)	BRESET
BCRB	R/W	010101 (21)	BRESET
Reserved		010110 (22)	
Reserved		010111 (23)	
Reserved		011000 (24)	
ASCLKRATE	R/W	011001 (25)	SRESET
BSCLKRATE	R/W	011010 (26)	SRESET

BRESET: can be reset using pin RESETB or bit BRESET.
ARESET: can be reset using pin RESETB or bit ARESET.
SRESET: only the pin RESETB can reset these registers.

Table V. Baseband Control Register A (BCRA)

Bit	Name	Function
BCRA0	MCLKDIV	MCLK Divider. When this bit is set to 0, the internal MCLK has the same value as the external MCLK. When this bit equals 1, the external MCLK is divided by 2 within the AD7729 so that the device operates at half the external clock frequency.
BCRA1	RxAUTOCAL	Selects AutoCal when set to 1 and UserCal when set to 0.
BCRA2	RxEXTCAL	When set to 1, the Rx calibration operates in external mode i.e., the I and Q analog inputs remain connected to the pins during the Rx autocalibration routine.
BCRA3	RxPOWER0	This bit, in conjunction with RxPOWER1, is used to reduce the analog current consumption of the ADCs.
BCRA4	RxPOWER1	This bit, in conjunction with RxPOWER0, is used to reduce the analog current consumption of the ADCs.
BCRA5	Reserved	
BCRA6	RxON	Power-on for the receive section of the AD7729.
BCRA7	BRESET	Baseband Reset.
BCRA8	Reserved	
BCRA9	Reserved	

Table VI. Power Modes for the ADCs

RxPOWER1	RxPOWER0	AIDD1 Reduction
0	0	Reserved
0	1	1/3 (Power Mode 1)
1	0	2/5 (Power Mode 2)
1	1	Reserved

Bits RxPOWER0 and RxPOWER1 are used to reduce the analog current consumption of the ADCs. The part is specified in Power Mode 1. In Power Mode 2, the MCLK needs to be less than 10 MHz. The performance of the part will then be comparable to the performance in Power Mode 1 except that the ADC current will now be less than 9.5 mA.

Table VII. Receive Section Activation

RxON Pin	RxON Bit	Receive Section
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

Table VIII. Baseband Control Register B (BCRB)

Bit	Name	Function
BCRB0	Reserved	
BCRB1	Reserved	
BCRB2	RU	REFOUT Use.
BCRB3	LP	Reference Low Power.
BCRB4	RxSPORTSEL	Selects the SPORT that will provide RxDATA when RxON is asserted. When set to 0, the BSPORT is selected and, when set to 1, the ASPORT is selected.
BCRB5	Reserved	
BCRB6	Reserved	
BCRB7	Reserved	
BCRB8	Reserved	
BCRB9	Reserved	

Table IX. Auxiliary Control Register A (ACRA)

Bit	Name	Function
ACRA0	Reserved	
ACRA1	Reserved	
ACRA2	AUXDACON	Power On for Auxiliary DAC
ACRA3	Reserved	
ACRA4	Reserved	
ACRA5	Reserved	
ACRA6	Reserved	
ACRA7	Reserved	
ACRA8	Reserved	
ACRA9	Reserved	

Table X. Auxiliary Control Register B (ACRB)

Bit	Name	Function
ACRB0	ARESET	Resets the Auxiliary Converter
ACRB1	Reserved	
ACRB2	Reserved	
ACRB3	Reserved	
ACRB4	Reserved	
ACRB5	Reserved	
ACRB6	Reserved	
ACRB7	Reserved	
ACRB8	Reserved	
ACRB9	Reserved	

Writing Over the Baseband (or Auxiliary) SPORT
Writing to and reading from registers via the SPORT involves the transfer of 16 bit words, 10 bits of data and 6 bits of address (with the exception of the Rx data). The frame format is as shown in Figure 19, Bit 15 being the first input bit of the frame. The destination of the 10-bit data is determined by the 6-bit destination address as indicated in Figure 19. Note that some registers are read only and, hence, cannot be written to.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	A5	A4	A3	A2	A1	A0

Figure 19. Write Operation Frame Format

Reading Over the Baseband (or Auxiliary) SPORT
To read the contents of a register, the address of the appropriate register is written to the read address register, ARDADDR or BRDADDR. The time interval between writing to the read address register and the frame synchronization signal becoming active equals 4 MCLK cycles. The read address register is 6 bits wide and Bits D11 to D6 of the input frame are used to write to this register, Bits D12 to D15 being don't cares, as shown in Figure 20. The frame format for reading is identical to that for writing i.e., 10 bits of data followed by 6 address bits corresponding to the source address of the data (with the exception of the Rx data).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	RA5	RA4	RA3	RA2	RA1	RA0	0	0	1	0	1	0

Figure 20. Writing to the Read Address Register (BRDADDR Shown Here)

Receiving RxDATA
The Rx ADC is activated by taking either the RxON bit or the RxON pin high. In this mode, Rx data is automatically output on the SDO pin of the SPORT at a word rate of 270 kHz for each of I and Q, after a delay of T1 + T2 + T3 (see Figure 16). The data format is I followed by Q. The AD7729 will output 16 bits of data, the 15-bit I or Q word, which is in twos complement format, and a flag bit. This flag bit (LSB) distinguishes between the I and Q words, the bit being at 0 when the word being output is an I word while this bit is at 1 when the output is a Q word.

When RxON is taken high, the serial clock will have a frequency of 13 MHz, irrespective of the value in the clock rate register. When the AD7729 is ready to output Rx data, an output frame synchronization signal is generated and the Rx data is automatically output on the SDO pin, an I and Q word being output every 48 MCLK cycles (see Figure 17). Data can be output on the ASPORT or the BSPORT, bit RxSPORTSEL in control register BCRB being used to select the SPORT. Rx data can be received on one SPORT only, the user cannot interchange from one SPORT to the other.

MICROPROCESSOR INTERFACING
The AD7729 has a standard serial interface which allows the user to interface the part to several DSPs. In all cases, the AD7729 operates as the master with the DSP acting as the slave. The AD7729 provides its own serial clock to clock the serial data/control information to/from the DSP.

AD7721-to-ADSP-21xx Interface
Figure 21 shows the AD7729 interface to the ADSP-21xx. For the ADSP-21xx, the bits in the serial port control register should be set up as TFSR = RFSR = 1 (a frame sync is needed for each transfer), SLEN = 15 (16-bit word length), TFSW = RFSW = 0 (normal framing), INVTFS = INVRFS = 0 (active high frame sync signals), IRFS = 0 (external RFS), ITFS = 1 (internal TFS) and ISCLK = 0 (external serial clock).

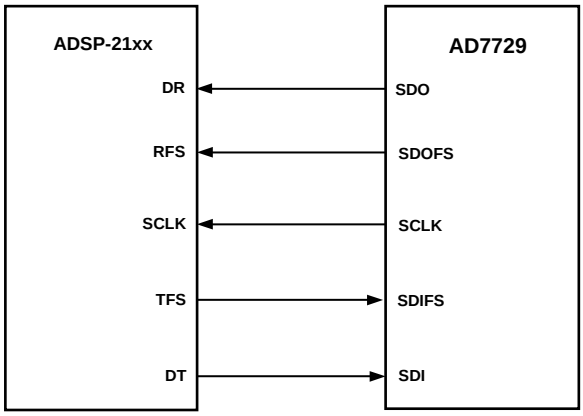


Figure 21. AD7729 to ADSP-21xx Interface

AD7729-to-TMS320C5x Interface

Figure 22 shows the interface between the AD7729 and the TMS320C5x DSP. The TMS320C5x is configured as follows: MCM = 0 (CLKX is an input), TXM = 1 (the transmit frame sync signal is generated by the DSP), FSM = 1 (a frame sync is required for each transfer), FO = 0 (16-bit word length).

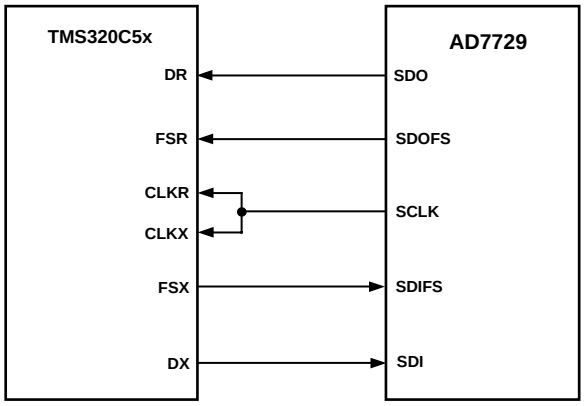


Figure 22. AD7729 to TMS320C5x Interface

Power-Down

Each section of the AD7729 can be powered down. The Rx ADCs and the auxiliary DAC can be powered down individually by setting the appropriate bits in the control registers. When each section is powered up, time must be allowed so that the analog and digital circuitry can settle and, also, time is needed for the reference REFCAP to power up. To reduce this power-up time, Bit LP can be set to 1 so that when the ADCs and DAC are powered down, the reference REFCAP remains powered up by setting Bit LP to 1. Therefore, because the reference is powered up, the time needed for circuitry to settle when a section is powered up is reduced considerably since the reference does not require time to power up and settle.

When all sections of the AD7729 are powered down, including the reference, the MCLK is stopped after 64 clock periods following the detection of the low power state. The MCLK reactivates when the AD7729 is communicated with, i.e., the SPORTs are activated, RxON is taken high, etc.

Grounding and Layout

Since the analog inputs to the AD7729 are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent Common-Mode Rejection of the part will remove common-mode noise on these inputs. The analog and digital supplies of the AD7729 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. The digital filters following the ADCs will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filters also remove noise from the analog inputs provided the noise source does not saturate the analog modulator. However, because the resolution of the AD7729 ADCs is high and the noise levels from the AD7729 are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7729 should be designed so that the analog and digital sections are separated and confined to certain sections of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD7729 is the only device requiring an AGND-to-DGND connection, the ground planes should be connected at the AGND-and-DGND pins of the AD7729. If the AD7729 is in a system where multiple devices require AGND-to-DGND connections, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7729.

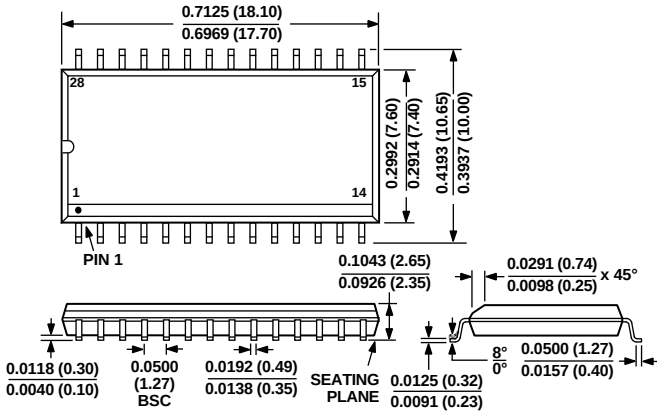
Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7729 to avoid noise coupling. The power supply lines to the AD7729 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply lines. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the other side.

Good decoupling is important when using high speed devices. All analog and digital supplies should be decoupled to AGND and DGND respectively with 0.1 μF ceramic capacitors in parallel with 10 μF tantalum capacitors. To achieve the best from these decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply voltage is used to drive both the AVDD and DVDD of the AD7729, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD7729 and AGND and the recommended digital supply decoupling capacitors between the DVDD pins and DGND.

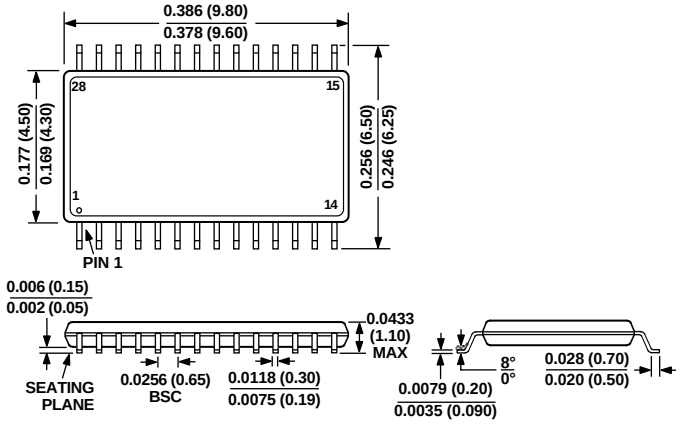
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Small Outline (SOIC)
(R-28)



28-Lead Thin Shrink Small Outline (TSSOP)
(RU-28)



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