User's Manual

RZ/G1M

User's Manual: Hardware

for Rich Graphics Applications
RZ/G Series

ARM®

Specifications of Individual RZ/G Series Product

Renesas Electronics
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(2012.4)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of hardware, pin assignments, pin multiplexing, and pin function controller.

For the rest of the sections on other on-chip peripheral functions, see the RZ/G Series User's Manual: Hardware.

> Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

> The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

We provide the following three types of user's manual for RZ/G series products.

Make sure to refer to the latest versions of these documents.

Document Type	Description	Document Title	Document No.
User's manual for specifications of individual RZ/G series product	Overview of hardware, pin assignments, pin multiplexing, and pin function controller	RZ/G1M User's Manual: Hardware	R01UH0626EJ0100 Rev.1.00 (This user's manual)
User's manual for specifications common to RZ/G series products	Hardware specifications (address map, general-purpose I/O port pins, clock, reset, core functions, graphics, video processing, sound processing, and network modules, serial interfaces, storage, timers, other on-chip peripheral functions, testing, and debugging) and descriptions of operation	RZ/G Series User's Manual: Hardware	R01UH0543EJ0100 Rev.1.00
User's manual for electrical characteristics	Electrical characteristics of the RZ/G series products	Provided as separate technical information.	

2. Notation of Numbers and Symbols

Bit notation: Bits are shown in high-to-low order from left to right.

Number notation: Binary numbers are given as B'XXXX, hexadecimal numbers are given as H'XXXX, and decimal numbers are given as XXXX.

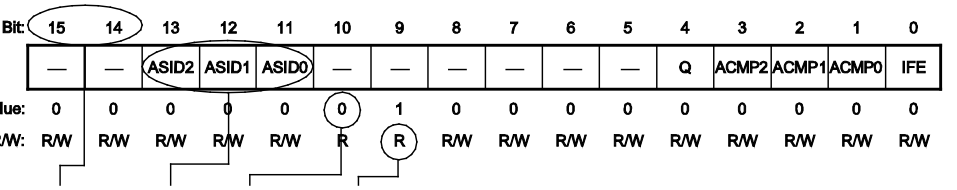
Signal notation: A number sign (#) after the name indicates that a signal or pin is active-low, unless otherwise specified.

Example: PRESET#

3. Register Notation

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings.

[Bit Chart]



[Table of Bits]

(1) (2) (3) (4) (5)

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved
14	—	0	R	These bits are always read as 0.
13 to 11	ASID2 to ASID0	All 0	R/W	Address Identifier These bits enable or disable the pin function.
10	—	0	R	Reserved This bit is always read as 0.
9	—	1	R	Reserved This bit is always read as 1.
	—	0		

Note: The bit names and sentences in the above figure are examples, and have nothing to do with the contents of this manual.

(1) Bit
Indicates the bit number or numbers.
In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.

(2) Bit name
Indicates the name of the bit or bit field.
When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[3:0]).
A reserved bit is indicated by "–".
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.

(3) Initial value
Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.
0: The initial value is 0.
1: The initial value is 1.
–: The initial value is undefined

(4) R/W
For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible.
The notation is as follows:

R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable.
However, writing is only performed to flag clearing.
R/WC0: The bit or field is readable and writable. Writing 0 to the bit initializes the bit.
Writing 1 to the bit is ignored.
R/WC1: The bit or field is readable and writable. Writing 1 to the bit initializes the bit.
Writing 0 to the bit is ignored.
R: The bit or field is readable.
"R" is indicated for all reserved bits. When writing to the register, write the value under Initial Value in the bit chart to reserved bits or fields.
W: The bit or field is writable.
Note that values read from write-only bits are not guaranteed, unless they are specified in the chart of bits.

(5) Description
Describes the function of the bit or field and specifies the values for writing.

Contents

1. Overview

1.1 Introduction

The RZ/G1M is that features the basic functions for Rich Graphics Applications.

The RZ/G1M includes:

- Two 1.5-GHz ARM® Cortex®-A15 MPCore cores,
- Memory controller for DDR3L-SDRAM (DDR3L-1600) with 32 bits × two channels,
- Three-dimensional graphics engines,
- Video processing unit,
- Sound processing unit,
- SD card host interface,
- USB3.0 and USB2.0 interfaces,
- PCI Express interface,
- Serial ATA interface, and
- CAN interface.

Also, a full implementation of the extremely expandable and Internal AXI bus has been adopted for the RZ/G1M.

This bus structure is optimized for maximum system performance, leading to the realization of high-performance and cost-effective premium in-vehicle infotainment systems.

Notes: 1. ARM is a registered trademark and Cortex is a trademark of ARM Limited. All other brands or product names are the property of their respective holders.

1.2 System Configuration Diagram

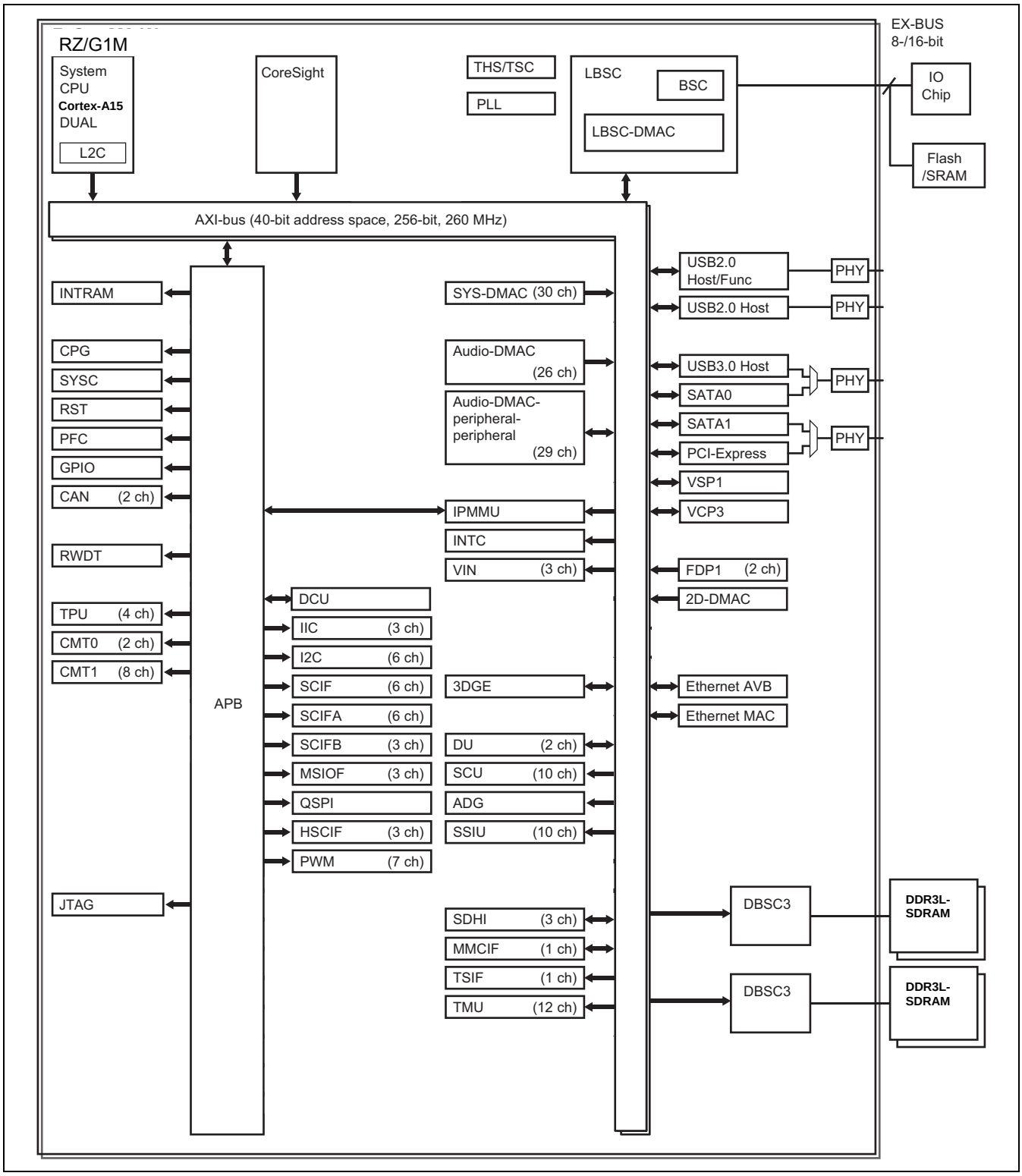


Figure 1.1 RZ/G1M System Configuration

1.3 List of Specifications

1.3.1 ARM Core

Item	Description
System CPU Cortex-A15	• ARM Cortex-A15 Dual MPCore 1.5 GHz • L1 I/D cache 32/32 Kbytes, L2 cache 1 Mbyte • NEON™/VFPv4 supported • Security extension supported
ARM debugger (CoreSight)	• CoreSight system compliant • JTAG/SWD I/F supported • CoreSight PTM-A15 supported (each CPU) • CoreSight ETR 16 Kbytes for program flow trace • CoreSight ETR 4 Kbytes for system trace

1.3.2 CPU Core Peripherals

Item	Description
Operating clock pulse generation circuit (CPG)	• Generates the clocks from external clock (EXTAL1). — Maximum Cortex-A15 clock: 1.5 GHz — Maximum AXI-bus clock: 260 MHz — Maximum SDRAM bus clock: 800 MHz (DDR3L-1600), 666 MHz (DDR3L-1333) — Maximum media clock: 260 MHz — Maximum peripheral clock (HPϕ): 130 MHz • System-CPU shut down mode control supported • Module-standby mode supported • Includes module reset registers to control reset operation of individual on-chip peripheral modules
System controller (SYSC)	• Shuts down and restores power to target modules. Target modules: — Cortex-A15 (with independent shutting down of CPUs 0, 1, and SCU+L2$)*1 — 3DGE*2 Notes: 1. SCU and L2$ are treated as one power-domain. When CPU is working, SCU+L2$ can't be powered off. 2. Although 3DGE is a target of power-shutdown, version/revision is different from H1's 3DGE. Please refer to 3DGE's specification.
Reset (RST)	• Includes one reset-signal external output port for external modules • Includes Boot Address Register etc.
Pin function controller (PFC)	• Setting multiplexed pin functions for LSI pins Function of the RZ/G1M pin selectable by setting the registers in the PFC module. • Module selection Enable and disable the functions of RZ/G1M LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module. • Pull-up control for each LSI pin On/off of the pull-up resistor on each LSI pin can be controlled by setting the registers in the PFC module. • Control of SDIO functions SDIO functions, including the driving ability of pins for the SDIF, can be controlled by setting registers of the PFC.
General-purpose I/O (GPIO)	• General-purpose I/O ports: 244 • Supports GPIO interrupts.
Thermal sensor (THS/TSC)	• Single channel of thermal sensor • Programmable 4 temperature level for the sensor, to indicate the temperature level • Selectable operation (Interrupt/Reset) when the temperature reaches programmed

1.3.3 External Bus Module

Item	Description
Local bus state controller (LBSC)	• EX-BUS interface: max. 16-bit bus • Frequency: 65 MHz • External area divided into several areas and managed — Allocation to space of area 0, area 1, and area 6 or allocation to space of area 0 only is selected at startup time. — Area 0 supports 128-Mbyte memory space (startup mode). — Space of area 6 is divided into up to six areas (capacity of each area variable) and managed — I/F settings, bus width settings, and wait state insertion are possible for each area • SRAM interface — Wait states can be inserted through register settings — Period of waiting is set in cycle unit, and the maximum value is 15. — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • Burst ROM interface — Wait states can be inserted through register settings — Number of bursts can be set through register settings — Connectable bus widths: 16 bits or 8 bits • Byte-control SRAM interface (available with areas 1 and 6 only) — Byte-control SRAM interface — Wait states can be inserted through register settings — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • ATA interface (two ports) — Wait states can be inserted through register settings — Supports PIO modes 0 through 4 — Supports multi-word modes 0 through 2 — Supports Ultra DMA modes 0 through 4 (Ultra ATA66) — Ready timeout detection (detection time (ns) = EX-BUS operating frequency (ns) × 100 clock cycles) • Supports external buffer enable/direction control

Item	Description
LBSC-DMAC	• Three channels • Address space: Physical address space • Transfer direction: Peripheral to memory (AXI-bus), memory (AXI-bus) to peripheral • Data packing for peripheral read data: Memory write data length is selectable as transfer data length to memory side. • Transfer data length: Peripheral (APB-bus) side: 1, 2, 4 bytes Memory (AXI-bus) side: 4 or 16 (channel 2), 32 (channel 0 and 1) bytes • Transfer burst length: 1, 8 (transfer with a burst length of 8 supported only for LBSCDMAC00, 01) • Number of transfers — Maximum number of transfers: 16 M (16,777,216 transfers), 64M (67,108,864 transfers), (64 M transfers supported only for LBSC-DMAC00) — Minimum number of transfers: One • Address mode: Dual address mode • Transfer modes: Single transfer mode, continuous transfer mode • Transfer end interrupt: Occurs at the end of the number of transfers specified in the register
External bus controller for DDR3-SDRAM (DBSC3)	• Two channels (32-bit bus mode) • DDR3L-SDRAM can be connected directly. • Memory size: Up to 8 Gbytes (8-Gbit memory × 8) • Data bus width: 32 bits × 2 • Auto-refresh/self-refresh/partial array self-refresh supported • Deep-power-down mode supported • Auto precharge mode/bank active mode • DDR back up supported (only 32-bit × 1 backup)
Memory connections	DDR3-SDRAM compliant to JEDEC JESD79-3E Supports from 512-Mbit to 8-Gbit memory unit configurations 32-bit DDR3L-1600 (four units with 8-bit width)

1.3.4 Internal Bus Module

Item	Description
AXI-bus	• On-chip main bus — Bus protocol : AXI3 with QoS control — Frequency: 260 MHz — Bus width: 256 bits/128 bits • On-chip CPU & GPU main bus — Corelink™ CCI-400 Cache Coherent Interconnect - r0p3 — Bus protocol: AMBA®4 ACE™ and ACE-Lite™ — Frequency: 520 MHz — Bus width: 128 bits

Item	Description
Direct memory access controller for system (SYS-DMAC)	• 30 channels for ARM domain • Address space: 4 Gbytes on architecture • Data transfer length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes and 64 bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Direct memory access controller for Audio (Audio-DMAC)	• 26 channels for Audio domain • Address space: 4 Gbytes on architecture • Data transfer length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes and 64 bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Direct memory access controller (Audio-DMAC-Peripheral-Peripheral)	Audio-DMAC (for transfer from Peripheral to Peripheral) • 29 channels for audio domain • Data transfer length: longword (4 bytes) • Transfer count: Transfer count is not specified (DMA transfer is made from the transfer-start to transfer-stop settings.) • Transfer request: Selectable from on-chip audio peripheral module request • Priority: round-robin mode • Interrupt request: not supports interrupt request to CPU at the end of data transfer
IPMMU	An IPMMU is a memory management unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks.

Item	Description	
Interrupt controller (INTC)	INTC-SYS	— 10 interrupt pins which can detect external interrupts — Fall/rise/high level/low level detection is selectable — On-chip peripheral interrupts: Priority can be specified for each module — Max. 384 shared peripheral interrupts supported — 16 software interrupts that have been generated and 6 private peripheral interrupts supported — 32-level priority selectable — Trust Zone supported

1.3.5 Local Memory

Item	Description
INTRAM	• RAM0 of 72 Kbytes • RAM1 of 4 Kbytes • RAM2 of 256 Kbytes

1.3.6 Graphics Units

Item	Description
3D graphics engine (3DGE)	• Imagination Technologies PowerVR SGX544MP2 • Max. Freq. 520 MHz • Most comprehensive IP core family and roadmap in the industry • USSE2 delivers twice the peak floating point and instruction throughput of Series5 USSE • YCbCr and color space accelerators for improved performance • Upgraded PowerVR Series5XT shader-driven tile-based deferred rendering (TBDR) architecture • Support for all industry standard mobile and desktop graphics APIs and operating systems

Item	Description	
Display unit (DU)	Display channel	Two independently controllable channels
	Screen size and number of composite planes	• Maximum screen size: 4095 × 2047 • Number of planes specifiable: 8 planes Note that possibility number of combined display depends on DCLK; 1-plane @DCLK > 75 MHz 2-plane @75 MHz ≥ DCLK > 38 MHz 3-plane @38 MHz ≥ DCLK
	CRT scanning method	Non-interlaced, interlaced sync, interlaced sync & video
	Synchronization method	Master, TV sync
	Internal color palette	Includes four color palette planes which can display 256 of 260 thousands colors at the same time.
	Digital RGB	• One output channel • Output on rising and falling edges of the synchronizing signal (resolution for the same display) • 8-bit precision for each RGB color
	Blending ratio settings	Number of color palette planes with blending ratio: 4
	Dot clock	Switchable between external input and internal clock
	Color management	• γ correction, gain correction • Applies correction of color (skin color adjustment and color correction set in memory) in terms of color phase, brightness, and chromaticity for a specified range of colors or for the full range of colors
	Interface	• LVDS output: Four lanes × single channel (two lanes × 2) • RGB888 × 1
	LVDS interface (1ch)	• Output: compliant with TIA/EIA-644; five pairs of differential output (four pairs of data and one pair of clock) • Operating frequency: Dotclk 148.5 MHz • Selectable 8 output formats
De-compression unit (DCU)	• De-compression to row picture data from compressed data by Run-length method • Input data format: Compressed data by Run-Length method (ARGB8888, RGB888, RGB565, RGBA4444, RGBA5551, and A8) • Output data format: Row data (ARGB8888, RGB888, RGB565, RGBA4444, RGBA5551, and A8) • 2 interrupt sources: Conversion finished, and Check sum error • Including DMAC (DCU_DMAC)	

Item	Description	
Video input (VIN)	Input data format	• 8-, 10-, or 12-bit YCbCr422 (CbYCrY format) • 16-bit YCbCr422 (8-bit (Y) + 8-bit (CbCr) format) • 20-bit YCbCr422 (10-bit (Y) + 10-bit (CbCr) format) • 24-bit YCbCr422 (12-bit (Y) + 12-bit (CbCr) format) • 18-bit RGB666 • 24-bit RGB888
	Clipping function	Up to 2048 × 2048
	Horizontal scaling	Uses a 9-tap multi-phase filter. Up to two times, but only scaling down is possible for HD1080i or HD720P data.
	Vertical scaling	Scaling by linear interpolation Up to three times, but only scaling down is possible for HD1080i or HD720P data.
	Output format	RGB-565, ARGB-1555, YCbCr422, RGB888 (for channels 0 and 1), YC separation, and extraction of the Y component

1.3.7 Video Processing

Item	Description
Video signal processor 1 (VSP1)	The VSP1 is the successor IP of Renesas' VIO6-IP series, and has the following features. (1) Supports various data formats and conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying (2) Full HD video processing — Up and down scaling with arbitrary scaling ratio — Super resolution processing — Blending of four picture layers and raster operations (ROPs) (3) Full HD picture quality/color correction with 1D/3D look up table (LUT) — Dynamic γ correction and gain correction — Correction of color (to adjust skin tones or colors in memory) — Hue, brightness, and saturation adjustment — 1D histogram (4) Direct connection to display module — Display unit (DU) supported

Item	Description
Video processing unit (VCP3)	The VCP3 is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g., H.264/AVC, MPEG-4, MPEG-2 and VC-1. This IP (Intellectual Property) is a multi codec that processes the frame or each field by controlling software for VCP3 executed on host CPU. The VCP3 has the following features: • Support for multiple codecs — H.264/MPEG-4 AVC HP (High Profile) and MVC SHP (Stereo High Profile) encoding and decoding — H.262/MPEG-2 MP (Main Profile) decoding — MPEG-4 ASP (Advanced Simple Profile) decoding — VC-1 SP/MP/AP (Simple, Main, Advanced Profile) decoding — H.263 Baseline decoding — VP8 decoding • Support for HDTV resolutions — 1920 pixels × 1080 lines × 60 frames/second × single channel — Maximum performance will change with securable bus bandwidth. • Data handling on a picture-by-picture basis — Encodes/decodes data one picture (frame or field) at a time. • High picture quality — Supports the H.264 high-efficiency coding tools (CABAC, 8 × 8 frequency conversion, and quantization matrix). — High-efficiency motion vector detection by a combination of discrete search and trace search — Highly efficient real-time intra-prediction by Prediction from Original Image (POI) — Optimal-mode selection by Rate-Distortion (RD) cost evaluation — Picture quality control based on activity analysis results which match visual models • Low power dissipation — Dynamically disables the clocks for the entire VCP3. — Dynamically disables the clocks for individual submodules. • Includes its own dedicated 64-KByte cache
Fine display processor 1 (FDP1)	The FDP1 is the de-interlacing module which converts the interlaced video to progressive video, and has the following features. (1) Supports various data formats — Input: YCbCr444/422/420 — Output: YCbCr444/422/420 and RGB/αRGB (2) Full HD video processing performance (3) High image quality de-interlacing algorithm — Motion adaptive de-interlacing — Accurate still detection — Diagonal line interpolation (DLI)

Item	Description
Image extraction direct memory access controller (2D-DMAC)	• Supports conversion between various RGB formats. • Image extraction function: Capable of extracting an image and storing it as a separate image in the RAM. • Image rotation/reversal function: Reverses an image vertically/horizontally or rotates it by 90°/270°. • Simple scaling function: Capable of scaling an image two times in the X or Y direction. • Format conversion • Supports conversion from RGB to RGB and from YCbCr to YCbCr.

1.3.8 Sound Interface

Item	Description	
Sampling rate converter unit (SCU)	Overall specification	• Includes ten SRC modules — Supports the quality suitable for audio sound (THD+N -132dB): six modules — Supports the quality suitable for voice sound (THD+N -96dB): four modules • The SRC module is capable of correcting phase change and delay (timing jitter) generated during data transfer over external memories or external devices. • The channel count conversion unit (CTU), mixer (MIX), and digital mute and volume function (DVC) can be used on two fixed output channels.
	Sampling rate conversion (SRC)	• Capable of asynchronous sampling rate conversion • Supports resolutions up to 24 bits • Two kinds of filter type for SRC. — Supports the quality suitable for audio sound (THD+N -132dB): Realized the filter by passband -1dB@0.4575FS, cutoff -18dB@0.5FS. — Supports the quality suitable for voice sound (THD+N -96dB): Realized the filter by passband -1dB@0.4561FS, cutoff -72dB@0.5FS (Characteristics of each filter is written in the equivalent/up-sampling cases). • Automatically generates antialiasing filter coefficients • For monaural to eight-channel sound sources
	Channel count conversion unit (CTU)	• Downmixing and splitter functions — Conversion of eight input channels into four output channels — Conversion of six input channels into two output channels — Conversion of two input channels into four sets of two output channels — Conversion of one input channel into eight sets of one output channel — No conversion
	Mixer (MIX)	• Mixing (adds) two to four sources into one • Ratio for adding sources is selectable • Ratio is dynamically changeable • Mixing with volume ramp is available (ramp period is selectable)

Item	Description	
	Digital volume and mute function (DVC)	• Volume control function including digital volume, volume ramp, and zero-crossing mute • The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute, or -120 to 18 dB) • The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment • The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2 • The zero-crossing mute function silences the sound at the zero-crossing point of the audio data
Serial sound interface unit (SSIU)	Overall specification	• Includes ten SSI modules functioning as interfaces with external devices. — Supports short and long formats — Supports TDM format (six modules of ten modules can be used for this function) • Up to four independent stereo sound sources in a TDM format can be distributed to each course. Up to four independent stereo sound sources can be combined output in TDM format.
	Serial sound interface (SSI)	• Operating mode: non-compressed mode (Not support compressed mode) • Supports versatile serial audio formats (I2S/left justified/right justified) • Supports master/slave functions • Programmable word clock, bit clock generation functions • Multichannel format functions (up to four channels) • Supports 8-/16-/18-/20-/22-/24-/32-bit data formats • Supports TDM mode • Supports WS continue mode • The DMA controller or interrupts control the transfer of data to and from the SSI module. • Supports short and long frames for monaural data (valid data lengths are 8 and 16 bits) • Up to nine independent clock signals can be input.
Audio clock generator (ADG)	Selection or division of audio clock signals	

1.3.9 Storage

Item	Description
USB2.0 host & function module (USB2.0)	• Two channels (Host only 1 channel/Host-Function 1 channel selected)* • PHY integrated • USB Host (EHCI/OHCI) 2LINK • Compliance with USB2.0 • USB Function 1LINK • Compliance with USB2.0 (High-Speed) • Interrupt request • Internal dedicated DMA Note: * A USB2.0 PHY is used as USB3.0 host HS/FS. USB2.0: Two channels (HS/FS/LS) / USB2.0 + USB3.0: Single channel (SS/HS/FS)
USB 3.0 host module (USB3.0)	• USB 3.0 host 1 ch* • Supports SS/HS/FS/LS. xHCI • Not support FUNCTION and OTG Note: * A USB2.0 PHY is used as USB3.0 HOST HS/FS. USB2.0: Two channels (HS/FS/LS) / USB2.0 + USB3.0: Single channel (SS/HS/FS)
Serial-ATA	• Serial ATA Standard Rev.3.1 supported • 3.0-Gbps (Gen2) transfer rate supported — Single-channel PHY for USB3.0 and SATA (channel 0) — Single-channel PHY for PCIEC and SATA (channel 1)
SD host interface (SDHI)	• Three channels — Interface 0: Support SDR104 class transfer rate at max. 97.5 Mbytes/s@ 195 MHz, and SDXC. Does not support CPRM. — Interfaces 1 and 2: Support SDR50 class transfer rate at max. 48 Mbytes/s@ 97.5 MHz, and SDXC. Does not support CPRM. • Supports SD memory/SDIO interface (1-/4-bit SD buses). • Error check function: CRC7 (command/response), CRC16 (data) • Card detection function • Supports write protection
Multi-media card interface (MMCIF)	• Single channel • MMC 4.41 base • eMMC controllable • Data bus: 1/4/8-bit MMC mode (not support SPI mode) • Support block transfer (not support stream transfer) • Block size in multi-block transfer: 512 bytes

1.3.10 Network

Item	Description
CAN interface (CAN)	• Two channels • Supports CAN specification 2.0B • ISO-11898-1 compliant • Maximum bit rate: 1 Mbps • Message box — Normal mode: 32 receive-only mailboxes and 32 mailboxes for transmission/reception — FIFO mode: 32 receive-only mailboxes and 24 mailboxes for transmission/reception, 4-stage FIFO for transmission, and 4-stage FIFO for reception • Reception — Data frame and remote frame can be received. — Selectable receiving ID format — Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • Acceptance filter — Mask can be enabled or disabled for each mailbox. • Transmission — Data frame and remote frame can be transmitted. — Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) — Selectable ID priority mode or mailbox number priority mode • Sleep mode for reducing power consumption
PCI-Express Controller (PCIEC)	• PCI Express Base Specification Revision 2.0 • Single channel • PHY integrated
Ethernet AVB	• Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions • Supports transfer at 1000 Mbps and 100 Mbps • Magic packet detection • Supports Reception Filtering to separate streaming frames from different sources • Supports interface conforming to IEEE802.3 PHY GMII (Gigabit Media Independent Interface) and MII (Media Independent Interface)
Ethernet MAC	• IEEE802.3u MAC (Ether) function • Supports transfer at 10 and 100 Mbps • Flow control conforming to IEEE802.3x or back pressure system • Supports interface conforming to IEEE802.3u • Magic packet detection • Includes DMAC • Supports RMII (Reduced Media Independent Interface)

1.3.11 Timer

Item	Description
Watchdog timer (RWDT)	• Internal 16-bit watchdog timer operated by RCLK • Programmable overflow time-period: more than 1 hour count capable

Item	Description
Timer pulse unit (TPU)	• 4-channels • 16-bit timers • Each channel outputs PWM
Compare match timer 0 (CMT0)	• 32-bit timer, two channels (16 bits/32 bits can be selected) • Source clock: RCLK clock • Compare match function provided • Interrupt requests
Compare match timer 1 (CMT1)	• 48-bit timer, eight channels (16 bits/32 bits/48 bits can be selected) • Source clock: RCLK/system clock • Compare match function provided • Interrupt requests
Timer unit (TMU)	• 4 sets of 3-channel 32-bit timer • Auto-reload type 32-bit down counter • Internal prescaler • Interrupt request • Two channels for input capture

1.3.12 Peripheral Module

Item	Description
I2C bus interface (IIC)	• Single channel for DVFS (open drain type IO buffer) • Two channels for general purpose • Supports single master transmission/reception • Interrupt request • DMAC request
Multi-master I2C bus interface (I2C)	• Five channels for 3.3-V LVTTL buffers and single channel for Open drain type IO buffer • Philips I2C bus interface method supported • Master/slave functions • Multi-master functions • Transfer rate up to 400 kbps supported • Programmable clock generation from the system clock
Serial communication interface with FIFO (SCIFA)	• Six channels • Internal 64-byte transmit/receive FIFOs • High-speed UART • Internal prescaler • Clock synchronous serial communications possible • Support edge selection function • Interrupt request, DMAC request and DMA multi-Byte transfer supported • Asynchronous mode (modem control is enabled) • Clock synchronous mode
Serial communication interface with FIFO (SCIFB)	• Three channels • Internal 256-byte transmit/receive FIFOs • High-speed UART • Internal prescaler • Clock synchronous serial communications possible • Support edge selection function • Interrupt request, DMAC request and DMA multi-Byte transfer supported • Asynchronous mode (modem control is enabled) • Clock synchronous mode

Item	Description	
Serial communication interface with FIFO (SCIF)	Overall specification	• Six channels • Asynchronous, clock-synchronized modes • Asynchronous serial communication mode The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats. — Data length: 7 bits or 8 bits — Stop bits: 1 bit or 2 bits — Parity: Even/odd/none — Receive error detection: Parity, framing, and overrun errors — Break detection: A break is detected when a framing error lasts for more than 1 frame length at space 0 (low level). When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR). • Clock synchronous serial communication mode The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication. — Data length: 8 bits — Receive error detection: Overrun errors • Full-duplex communication capability The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception. • On-chip baud rate generator, enabling any bit rate to be selected The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock. • Eight interrupt sources The SCIF has eight types of interrupt sources: receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently. • DMA data transfer When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.

Item	Description
Clock-synchronized serial interface with FIFO (MSIOF)	• Three channels • Max. speed: 26 Mbps • Internal 64-byte transmit FIFOs/internal 256-byte receive FIFOs • Supports master and slave modes • Internal prescaler • Supports serial formats: IIS, SPI (master and slave modes) • Interrupt request, DMAC request
QSPI	• Single/Dual/Quad-SPI: serial slave transfer enabled • Supports master mode • SPICLK clock rate: 1 to 4080 in master mode; Max. 78 MHz
High-speed serial communication interface with FIFO (HSCIF)	• Three channels • Asynchronous serial communication mode • Capable of full-duplex communication • On-chip baud rate generator, enabling any bit rate to be selected • Eight interrupt sources • DMA data transfer • Modem control functions (HRTS and HCTS) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • A receive data ready (DR) or a timeout error (TO) can be detected during reception.
PWM timer (PWM)	• Seven channels • High-level width (10 bits) of PWM output can be set. • High-level periods (10 bits) of PWM can be set. • Periods in the range from two to $2^{24} \times 1024$ cycles of the Pϕ clock can be set. • Continuous pulse or single pulse output selectable
TSIF	• Single channel • Serial data input • Support for TS data transfer by DMA auto request • Acquisition of TS packets Filters 67 kinds of PIDs (Packet ID) in total (The PID values of PAT and CAT packets are fixed. For PCR, video, and audio packets, the PID values are predefined).
Boot Function (BOOT)	• System startup with selectable boot mode at power-on reset • Program downloaded to internal memory (LRAM) • Autorun function for the downloaded program

1.3.13 Others

Item	Description
JTAG	JTAG interface for CoreSight
Process	28-nm Si-CMOS
Package	FC-BGA2727-831

1.4 Power Supply Voltages and Temperature Range

- Power supply voltage (typ.)
  1.8 V: (ETM, SD, MMC, SATA, PCI Express, USB3.0, LVCMOS I/F, Xtal, JTAG, Trace and RST)
  1.03 V: (core)
  1.35V: (DDR3-I/O SSTL mode: DDR3L)
  3.3 V: (Others)

- Temperature range
  Tc = –40°C to +105°C
  Ta = –40°C to +85°C

2. Area Map

See section 2, Area Map in the RZ/G Series User's Manual: Hardware.

3. Pin Assignment

3.1 Top View (Left)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VDDQ_M1	M1DQ31	M1DQ29	M1DM3	M1DQ28	VDDQ_M1	M1DQ17	M1DQ21	VSS	M1DQ3	M1DM0	VDDQ_M1	M1DQ8	M1DQ9	M1DQ15	M0A8
B	M1A0	VSS	M1DQ24	VSS	M1DQ30	M1DQ16	VSS	M1DQ19	M1DQ23	VSS	M1DQ1	M1DQ0	VSS	M1DQ11	M1DQ13	M0A14
C	M1BA1	M1A12	VSS	M1DQ26	M1DQ27	VSS	M1DM2	M1DQ18	VSS	M1DQ6	M1DQ4	VSS	M1DM1	M1DQ12	VDDQ_M0	M0BA1
D	M1A5	VSS	M1RAS#	VSS	M1DQ25	M1DQ22	VSS	M1DQ20	VSS	M1DQ5	M1DQ7	M1DQ2	VSS	M1DQ10	M1DQ14	M0A5
E	M1A4	M1A2	M1WE#	M1CAS#	VSS	M1DQS3#	M1DQS3	M1DQS2	M1DQS2#	VSS	M1DQS0#	M1DQS0	M1DQS1#	M1DQS1	VSS	M0A12
F	VDDQ_M1A	M1CS0#	VSS	M1ODT0	M1CKE0	VSS	VDDQ_M1	VSS	VSSQ_M1DPLL2	VDDQ_M1DPLL2	VSS	VSSQ_M1DPLL1	VDDQ_M1DPLL1	VSS	VSS_CPGPLL0	VDD_CPGPLL0
G	M1CS1#	VSS	M1CKE1	VSS	M1RESET#	VDDQ_M1BKUP	VSS	M1VREFDQ1	VSSQ_M1DPLL3	VDDQ_M1DPLL3	VSS	VSSQ_M1DPLL0	VDDQ_M1DPLL0	M1VREFDQ0	VSS_CPGPLL1	VSS
H	M1A7	M1A1	M1BA2	M1ODT1	M1CK0#	VSS	M1VREFCA	VSS	VSS	VDDQ_M1	VSS	VSS	VDDQ_M1	VSS	VDD_CPGPLL1	M0ZQ
J	VSS	M1A9	M1BA0	VSS	M1CK0	VDDQ_M1A	M1BKPRST#	VSS								
K	M1A11	M1A6	M1A15	VSS	M1CK1#	VSSQ_M1MPLL	VSSQ_M1APLL	VSS								
L	M1A13	VDDQ_M1A	M1A10	VSS	M1CK1	VDDQ_M1MPLL	VDDQ_M1APLL	M1ZQ				VDD	VDD	VSS	VDD_DVFS	VSS
M	M1A8	M1A14	M1A3	VSS	VSS	VSS	VSS	VDDQ_M1A			VSS	VSS	VDD	VSS	VDD_DVFS	VSS
N	EX_CS1#	EX_CS2#	BS#/MD10	RD/WR#	WE0#/MD6	WE1#/MD4	DACK0/MD7	VSS			VDD	VDD	VSS	VSS	VDD_DVFS	VSS
P	A25	A24	A23	A22	A21	A20	A19/MD14	VCCQ			VSS	VSS	VSS			
R	CS1#/A26	A18	A17	A16	A15/MD20	A14/MD19	A13/MD21	VSS			VDD_DVFS	VDD_DVFS	VDD_DVFS			
T	CS0#	A12	A11	A9	A8	A6	A0	VCCQ			VSS	VSS	VSS			
U	CLKOUT	VSS	EX_WAIT0	DREQ0	PRESETOUT#	AVS1	AVS2	VCCQ			VDD_DVFS	VDD_DVFS	VDD_DVFS			
V	EX_CS0#	RD#/MD12	EX_CS3#/MD9	EX_CS4#	EX_CS5#/MD8	A10/MD22	A7/MD27	VSS			VSS	VSS	VSS			
W	D15	D14	A5	A4/MD24	A3/MD13	A2/MD23	A1/MD28	VSS			VDD	VDD	VSS	VSS	VDD_DVFS	VSS
Y	D13	D12	D11	D10	D9	D8	D7	VSS			VSS	VSS	VDD	VSS	VDD_DVFS	VSS
AA	D6	D5	D4	D3	D2	D1	D0	VSS			VDD	VSS	VDD	VSS	VDD_DVFS	VSS
AB	VI0_CLKENB	VI0_HSYNC#	VI0_VSYNC#	VI0_DATA0/VI0_B0	VI0_DATA1/VI0_B1	VI0_DATA2/VI0_B2	VI0_DATA4/VI0_B4	VCCQ								
AC	VI0_CLK	VI0_FIELD	VI0_DATA3/VI0_B3	VI0_DATA5/VI0_B5	VCCQ18	VI0_DATA6/VI0_B6	VI0_DATA7/VI0_B7	VCCQ								
AD	VI0_G0	VI0_G1	VI0_G2	VI0_G3	VI0_G4	VI0_G5	VI0_G7	VSS	VSS	VCCQ	VCCQ	VSS	VCCQ_SD3	VSS	VCCQ_SD2	VCCQ_SD0
AE	VI0_R0	VSS	VI0_R1	VI0_R2	VI0_R3	VI0_G6	VSS	DU1_EXHSYNC/DU1_HSYNC/MD3	DU1_DB4	DU1_DG7	DU1_DR7	DU1_DR6	SD3_DATA3	SD3_DATA2	SD2_DATA2	SD0_DATA2
AF	VI1_HSYNC#	VI1_VSYNC#	VI0_R4	VI0_R5	VI0_R6	VSS	ETH_MDC	DU1_EXVSYNC/DU1_VSYNC/MD2	DU1_DB3	DU1_DG6	DU1_DG5	DU1_DR5	SD3_DATA1	SD2_WP	SD2_DATA1	SD0_DATA1
AG	VI1_CLK	VCCQ	VI1_CLKENB	VI0_R7	VSS	ETH_TX_EN	ETH_TXD0	DU1_EXODDF/DU1_ODDF/DISP/CDE	DU1_DB2	DU1_DB7	DU1_DG4	DU1_DR4	SD3_DATA0	SD2_DATA3	SD2_DATA0	SD0_DATA0
AH	VI1_DATA1	VI1_FIELD	VI1_DATA0	VSS	ETH_RXD0	ETH_LINK	STP_ISD_0	DU1_DISP/MD1	DU1_DB1	DU1_DB6	DU1_DG3	DU1_DR3	SD3_CMD	SD2_CMD	SD0_DATA3	SD0_CMD
AJ	VI1_DATA2	VI1_DATA3	VSS	VI1_DATA7	ETH_TXD1	ETH_MAGIC	STP_ISEN_0	DU1_CDE/MD0	DU1_DB0	DU1_DB5/MD11	DU1_DG2	DU1_DR2	SD3_WP	SD2_CD	SD0_CD	SD0_WP
AK	VI1_DATA4	VSS	VI1_DATA6	ETH_CRS_DV	VCCQ	VSS	STP_ISSYNC_0	STP_IVCXO27_0	VSS	DU1_DOTCLKOUT1	DU1_DG1	DU1_DR1	SD3_CD	VSS	VSS	VSS
AL	VSS	VI1_DATA5	ETH_MDIO	ETH_RX_ER	ETH_RXD1	ETH_REFCLK	STP_OPWM_0	STP_ISCLK_0	DU1_DOTCLKIN	DU1_DOTCLKOUT0	DU1_DG0	DU1_DR0	SD3_CLK	SD2_CLK	SD0_CLK	NMI
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

3.2 Top View (Right)

17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
M0A13	M0A11	M0CS1#	VDDQ_ M0	M0A4	M0A2	VSS	M0DQ9	M0DQ15	VDDQ_ M0	M0DQ0	M0DM0	M0DQ3	M0DQ7	VDDQ_ M0	A
M0A6	M0A9	VSS	M0CS0#	M0A7	M0A1	M0DQ8	M0DQ14	VSS	M0DQ12	M0DQ4	VSS	M0DQ5	VSS	M0DQ19	B
VSS	M0A10	M0CKE1	VSS	M0BA0	M0CAS#	VSS	M0DQ10	M0DM1	VSS	M0DQ6	M0DQ1	VSS	M0DQ17	M0DQ21	C
M0A3	M0A15	VSS	M0ODT0	M0BA2	M0RAS#	VSS	M0DQ11	VSS	M0DQ13	M0DQ2	VSS	M0DQ23	VSS	M0DM2	D
M0A0	M0ODT1	M0RESET#	VDDQ_ M0	M0WE#	VSS	M0DQS1	M0DQS1#	M0DQS0#	M0DQS0	VSS	M0DQ22	M0DQ18	M0DQ20	M0DQ16	E
VSS	VSS	VSS	M0CKE0	VSS	VDDQ_ M0DPLL1	VSSQ_ M0DPLL1	VSS	VDDQ_ M0	VSS	M0DQS2	M0DQ24	VSS	M0DQ26	VDDQ_ M0	F
M0CK1	M0CK1#	M0CK0#	M0CK0	VDDQ_ M0APLL	VDDQ_ M0DPLL0	VSSQ_ M0DPLL0	M0VREF DQ0	VSS	VDDQ_ M0	M0DQS2#	VSS	M0DM3	VSS	M0DQ25	G
VDDQ_ M0	M0BKP RST#	VDDQ_ M0BKUP	VSS	VSSQ_ M0APLL	VDDQ_ M0	VSS	VSS	M0VREF DQ1	VSS	M0DQS3#	M0DQ28	M0DQ30	M0DQ27	M0DQ31	H
							VDDQ_ M0	VSSQ_ M0DPLL2	VSSQ_ M0DPLL3	M0DQS3	VSS	VSS	M0DQ29	VSS	J
							VSS	VDDQ_ M0DPLL2	VDDQ_ M0DPLL3	VSS	VCCQ18_ MLBP	VCCQ33_ MLBP	VSS	NC	K
VDD_ DVFS	VSS	VDD	VSS	VDD			VDDQ_ M0	VDD_CPG PLL2	VDD_CPG PLL3	VSS	NC	NC	VSS	NC	L
VDD_ DVFS	VSS	VDD	VSS	VSS			VSS	VSS_CPG PLL2	VSS_CPG PLL3	VSS	NC	NC	VSS	NC	M
VDD_ DVFS	VSS	VSS	VDD	VDD			VCCQ	VDD_ MLBPPLL0	VDD_ MLBPPLL1	VTHREF0	VCCQ18_ MLBP	VCCQ33_ MLBP	VSS	NC	N
		VSS	VSS	VSS			VSS	VSS_ MLBPPLL0	VSS_ MLBPPLL1	VTHSENS E0	HCTS0#	HRX0	HTX0	HSCK0	P
		VDD_ DVFS	VDD_ DVFS	VDD_ DVFS			VCCQ	HRTS0#	SIM0_RST /MDT1	SIM0_D	SIM0_CLK /MDT0	GPS_MAG	GPS_SIGN	GPS_CLK	R
		VSS	VSS	VSS			VSS	SPEEDIN	MSIOF0_ SS2	MSIOF0_ SS1	MSIOF0_ RXD	MSIOF0_ TXD	MSIOF0_ SYNC	MSIOF0_ SCK	T
		VDD_ DVFS	VDD_ DVFS	VDD_ DVFS			VCCQ	VSS_ MLBPLL	VDD_ MLBPLL	NC	HRTS1#	HCTS1#	VSS	HSCK1	U
		VSS	VSS	VSS			VSS	HRX1	HTX1	SSI_ SDATA1	SSI_WS1	SSI_ SDATA0	SSI_ WS0129	SSI_ SCK0129	V
VDD_ DVFS	VSS	VSS	VDD	VDD			VCCQ	SSI_ SDATA3	SSI_WS34	SSI_ SCK34	SSI_ SDATA2	SSI_WS2	SSI_SCK2	SSI_SCK1	W
VDD_ DVFS	VSS	VDD	VSS	VSS			VSS	SSI_ SDATA7	SSI_ SDATA5	SSI_WS5	SSI_SCK5	SSI_ SDATA4	SSI_WS4	SSI_SCK4	Y
VDD_ DVFS	VSS	VDD	VSS	VDD			VCCQ	SSI_ SDATA8	SSI_ WS78	SSI_ SCK78	VCCQ18	SSI_ SDATA6	SSI_WS6	SSI_SCK6	AA
							AVDD	VSS	IRQ7	IRQ8	IRQ9	SSI_SDAT A9	SSI_WS9	SSI_SCK9	AB
							AVSS	AVDD	VSS	IRQ6	IRQ5	IRQ4	AUDIO_ CLKB	VSS	AC
VSS	VCCQ18	VCCQ_ ISO	DU0_ LVDS_ PLL1_VCC	DU0_ LVDS_ PLL1_VSS	VDDQ_ LVDS	VSS_ SATA1	VSS_ SATA0	AVSS	VD181	USB1_ OVC	IRQ3	IRQ2	AUDIO_ CLKC	AUDIO_ CLKA	AD
ACK	TCK	PRESET#	DU0_ LVDS_ CLK_P	VSS	VDDQ_ LVDS	VSS_ SATA1	VSS_ SATA1	VSS_ SATA0	AVSS	VD331	USB1_ PWEN	IRQ1	IRQ0	AUDIO_ CLKOUT/ MD5	AE
BSMODE	TMS	TRST#	DU0_ LVDS_ CLK_N	VSS	VDDQ_ LVDS	VDDD_ SATA1	VDDA_ SATA1	VSS_ SATA0	VSS_ SATA0	AVSS	VD331	VSS	USB0_ OVC	USB0_ PWEN	AF
DU0_DOT CLKIN	MPMD1	MPMD0	VSS	DU0_ LVDS_ CH3_N	DU0_ LVDS_ CH3_P	VDDD_ SATA1	VDDA_ SATA1	VDDD_ SATA0	VDDA_ SATA0	VSS_ SATA0	AVSS	USB0_ RREF	VSS	USB0_ DP	AG
TDI	I2C5_SDA	IIC3_SDA	VSS	VSS	VSS	VSS	VDDD_ SATA1	VDDD_ SATA0	VDDD_ SATA0	VDDA_ SATA0	VSS_ SATA0	USB1_ RREF	VSS	USB0_ DM	AH
TDO	I2C5_SCL	IIC3_SCL	DU0_ LVDS_ CH2_P	DU0_ LVDS_ CH2_N	DU0_ LVDS_ CH0_N	DU0_ LVDS_ CH0_P	VSS_ SATA1	CICREF N1_SATA	CICREF P1_SATA	CICREF N0_SATA	CICREF P0_SATA	VSS_ SATA0	VSS	USB1_ DP	AJ
VSS	VSS	VSS	VSS	VSS	VSS	VSS_ SATA1	VSS_ SATA1	VSS_ SATA1	VSS_ SATA1	VSS_ SATA0	VSS_ SATA0	VSS_ SATA0	VSS_ SATA0	USB1_ DM	AK
XTAL	EXTAL	USB_ XTAL	USB_ EXTAL	DU0_ LVDS_ CH1_P	DU0_ LVDS_ CH1_N	RIDP1_ SATA	RIDN1_ SATA	TODP1_ SATA	TODN1_ SATA	RIDP0_ SATA	RIDN0_ SATA	TODP0_ SATA	TODN0_ SATA	VSS_ SATA0	AL
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

: Multiplexed pin that function is selected by the Pin Function Controller (PFC) register and mode pin setting.

3.3 Mode Pin Settings

Input fixed values for the MPMD0, MPMD1, and BSMODE pins. These values cannot be changed after power is supplied. The values of pins MD0 to MD14, MD19 to MD24, MD27, MD28, MDT0 and MDT1 are input upon power-on reset using the PRESET# pin. Power-on reset results in switching to a different function.

Note that this LSI does not have pins MD15 to MD18, MD25, and MD26.

Legend: "0" means logic low level input, "1" means logic high level input.
"—" means either "0" or "1", but its level must be fixed.

MPMD1	MPMD0	MP Mode Switching
0	0	Normal operation
0	1	Setting prohibited
1	0	Setting prohibited
1	1	Setting prohibited

BSMODE	JTAG Pin Operating Mode Switching
0	Normal operation
1	Operates in boundary scan mode When PRESET# is at low level, pin IO control is disabled.

MD0	Free-Running Mode or Step-Up Mode
0	Free-running mode
1	Step-up mode

MD3	MD2	MD1	Boot Device Selection
0	0	0	Area 0 boot (boot from the external mask ROM)
0	1	0	QSPI (16-Kbyte transfer at 48.75 MHz)
0	0	1	Reserved
0	1	1	Reserved
1	0	0	QSPI (16-Kbyte transfer at 39 MHz)
1	0	1	Reserved
1	1	0	QSPI (4-Kbyte transfer at 39 MHz)
1	1	1	Reserved

MD4	Area Division
0	Area 0: 64 Mbytes
1	Area 0: 128 Mbytes

MD5	Reserved, fixed to 1

MD7	MD6	Master Boot Processor Selection
0	0	Cortex-A15 boot
0	1	Setting prohibited
1	0	Setting prohibited
1	1	Setting prohibited

MD8	EXBUS Area 0 Data Bus Width
0	8-bit
1	16-bit

MD9	EXTAL/XTAL Pin Setting
0	Inputs an external clock to the EXTAL pin
1	Connects a crystal resonator to the EXTAL/XTAL pin

MD12	MD10	MD21, 20	MD11	MDT [1:0]	JTAG	SDHI2	SDHI3
0	0	00	—	—	Boundary scan	Normal	Normal
		01	—	—	Reserved	Reserved	Reserved
		10	0	—	CoreSight debug port	Normal	Normal
			1	00		Reserved	Normal
				01		Reserved	Normal
				10		Normal	Reserved
				11		Normal	Reserved
		11	0	—	Reserved	Normal	Normal
			1	00		CoreSight debug port	Normal
				01	Reserved	Reserved	Reserved
				1-			
	1	00	—	—	Reserved	Reserved	Reserved
		01	0	—	CoreSight debug port	Normal	Normal
			1	00		Reserved	Normal
				01		Reserved	Normal
				1-	Reserved	Reserved	Reserved
		10	0	—	Reserved	Normal	Normal
			1	—	Reserved	Reserved	Reserved
		11	—	—	Reserved	Reserved	Reserved
1	—	—	—	—	Reserved	Reserved	Reserved

Note: For normal operation, set MD12, MD10 and MD[21:20] to 0000 and TRST# pin must be pulled-down (MD11 and MDT[1:0]: don't care, but which level must be fixed at a power-on reset).

MD14	MD13	Internal Clock	External Clock	PLL1	PLL0	PLL3/ MD19: DDR3-1600	PLL3/ MD19: DDR3-1333
0	0	15 MHz	× 1/1*1	× 208*3	× 172	× 106 (VCO = 1590 MHz)	× 88 (VCO = 1320 MHz)
0	1	20 MHz	× 1/1*1	× 156*3	× 130	× 80 (VCO = 1600 MHz)	× 66 (VCO = 1320 MHz)
1	0	26 MHz	× 1/2*2	× 240*3	× 200	× 122 (VCO = 1586 MHz)	× 102 (VCO = 1326 MHz)
1	1	30 MHz	× 1/2*2	× 208*3	× 172	× 106 (VCO = 1590 MHz)	× 88 (VCO = 1320 MHz)

Notes: 1. Do not input the clock frequency of less than 12 MHz when the input division ratio is × 1/1.
2. Do not input the clock frequency of less than 24 MHz when the input division ratio is × 1/2.
3. VCO = 3120 MHz

MD19	DDR3-SDRAM Bus Clock
0	DDR3L-1600 mode
1	DDR3L-1333 mode

MD28	MD27	MD22	DDR 64 Bits or 32 Bits	Remarks
0	0	0	DDR 64 bits × single channel	Reserved (setting prohibited)
		1	DDR 64 bits × single channel	Reserved (setting prohibited)
	1	0	—	Reserved (setting prohibited)
		1	DDR 64 bits × single channel	Reserved (setting prohibited)
1	0	0	DDR 32 bits × single channel	Reserved (setting prohibited)
		1	DDR 32 bits × single channel	Reserved (setting prohibited)
	1	0	DDR 32 bits × single channel	
		1	DDR 32 bits × two channels	(initial)

MD23	ComboPHY1 Function Selection
0	SATA-0
1	USB3.0

MD24	ComboPHY0 Function Selection
0	SATA-1
1	PCI express

4. Pin Multiplexing

4.1 List of Multiplexed Pin Functions

Table 4.1 lists the multiplexed pin functions of the RZ/G1M.

The default pin function of each pin after power-on reset is "Function 1" respectively, unless otherwise mentioned in each table note.

For details on pin function control, refer to section 3.3, Mode Pin Settings and section 5, Pin Function Controller (PFC).

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Mode Pin (only for corresponding pin): Mode pin is assigned, Function n (n=1, 2, 3, ...)/GPIO: Module or GPIO, Module: Module abbreviation except for GPIO, Pin Name: Module or GPIO pin name, I/O: Input or output

"Reserved" in module column is assigned internal function and "-" in module column is undefined, they must not be specified.

During POR: Pin state during power-on reset (PRESET# pin input is low-level).

V/|IOH|: Pin voltage and output drive current (nominal value respectively).

Pull-up: Internal pull-up control function is available or not from a power-on reset.

"On": Pull-up control function is available and default state is pulled-up.
(No.212, ACK pin is available for internal pull-down function.)
"Off": Pull-up control function is available and default state is not pulled-up.
"-": Pull-up control function is not available.
For details of pull-up control function, refer to PUPR0 through PUPR7 registers in section 5, Pin Function Controller (PFC).

I: Input, I(S): Schmitt input, IO: Input and output, IO (OD): Input and open drain output, O: Output, P: Power supply pin.

(H)/(L)/(X)/(Z) in I/O row: Default pin state (only for default pin, except for clock or analog output)

H: High level output, L: Low level output, X: Undefined value output, Z: High impedance

Notes:

1. All power supply pins and ground pins must be supplied suitable power supply and GND respectively.
2. All mode pins must be used during power-on reset.
3. Pin name that has an identifier for example "XXXX_B", "XXXX_C" etc. are mirror pins of the XXXX pin. Only one pin out of the XXXX pin or its mirror pins can be used. When using mirror pin, specify the suite of pin that has the same identifier for the selected module. It is prohibited to use a suite of pin as mixed two or more identifiers for a selected module.
4. Do not use any pins that of unused modules.
5. Unused pins must be handled as described in section 4.3, Handling of Unused Pins.
6. The terminal state after the reset cancellation has been described as a premise not using the BKPRST (BKRST#=H(fixed)).

Table 4.1 List of Multiplexed Pin Functions

DBSC3 channel 0 (No.1 to 60): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
1	DBSC3 channel 0	X
F20	M0CKE0	1.35V/-
	O(L)	-
2	DBSC3 channel 0	X
C19	M0CKE1	1.35V/-
	O(L)	-
3	DBSC3 channel 0	P
G16	VSS	-
	P	-
4	DBSC3 channel 0	I
H18	M0BKPRST#	1.35V/-
	I	-
5	DBSC3 channel 0	H
E19	M0RESET#	1.35V/-
	O(H to L)	-
6	DBSC3 channel 0	X
G20	M0CK0	1.35V/-
	O	-
7	DBSC3 channel 0	X
G19	M0CK0#	1.35V/-
	O	-
8	DBSC3 channel 0	X
G17	M0CK1	1.35V/-
	O	-
9	DBSC3 channel 0	X
G18	M0CK1#	1.35V/-
	O	-
10	DBSC3 channel 0	H
B20	M0CS0#	1.35V/-
	O(H)	-
11	DBSC3 channel 0	H
A19	M0CS1#	1.35V/-
	O(H)	-
12	DBSC3 channel 0	L
D20	M0ODT0	1.35V/-
	O(L)	-
13	DBSC3 channel 0	L
E18	M0ODT1	1.35V/-
	O(L)	-
14	DBSC3 channel 0	IO
H16	M0ZQ	-
	IO	-
15	DBSC3 channel 0	H
E21	M0WE#	1.35V/-
	O(H)	-
16	DBSC3 channel 0	H
D22	M0RAS#	1.35V/-
	O(H)	-
17	DBSC3 channel 0	H
C22	M0CAS#	1.35V/-
	O(H)	-
18	DBSC3 channel 0	L
E17	M0A0	1.35V/-
	O(L)	-
19	DBSC3 channel 0	L
B22	M0A1	1.35V/-
	O(L)	-
20	DBSC3 channel 0	L
A22	M0A2	1.35V/-
	O(L)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
21	DBSC3 channel 0	L
D17	M0A3	1.35V/-
	O(L)	-
22	DBSC3 channel 0	L
A21	M0A4	1.35V/-
	O(L)	-
23	DBSC3 channel 0	L
D16	M0A5	1.35V/-
	O(L)	-
24	DBSC3 channel 0	L
B17	M0A6	1.35V/-
	O(L)	-
25	DBSC3 channel 0	L
B21	M0A7	1.35V/-
	O(L)	-
26	DBSC3 channel 0	L
A16	M0A8	1.35V/-
	O(L)	-
27	DBSC3 channel 0	L
B18	M0A9	1.35V/-
	O(L)	-
28	DBSC3 channel 0	L
C18	M0A10	1.35V/-
	O(L)	-
29	DBSC3 channel 0	L
A18	M0A11	1.35V/-
	O(L)	-
30	DBSC3 channel 0	L
E16	M0A12	1.35V/-
	O(L)	-
31	DBSC3 channel 0	L
A17	M0A13	1.35V/-
	O(L)	-
32	DBSC3 channel 0	L
B16	M0A14	1.35V/-
	O(L)	-
33	DBSC3 channel 0	L
D18	M0A15	1.35V/-
	O(L)	-
34	DBSC3 channel 0	L
C21	M0BA0	1.35V/-
	O(L)	-
35	DBSC3 channel 0	L
C16	M0BA1	1.35V/-
	O(L)	-
36	DBSC3 channel 0	L
D21	M0BA2	1.35V/-
	O(L)	-
37	DBSC3 channel 0	P
G21	VDDQ_M0APLL	-
	P	-
38	DBSC3 channel 0	P
H21	VSSQ_M0APLL	-
	P	-
39	DBSC3 channel 0	Z
A27	M0DQ0	1.35V/-
	IO(Z)	-
40	DBSC3 channel 0	Z
C28	M0DQ1	1.35V/-
	IO(Z)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
41	DBSC3 channel 0	Z
D27	M0DQ2	1.35V/-
	IO(Z)	-
42	DBSC3 channel 0	Z
A29	M0DQ3	1.35V/-
	IO(Z)	-
43	DBSC3 channel 0	Z
B27	M0DQ4	1.35V/-
	IO(Z)	-
44	DBSC3 channel 0	Z
B29	M0DQ5	1.35V/-
	IO(Z)	-
45	DBSC3 channel 0	Z
C27	M0DQ6	1.35V/-
	IO(Z)	-
46	DBSC3 channel 0	Z
A30	M0DQ7	1.35V/-
	IO(Z)	-
47	DBSC3 channel 0	Z
E26	M0DQS0	1.35V/-
	IO(Z)	-
48	DBSC3 channel 0	Z
E25	M0DQS0#	1.35V/-
	IO(Z)	-
49	DBSC3 channel 0	Z
A28	M0DM0	1.35V/-
	O(Z)	-
50	DBSC3 channel 0	P
G22	VDDQ_M0DPLL0	-
	P	-
51	DBSC3 channel 0	P
G23	VSSQ_M0DPLL0	-
	P	-
52	DBSC3 channel 0	P
G24	M0VREFDQ0	-
	P	-
53	DBSC3 channel 0	Z
B23	M0DQ8	1.35V/-
	IO(Z)	-
54	DBSC3 channel 0	Z
A24	M0DQ9	1.35V/-
	IO(Z)	-
55	DBSC3 channel 0	Z
C24	M0DQ10	1.35V/-
	IO(Z)	-
56	DBSC3 channel 0	Z
D24	M0DQ11	1.35V/-
	IO(Z)	-
57	DBSC3 channel 0	Z
B26	M0DQ12	1.35V/-
	IO(Z)	-
58	DBSC3 channel 0	Z
D26	M0DQ13	1.35V/-
	IO(Z)	-
59	DBSC3 channel 0	Z
B24	M0DQ14	1.35V/-
	IO(Z)	-
60	DBSC3 channel 0	Z
A25	M0DQ15	1.35V/-
	IO(Z)	-

1/2 (DBSC3 channel 0)

DBSC3 channel 0 (No.61 to 93): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
61	DBSC3 channel 0	Z
E23	M0DQS1	1.35V/-
	IO(Z)	-
62	DBSC3 channel 0	Z
E24	M0DQS1#	1.35V/-
	IO(Z)	-
63	DBSC3 channel 0	Z
C25	M0DM1	1.35V/-
	O(Z)	-
64	DBSC3 channel 0	P
F22	VDDQ_M0DPLL1	-
	P	-
65	DBSC3 channel 0	P
F23	VSSQ_M0DPLL1	-
	P	-
66	DBSC3 channel 0	Z
E31	M0DQ16	1.35V/-
	IO(Z)	-
67	DBSC3 channel 0	Z
C30	M0DQ17	1.35V/-
	IO(Z)	-
68	DBSC3 channel 0	Z
E29	M0DQ18	1.35V/-
	IO(Z)	-
69	DBSC3 channel 0	Z
B31	M0DQ19	1.35V/-
	IO(Z)	-
70	DBSC3 channel 0	Z
E30	M0DQ20	1.35V/-
	IO(Z)	-
71	DBSC3 channel 0	Z
C31	M0DQ21	1.35V/-
	IO(Z)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
72	DBSC3 channel 0	Z
E28	M0DQ22	1.35V/-
	IO(Z)	-
73	DBSC3 channel 0	Z
D29	M0DQ23	1.35V/-
	IO(Z)	-
74	DBSC3 channel 0	Z
F27	M0DQS2	1.35V/-
	IO(Z)	-
75	DBSC3 channel 0	Z
G27	M0DQS2#	1.35V/-
	IO(Z)	-
76	DBSC3 channel 0	Z
D31	M0DM2	1.35V/-
	O(Z)	-
77	DBSC3 channel 0	P
K25	VDDQ_M0DPLL2	-
	P	-
78	DBSC3 channel 0	P
J25	VSSQ_M0DPLL2	-
	P	-
79	DBSC3 channel 0	P
H25	M0VREFDQ1	-
	P	-
80	DBSC3 channel 0	Z
F28	M0DQ24	1.35V/-
	IO(Z)	-
81	DBSC3 channel 0	Z
G31	M0DQ25	1.35V/-
	IO(Z)	-
82	DBSC3 channel 0	Z
F30	M0DQ26	1.35V/-
	IO(Z)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
83	DBSC3 channel 0	Z
H30	M0DQ27	1.35V/-
	IO(Z)	-
84	DBSC3 channel 0	Z
H28	M0DQ28	1.35V/-
	IO(Z)	-
85	DBSC3 channel 0	Z
J30	M0DQ29	1.35V/-
	IO(Z)	-
86	DBSC3 channel 0	Z
H29	M0DQ30	1.35V/-
	IO(Z)	-
87	DBSC3 channel 0	Z
H31	M0DQ31	1.35V/-
	IO(Z)	-
88	DBSC3 channel 0	Z
J27	M0DQS3	1.35V/-
	IO(Z)	-
89	DBSC3 channel 0	Z
H27	M0DQS3#	1.35V/-
	IO(Z)	-
90	DBSC3 channel 0	Z
G29	M0DM3	1.35V/-
	O(Z)	-
91	DBSC3 channel 0	P
K26	VDDQ_M0DPLL3	-
	P	-
92	DBSC3 channel 0	P
J26	VSSQ_M0DPLL3	-
	P	-
93	DBSC3 channel 0	P
H19	VDDQ_M0BKUP	-
	P	-

2/2 (DBSC3 channel 0)

DBSC3 channel 1 (No.94 to 113): 3-Function Multiplexed

These pins function and pin states during power-on reset depend on MD28, MD 27 and MD22 pins setting, and cannot be changed after power-on reset by software.

	Function 1	Function 2	Function 3	
	MD28 = 1, MD27 = 1, MD22 = 1	MD28 = 0, MD27 = 1, MD22 = 1	MD28 = 1, MD27 = 1, MD22 = 0	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
94	DBSC3 channel 1	GPIO	GPIO	X
F5	M1CKE0	GP_DDR1	GP_DDR1	1.35V/1.8V(GPIO)/-
	O(L)	O	O	-
95	DBSC3 channel 1	GPIO	GPIO	X
G3	M1CKE1	GP_DDR2	GP_DDR2	1.35V/1.8V(GPIO)/-
	O(L)	O	O	-
96	DBSC3 channel 1	Reserved*	Reserved*	P
H7	M1VREFCA	-	-	-
	P	-	-	-
97	DBSC3 channel 1	Reserved*	Reserved*	I
J7	M1BKPRST#	-	-	1.35V/-
	I	-	-	-
98	DBSC3 channel 1	GPIO	GPIO	H/X(GPIO)
G5	M1RESET#	GP_DDR3	GP_DDR3	1.35V/1.8V(GPIO)/-
	O(H to L)	O	O	-
99	DBSC3 channel 1	Reserved*	Reserved*	X
J5	M1CK0	-	-	1.35V/-
	O	-	-	-
100	DBSC3 channel 1	Reserved*	Reserved*	X
H5	M1CK0#	-	-	1.35V/-
	O	-	-	-
101	DBSC3 channel 1	Reserved*	Reserved*	X
L5	M1CK1	-	-	1.35V/-
	O	-	-	-
102	DBSC3 channel 1	Reserved*	Reserved*	X
K5	M1CK1#	-	-	1.35V/-
	O	-	-	-
103	DBSC3 channel 1	GPIO	GPIO	H/I(GPIO)
F2	M1CS0#	GP_DDR5	GP_DDR5	1.35V/1.8V(GPIO)/-
	O(H)	I	I	-
104	DBSC3 channel 1	GPIO	GPIO	H/I(GPIO)
G1	M1CS1#	GP_DDR8	GP_DDR8	1.35V/1.8V(GPIO)/-
	O(H)	I	I	-
105	DBSC3 channel 1	GPIO	GPIO	L/I(GPIO)
F4	M1ODT0	GP_DDR6	GP_DDR6	1.35V/1.8V(GPIO)/-
	O(L)	I	I	-
106	DBSC3 channel 1	GPIO	GPIO	L/I(GPIO)
H4	M1ODT1	GP_DDR10	GP_DDR10	1.35V/1.8V(GPIO)/-
	O(L)	I	I	-
107	DBSC3 channel 1	Reserved*	Reserved*	IO
L8	M1ZQ	-	-	-
	IO	-	-	-
108	DBSC3 channel 1	GPIO	GPIO	H/Z(GPIO)
E3	M1WE#	GP_DDR9	GP_DDR9	1.35V/1.8V(GPIO)/-
	O(H)	O(Z)	O(Z)	-
109	DBSC3 channel 1	GPIO	GPIO	H/Z(GPIO)
D3	M1RAS#	GP_DDR12	GP_DDR12	1.35V/1.8V(GPIO)/-
	O(H)	O(Z)	O(Z)	-
110	DBSC3 channel 1	GPIO	GPIO	H/I(GPIO)
E4	M1CAS#	GP_DDR4	GP_DDR4	1.35V/-
	O(H)	I	I	-
111	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
B1	M1A0	GP_DDR7	GP_DDR7	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
112	DBSC3 channel 1	GPIO	GPIO	L/I(GPIO)
H2	M1A1	GP_DDR13	GP_DDR13	1.35V/1.8V(GPIO)/-
	O(L)	I	I	-
113	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
E2	M1A2	GP_DDR15	GP_DDR15	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-

1/5 (DBSC3 channel 1)

Note: * Reserved pins in function 2 and 3 should be handled as described in section 4.3, Handling of Unused Pins.

DBSC3 channel 1 (No.114 to 133): 3-Function Multiplexed

These pins function and pin states during power-on reset depend on MD28, MD 27 and MD22 pins setting, and cannot be changed after power-on reset by software.

	Function 1	Function 2	Function 3	
	MD28 = 1, MD27 = 1, MD22 = 1	MD28 = 0, MD27 = 1, MD22 = 1	MD28 = 1, MD27 = 1, MD22 = 0	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
114	DBSC3 channel 1	GPIO	GPIO	L/I(GPIO)
M3	M1A3	GP_DDR23	GP_DDR23	1.35V/1.8V(GPIO)/-
	O(L)	I	I	-
115	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
E1	M1A4	GP_DDR17	GP_DDR17	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
116	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
D1	M1A5	GP_DDR11	GP_DDR11	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
117	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
K2	M1A6	GP_DDR24	GP_DDR24	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
118	DBSC3 channel 1	GPIO	GPIO	L/I(GPIO)
H1	M1A7	GP_DDR14	GP_DDR14	1.35V/1.8V(GPIO)/-
	O(L)	I	I	-
119	DBSC3 channel 1	GPIO	GPIO	L/I(GPIO)
M1	M1A8	GP_DDR25	GP_DDR25	1.35V/1.8V(GPIO)/-
	O(L)	I	I	-
120	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
J2	M1A9	GP_DDR26	GP_DDR26	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
121	DBSC3 channel 1	GPIO	GPIO	L/I(GPIO)
L3	M1A10	GP_DDR22	GP_DDR22	1.35V/1.8V(GPIO)/-
	O(L)	I	I	-
122	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
K1	M1A11	GP_DDR21	GP_DDR21	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
123	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
C2	M1A12	GP_DDR16	GP_DDR16	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
124	DBSC3 channel 1	GPIO	GPIO	L/I(GPIO)
L1	M1A13	GP_DDR27	GP_DDR27	1.35V/1.8V(GPIO)/-
	O(L)	I	I	-
125	DBSC3 channel 1	GPIO	GPIO	L/I(GPIO)
M2	M1A14	GP_DDR28	GP_DDR28	1.35V/1.8V(GPIO)/-
	O(L)	I	I	-
126	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
K3	M1A15	GP_DDR29	GP_DDR29	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
127	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
J3	M1BA0	GP_DDR20	GP_DDR20	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
128	DBSC3 channel 1	GPIO	GPIO	L/Z(GPIO)
C1	M1BA1	GP_DDR19	GP_DDR19	1.35V/1.8V(GPIO)/-
	O(L)	O(Z)	O(Z)	-
129	DBSC3 channel 1	GPIO	GPIO	L/I(GPIO)
H3	M1BA2	GP_DDR18	GP_DDR18	1.35V/1.8V(GPIO)/-
	O(L)	I	I	-
130	DBSC3 channel 1	DBSC3 channel 1	DBSC3 channel 1	P
L7	VDDQ_M1APLL	VDDQ_M1APLL	VDDQ_M1APLL	-
	P	P	P	-
131	DBSC3 channel 1	DBSC3 channel 1	DBSC3 channel 1	P
K7	VSSQ_M1APLL	VSSQ_M1APLL	VSSQ_M1APLL	-
	P	P	P	-
132	DBSC3 channel 1	DBSC3 channel 1	DBSC3 channel 1	P
L6	VDDQ_M1MPLL	VDDQ_M1MPLL	VDDQ_M1MPLL	-
	P	P	P	-
133	DBSC3 channel 1	DBSC3 channel 1	DBSC3 channel 1	P
K6	VSSQ_M1MPLL	VSSQ_M1MPLL	VSSQ_M1MPLL	-
	P	P	P	-

2/5 (DBSC3 channel 1)

DBSC3 channel 1 (No.134 to 153): 3-Function Multiplexed

These pins function and pin states during power-on reset depend on MD28, MD 27 and MD22 pins setting, and cannot be changed after power-on reset by software.

	Function 1	Function 2	Function 3	
	MD28 = 1, MD27 = 1, MD22 = 1	MD28 = 0, MD27 = 1, MD22 = 1	MD28 = 1, MD27 = 1, MD22 = 0	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
134	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B12	M1DQ0	M0DQ32	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
135	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B11	M1DQ1	M0DQ33	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
136	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D12	M1DQ2	M0DQ34	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
137	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A10	M1DQ3	M0DQ35	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
138	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C11	M1DQ4	M0DQ36	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
139	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D10	M1DQ5	M0DQ37	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
140	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C10	M1DQ6	M0DQ38	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
141	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D11	M1DQ7	M0DQ39	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
142	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E12	M1DQS0	M0DQS4	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
143	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E11	M1DQS0#	M0DQS4#	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
144	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A11	M1DM0	M0DM4	-	1.35V/-
	O(Z)	O(Z)	Z	-
145	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
G13	VDDQ_M1DPLL0	VDDQ_M0DPLL4	VDDQ_M0DPLL4	-
	P	P	P	-
146	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
G12	VSSQ_M1DPLL0	VSSQ_M0DPLL4	VSSQ_M0DPLL4	-
	P	P	P	-
147	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
G14	M1VREFDQ0	M0VREFDQ2	M0VREFDQ2	-
	P	P	P	-
148	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A13	M1DQ8	M0DQ40	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
149	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A14	M1DQ9	M0DQ41	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
150	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D14	M1DQ10	M0DQ42	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
151	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B14	M1DQ11	M0DQ43	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
152	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C14	M1DQ12	M0DQ44	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
153	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B15	M1DQ13	M0DQ45	-	1.35V/-
	IO(Z)	IO(Z)	Z	-

3/5 (DBSC3 channel 1)

Note: * Reserved pins in function 3 should be opened.

DBSC3 channel 1 (No.154 to 173): 3-Function Multiplexed

These pins function and pin states during power-on reset depend on MD28, MD 27 and MD22 pins setting, and cannot be changed after power-on reset by software.

	Function 1	Function 2	Function 3	
	MD28=1, MD27=1, MD22=1	MD28=0, MD27=1, MD22=1	MD28=1,MD27=1,MD22=0	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
154	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D15	M1DQ14	M0DQ46	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
155	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A15	M1DQ15	M0DQ47	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
156	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E14	M1DQS1	M0DQS5	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
157	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E13	M1DQS1#	M0DQS5#	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
158	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C13	M1DM1	M0DM5	-	1.35V/-
	O(Z)	O(Z)	Z	-
159	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
F13	VDDQ_M1DPLL1	VDDQ_M0DPLL5	VDDQ_M0DPLL5	-
	P	P	P	-
160	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
F12	VSSQ_M1DPLL1	VSSQ_M0DPLL5	VSSQ_M0DPLL5	-
	P	P	P	-
161	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B6	M1DQ16	M0DQ48	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
162	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A7	M1DQ17	M0DQ49	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
163	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C8	M1DQ18	M0DQ50	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
164	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B8	M1DQ19	M0DQ51	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
165	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D8	M1DQ20	M0DQ52	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
166	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A8	M1DQ21	M0DQ53	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
167	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D6	M1DQ22	M0DQ54	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
168	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B9	M1DQ23	M0DQ55	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
169	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E8	M1DQS2	M0DQS6	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
170	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E9	M1DQS2#	M0DQS6#	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
171	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C7	M1DM2	M0DM6	-	1.35V/-
	O(Z)	O(Z)	Z	-
172	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
F10	VDDQ_M1DPLL2	VDDQ_M0DPLL6	VDDQ_M0DPLL6	-
	P	P	P	-
173	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
F9	VSSQ_M1DPLL2	VSSQ_M0DPLL6	VSSQ_M0DPLL6	-
	P	P	P	-

4/5 (DBSC3 channel 1)

Note: * Reserved pins in function 3 should be opened.

DBSC3 channel 1 (No.174 to 188): 3-Function Multiplexed

These pins function and the pin state during power-on reset depend on MD28, MD 27 and MD22 pins setting, and cannot be changed after power-on reset by software.

	Function 1	Function 2	Function 3	
	MD28=1, MD27=1, MD22=1	MD28=0, MD27=1, MD22=1	MD28=1,MD27=1,MD22=0	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
174	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
G8	M1VREFDQ1	M0VREFDQ3	M0VREFDQ3	-
	P	P	P	-
175	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B3	M1DQ24	M0DQ56	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
176	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
D5	M1DQ25	M0DQ57	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
177	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C4	M1DQ26	M0DQ58	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
178	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
C5	M1DQ27	M0DQ59	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
179	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A5	M1DQ28	M0DQ60	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
180	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A3	M1DQ29	M0DQ61	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
181	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
B5	M1DQ30	M0DQ62	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
182	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A2	M1DQ31	M0DQ63	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
183	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E7	M1DQS3	M0DQS7	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
184	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
E6	M1DQS3#	M0DQS7#	-	1.35V/-
	IO(Z)	IO(Z)	Z	-
185	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	Reserved*	Z
A4	M1DM3	M0DM7	-	1.35V/-
	O(Z)	O(Z)	Z	-
186	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
G10	VDDQ_M1DPLL3	VDDQ_M0DPLL7	VDDQ_M0DPLL7	-
	P	P	P	-
187	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
G9	VSSQ_M1DPLL3	VSSQ_M0DPLL7	VSSQ_M0DPLL7	-
	P	P	P	-
188	DBSC3 channel 1	DBSC3 channel 0 (64-bit)	DBSC3 channel 0	P
G6	VDDQ_M1BKUP	VDDQ_M1BKUP	VDDQ_M1BKUP	-
	P	P	P	-

5/5 (DBSC3 channel 1)

Note: * Reserved pins in function 3 should be opened.

CPG, RESET, SYSTEM, AVS, POWER ISO and Debug (No.189 to 212): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
189	CPG	I
AL18	EXTAL	1.8V/-
	I	-
190	CPG	O
AL17	XTAL	1.8V/-
	O	-
191	CPG	P
F16	VDD_CPGPLL1	-
	P	-
192	CPG	P
F15	VSS_CPGPLL1	-
	P	-
193	CPG	P
H15	VDD_CPGPLL2	-
	P	-
194	CPG	P
G15	VSS_CPGPLL2	-
	P	-
195	CPG	P
L25	VDD_CPGPLL0	-
	P	-
196	CPG	P
M25	VSS_CPGPLL0	-
	P	-
197	CPG	P
L26	VDD_CPGPLL3	-
	P	-
198	CPG	P
M26	VSS_CPGPLL3	-
	P	-
199	RESET	I(S)
AE19	PRESET#	1.8V/-
	I(S)	-
200	RESET	L
U5	PRESETOUT#	3.3V/4mA
	O(L to H)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up(pull-down)*2
201	SYSTEM	I(S)
AG19	MPMD0	1.8V/-
	I(S)	-
202	SYSTEM	I(S)
AG18	MPMD1	1.8V/-
	I(S)	-
203	SYSTEM	I(S)
AF17	BSMODE	1.8V/-
	I(S)	-
204	AVS	L
U6	AVS1	3.3V/4mA
	O(H/L)*1	Off
205	AVS	L
U7	AVS2	3.3V/4mA
	O(H/L)*1	Off
206	POWER ISO	P
AD19	VCCQ_ISO	-
	P	-
207	Debug	I
AF19	TRST#	1.8V/-
	I	On
208	Debug	I
AE18	TCK	1.8V/-
	I	On
209	Debug	I
AF18	TMS	1.8V/-
	I(I)	On
210	Debug	I
AH17	TDI	1.8V/-
	I	On
211	Debug	Z
AJ17	TDO	1.8V/8mA
	O(Z)	-
212	Debug	I
AE17	ACK	1.8V/4mA
	IO(I)	On(pulled-down)*2

Notes: 1. (No.204 and 205): Output value of the AVS[2:1] pins depends on each product.
2. (No.212): ACK pin is available for pull-down function.

SATA, PCIEC and USB3.0 (No.213 to 254): 2-Function Multiplexed

These pins function depends on the MD[24:23] pins setting, and cannot be changed after power-on reset by software.

	Function 1	Function 2	
	MD24=0	MD24=1	
No.	Module		During POR
Pin No.	Pin Name		V/|IOH|
	I/O		Pull-up
213	SATA1	PCIEC	I
AL23	RIDP1_SATA	RIDP1_PCIe	1.0V/-
	I	I	-
214	SATA1	PCIEC	I
AL24	RIDN1_SATA	RIDN1_PCIe	1.0V/-
	I	I	-
215	SATA1	PCIEC	O
AL25	TODP1_SATA	TODP1_PCIe	1.0V/-
	O	O	-
216	SATA1	PCIEC	O
AL26	TODN1_SATA	TODN1_PCIe	1.0V/-
	O	O	-
217	SATA1	PCIEC	I
AJ26	CICREFP1_SATA	CICREFP1_PCIe	1.0V/-
	I	I	-
218	SATA1	PCIEC	I
AJ25	CICREFN1_SATA	CICREFN1_PCIe	1.0V/-
	I	I	-
219	SATA1	PCIEC	P
AE23	VSS_SATA1	VSS_PCIe	-
	P	P	-
220	SATA1	PCIEC	P
AF24	VDDA_SATA1	VDDA_PCIe	-
	P	P	-
221	SATA1	PCIEC	P
AG24	VDDA_SATA1	VDDA_PCIe	-
	P	P	-
222	SATA1	PCIEC	P
AF23	VDDD_SATA1	VDDD_PCIe	-
	P	P	-
223	SATA1	PCIEC	P
AG23	VDDD_SATA1	VDDD_PCIe	-
	P	P	-
224	SATA1	PCIEC	P
AH24	VDDD_SATA1	VDDD_PCIe	-
	P	P	-
225	SATA1	PCIEC	P
AD23	VSS_SATA1	VSS_PCIe	-
	P	P	-
226	SATA1	PCIEC	P
AE24	VSS_SATA1	VSS_PCIe	-
	P	P	-
227	SATA1	PCIEC	P
AJ24	VSS_SATA1	VSS_PCIe	-
	P	P	-
228	SATA1	PCIEC	P
AK24	VSS_SATA1	VSS_PCIe	-
	P	P	-
229	SATA1	PCIEC	P
AK25	VSS_SATA1	VSS_PCIe	-
	P	P	-
230	SATA1	PCIEC	P
AK26	VSS_SATA1	VSS_PCIe	-
	P	P	-
231	SATA1	PCIEC	P
AK23	VSS_SATA1	VSS_PCIe	-
	P	P	-

	Function 1	Function 2	
	MD23=0	MD23=1	
No.	Module		During POR
Pin No.	Pin Name		V/|IOH|
	I/O		Pull-up
232	SATA0	USB 3.0	I
AL27	RIDP0_SATA	RIDP0_USB3	1.0V/-
	I	I	-
233	SATA0	USB 3.0	I
AL28	RIDN0_SATA	RIDN0_USB3	1.0V/-
	I	I	-
234	SATA0	USB 3.0	O
AL29	TODP0_SATA	TODP0_USB3	1.0V/-
	O	O	-
235	SATA0	USB 3.0	O
AL30	TODN0_SATA	TODN0_USB3	1.0V/-
	O	O	-
236	SATA0	USB 3.0	I
AJ28	CICREFP0_SATA	CICREFP0_USB3	1.0V/-
	I	I	-
237	SATA0	USB 3.0	I
AJ27	CICREFN0_SATA	CICREFN0_USB3	1.0V/-
	I	I	-
238	SATA0	USB 3.0	P
AF25	VSS_SATA0	VSS_USB3	-
	P	P	-
239	SATA0	USB 3.0	P
AG26	VDDA_SATA0	VDDA_USB3	-
	P	P	-
240	SATA0	USB 3.0	P
AH27	VDDA_SATA0	VDDA_USB3	-
	P	P	-
241	SATA0	USB 3.0	P
AH25	VDDD_SATA0	VDDD_USB3	-
	P	P	-
242	SATA0	USB 3.0	P
AH26	VDDD_SATA0	VDDD_USB3	-
	P	P	-
243	SATA0	USB 3.0	P
AG25	VDDD_SATA0	VDDD_USB3	-
	P	P	-
244	SATA0	USB 3.0	P
AD24	VSS_SATA0	VSS_USB3	-
	P	P	-
245	SATA0	USB 3.0	P
AE25	VSS_SATA0	VSS_USB3	-
	P	P	-
246	SATA0	USB 3.0	P
AF26	VSS_SATA0	VSS_USB3	-
	P	P	-
247	SATA0	USB 3.0	P
AG27	VSS_SATA0	VSS_USB3	-
	P	P	-
248	SATA0	USB 3.0	P
AK27	VSS_SATA0	VSS_USB3	-
	P	P	-
249	SATA0	USB 3.0	P
AH28	VSS_SATA0	VSS_USB3	-
	P	P	-
250	SATA0	USB 3.0	P
AK28	VSS_SATA0	VSS_USB3	-
	P	P	-
251	SATA0	USB 3.0	P
AJ29	VSS_SATA0	VSS_USB3	-
	P	P	-
252	SATA0	USB 3.0	P
AK29	VSS_SATA0	VSS_USB3	-
	P	P	-
253	SATA0	USB 3.0	P
AK30	VSS_SATA0	VSS_USB3	-
	P	P	-
254	SATA0	USB 3.0	P
AL31	VSS_SATA0	VSS_USB3	-
	P	P	-

USB 2.0 and DU/LVDS (No.255 to 292): Up to 2-Function Multiplexed

These pins default function after power-on reset is USB2.0 and DU0 except for No.287 (DU0_DOTCLKIN).

	Function 1	GPIO	
No.	**Module**		**During POR**
Pin No.	**Pin Name**		**V/|IOH|**
	I/O		**Pull-up**
255	USB	-	I
AL20	USB_EXTAL	-	1.8V/-
	I	-	-
256	USB	-	O
AL19	USB_XTAL	-	1.8V/-
	O	-	-
257	USB 2.0 channel 0	-	I
AG31	USB0_DP	-	3.3V/-
	IO	-	-
258	USB 2.0 channel 0	-	I
AH31	USB0_DM	-	3.3V/-
	IO	-	-
259	USB 2.0 channel 0	-	I
AG29	USB0_RREF	-	3.3V/-
	I	-	-
260	USB 2.0 channel 0	-	P
AE27	VD331	-	-
	P	-	-
261	USB 2.0 channel 0	-	P
AD26	VD181	-	-
	P	-	-
262	USB 2.0 channel 0	-	P
AB24	AVDD	-	-
	P	-	-
263	USB 2.0 channel 0	-	P
AC24	AVSS	-	-
	P	-	-
264	USB 2.0 channel 0		L
AF31	USB0_PWEN	GP7_23	3.3V/4mA
	O(L)	IO	Off
265	USB 2.0 channel 0		I
AF30	USB0_OVC/VBUS	GP7_24	3.3V/4mA
	I	IO	On
266	USB 2.0 channel 1	-	I
AJ31	USB1_DP	-	3.3V/-
	IO	-	-
267	USB 2.0 channel 1	-	I
AK31	USB1_DM	-	3.3V/-
	IO	-	-
268	USB 2.0 channel 1	-	I
AH29	USB1_RREF	-	3.3V/-
	I	-	-
269	USB 2.0 channel 1	-	P
AF28	VD331	-	-
	P	-	-
270	USB 2.0 channel 1	-	P
AC25	AVDD	-	-
	P	-	-
271	USB 2.0 channel 1	-	P
AD25	AVSS	-	-
	P	-	-
272	USB 2.0 channel 1	-	P
AE26	AVSS	-	-
	P	-	-
273	USB 2.0 channel 1	-	P
AF27	AVSS	-	-
	P	-	-

	Function 1	GPIO	
No.	**Module**		**During POR**
Pin No.	**Pin Name**		**V/|IOH|**
	I/O		**Pull-up**
274	USB 2.0 channel 1	-	P
AG28	AVSS	-	-
	P	-	-
275	USB 2.0 channel 1		L
AE28	USB1_PWEN	GP7_25	3.3V/4mA
	O(L)	IO	Off
276	USB 2.0 channel 1		I
AD27	USB1_OVC	GP6_30	3.3V/4mA
	I	IO	On
277	DU0	-	Z
AE20	DU0_LVDS_CLK_P	-	1.8V/-
	O(Z)	-	-
278	DU0	-	Z
AF20	DU0_LVDS_CLK_N	-	1.8V/-
	O(Z)	-	-
279	DU0	-	Z
AJ23	DU0_LVDS_CH0_P	-	1.8V/-
	O(Z)	-	-
280	DU0	-	Z
AJ22	DU0_LVDS_CH0_N	-	1.8V/-
	O(Z)	-	-
281	DU0	-	Z
AL21	DU0_LVDS_CH1_P	-	1.8V/-
	O(Z)	-	-
282	DU0	-	Z
AL22	DU0_LVDS_CH1_N	-	1.8V/-
	O(Z)	-	-
283	DU0	-	Z
AJ20	DU0_LVDS_CH2_P	-	1.8V/-
	O(Z)	-	-
284	DU0	-	Z
AJ21	DU0_LVDS_CH2_N	-	1.8V/-
	O(Z)	-	-
285	DU0	-	Z
AG22	DU0_LVDS_CH3_P	-	1.8V/-
	O(Z)	-	-
286	DU0	-	Z
AG21	DU0_LVDS_CH3_N	-	1.8V/-
	O(Z)	-	-
287*	DU0		I(GPIO)
AG17	DU0_DOTCLKIN	GP6_31	1.8V/4mA
	I	IO(I)	On
288	DU0	-	P
AD22	VDDQ_LVDS	-	-
	P	-	-
289	DU0	-	P
AE22	VDDQ_LVDS	-	-
	P	-	-
290	DU0	-	P
AF22	VDDQ_LVDS	-	-
	P	-	-
291	DU0	-	P
AD20	DU0_LVDS_PLL1_VCC	-	-
	P	-	-
292	DU0	-	P
AD21	DU0_LVDS_PLL1_VSS	-	-
	P	-	-

Note: * (No.287): DU0_DOTCLKIN pin is set for GPIO after power-on reset. For details, refer to GPSR6 register in section 5, Pin Function Controller (PFC).

LBSC (D[15:0]) and GPIO (No.293 to 308): 3-Function Multiplexed

These pins default function (function 1 or GPIO) after power-on reset depends on MD[3:1] pins setting.

	Function 1	Function 2	GPIO	
	MD[3:1] = 000		MD[3:1] ≠ 000	
No.	Module			During POR
Pin No.	Pin Name			V/|IOH|
	I/O			Pull-up
293	LBSC	Reserved		I(GPIO)
AA7	D0	-	GP0_0	3.3V/8mA
	IO(I)	-	IO(I)	On
294	LBSC	Reserved		I(GPIO)
AA6	D1	-	GP0_1	3.3V/8mA
	IO(I)	-	IO(I)	On
295	LBSC	Reserved		I(GPIO)
AA5	D2	-	GP0_2	3.3V/8mA
	IO(I)	-	IO(I)	On
296	LBSC	Reserved		I(GPIO)
AA4	D3	-	GP0_3	3.3V/8mA
	IO(I)	-	IO(I)	On
297	LBSC	Reserved		I(GPIO)
AA3	D4	-	GP0_4	3.3V/8mA
	IO(I)	-	IO(I)	On
298	LBSC	Reserved		I(GPIO)
AA2	D5	-	GP0_5	3.3V/8mA
	IO(I)	-	IO(I)	On
299	LBSC	Reserved		I(GPIO)
AA1	D6	-	GP0_6	3.3V/8mA
	IO(I)	-	IO(I)	On
300	LBSC	Reserved		I(GPIO)
Y7	D7	-	GP0_7	3.3V/8mA
	IO(I)	-	IO(I)	On
301	LBSC	Reserved		I(GPIO)
Y6	D8	-	GP0_8	3.3V/8mA
	IO(I)	-	IO(I)	On
302	LBSC	Reserved		I(GPIO)
Y5	D9	-	GP0_9	3.3V/8mA
	IO(I)	-	IO(I)	On
303	LBSC	Reserved		I(GPIO)
Y4	D10	-	GP0_10	3.3V/8mA
	IO(I)	-	IO(I)	On
304	LBSC	Reserved		I(GPIO)
Y3	D11	-	GP0_11	3.3V/8mA
	IO(I)	-	IO(I)	On
305	LBSC	Reserved		I(GPIO)
Y2	D12	-	GP0_12	3.3V/8mA
	IO(I)	-	IO(I)	On
306	LBSC	Reserved		I(GPIO)
Y1	D13	-	GP0_13	3.3V/8mA
	IO(I)	-	IO(I)	On
307	LBSC	Reserved		I(GPIO)
W2	D14	-	GP0_14	3.3V/8mA
	IO(I)	-	IO(I)	On
308	LBSC	Reserved		I(GPIO)
W1	D15	-	GP0_15	3.3V/8mA
	IO(I)	-	IO(I)	On

LBSC, MSIOF, I2C, PWM, MSIOF, and GPIO (No.309 to 324): Up to 7-Function Multiplexed and Mode Pins assigned (No.310 to 313, 316, 319, 322 to 324)

These pins default function (function 1 or GPIO) after power-on reset depends on MD[3:1] pins setting.

	Function							
	1	2	3	4	5	6	GPIO	
	MD[3:1] = 000						MD[3:1]≠000	
No.	Module							During POR
Pin No.	Pin Name							V/|IOH|
Mode Pin	I/O							Pull-up
309	LBSC	LBSC	MSIOF0	I2C0	PWM2	Reserved		I(GPIO)
T7	A0	ATAWR0#_C	MSIOF0_SCK_B	I2C0_SCL_C	PWM2_B	-	GP0_16	3.3V/8mA
-	O(L)	O	IO	IO	O	-	IO(I)	On
310	LBSC	MSIOF0	Reserved	-	-	-		I(Mode Pin)
W7	A1	MSIOF0_SYNC_B	-	-	-	-	GP0_17	3.3V/8mA
MD28	O(L)	IO	-	-	-	-	IO(I)	Off
311	LBSC	MSIOF0	Reserved	-	-	-		I(Mode Pin)
W6	A2	MSIOF0_SS1_B	-	-	-	-	GP0_18	3.3V/8mA
MD23	O(L)	O	-	-	-	-	IO(I)	Off
312	LBSC	MSIOF0	Reserved	-	-	-		I(Mode Pin)
W5	A3	MSIOF0_SS2_B	-	-	-	-	GP0_19	3.3V/8mA
MD13	O(L)	O	-	-	-	-	IO(I)	Off
313	LBSC	MSIOF0	Reserved	-	-	-		I(Mode Pin)
W4	A4	MSIOF0_TXD_B	-	-	-	-	GP0_20	3.3V/8mA
MD24	O(L)	O	-	-	-	-	IO(I)	Off
314	LBSC	MSIOF0	Reserved	-	-	-		I(GPIO)
W3	A5	MSIOF0_RXD_B	-	-	-	-	GP0_21	3.3V/8mA
-	O(L)	I	-	-	-	-	IO(I)	On
315	LBSC	MSIOF1	Reserved	-	-	-		I(GPIO)
T6	A6	MSIOF1_SCK	-	-	-	-	GP0_22	3.3V/8mA
-	O(L)	IO	-	-	-	-	IO(I)	On
316	LBSC	MSIOF1	Reserved	-	-	-		I(Mode Pin)
V7	A7	MSIOF1_SYNC	-	-	-	-	GP0_23	3.3V/8mA
MD27	O(L)	IO	-	-	-	-	IO(I)	Off
317	LBSC	MSIOF1	I2C0	Reserved	-	-		I(GPIO)
T5	A8	MSIOF1_SS1	I2C0_SCL	-	-	-	GP0_24	3.3V/8mA
-	O(L)	O	IO	-	-	-	IO(I)	On
318	LBSC	MSIOF1	I2C0	Reserved	-	-		I(GPIO)
T4	A9	MSIOF1_SS2	I2C0_SDA	-	-	-	GP0_25	3.3V/8mA
-	O(L)	O	IO	-	-	-	IO(I)	On
319	LBSC	MSIOF1	Reserved	MSIOF1	-	-		I(Mode Pin)
V6	A10	MSIOF1_TXD	-	MSIOF1_TXD_D	-	-	GP0_26	3.3V/8mA
MD22	O(L)	O	-	O	-	-	IO(I)	Off
320	LBSC	MSIOF1	I2C3	MSIOF1	Reserved	-		I(GPIO)
T3	A11	MSIOF1_RXD	I2C3_SCL_D	MSIOF1_RXD_D	-	-	GP0_27	3.3V/8mA
-	O(L)	I	IO	I	-	-	IO(I)	On
321	LBSC	Reserved	I2C3	MSIOF1	Reserved	-		I(GPIO)
T2	A12	-	I2C3_SDA_D	MSIOF1_SCK_D	-	-	GP0_28	3.3V/8mA
-	O(L)	-	IO	IO	-	-	IO(I)	On
322	LBSC	LBSC	Reserved	MSIOF1	Reserved	-		I(Mode Pin)
R7	A13	ATAG0#_C	-	MSIOF1_SS1_D	-	-	GP0_29	3.3V/8mA
MD21	O(L)	O	-	O	-	-	IO(I)	Off
323	LBSC	LBSC	Reserved	Reserved	MSIOF1	Reserved		I(Mode Pin)
R6	A14	ATADIR0#_C	-	-	MSIOF1_SYNC_D	-	GP0_30	3.3V/8mA
MD19	O(L)	O	-	-	IO	-	IO(I)	Off
324	LBSC	Reserved	Reserved	Reserved	Reserved	-		I(Mode Pin)
R5	A15	-	-	-	-	-	GP0_31	3.3V/8mA
MD20	O(L)	-	-	-	-	-	IO(I)	Off

LBSC, MSIOF, I2C, SCIFA, SCIFB, QSPI, SCIF, HSCIF, PWM, TPU, and GPIO (No.325 to 343): Up to 9-Function Multiplexed and Mode Pins assigned (No.328, 341, 343)

These pins default function (function 1 or GPIO) after power-on reset depends on MD[3:1] pins setting. When MD[3:1] = 010, 100, 101 or 110, QSPI boot is executed after power-on reset and after that the GPIO is available.

	Function									
	1	2	3	4	5	6	7	8	GPIO	
	MD[3:1] = 000								MD[3:1] ≠000	
No.	Module									During POR
Pin No.	Pin Name									V/|IOH|
Mode Pin	I/O									Pull-up
325	LBSC	LBSC	Reserved	Reserved	SCIFA1	Reserved	Reserved	-		I(GPIO)
R4	A16	DREQ2_B	-	-	SCIFA1_SCK_B	-	-	-	GP1_0	3.3V/8mA
	O(L)	I	-	-	O	-	-	-	IO(I)	On
326	LBSC	LBSC	Reserved	I2C0	Reserved	Reserved	-	-		I(GPIO)
R3	A17	DACK2_B	-	I2C0_SDA_C	-	-	-	-	GP1_1	3.3V/8mA
	O(L)	O	-	IO	-	-	-	-	IO(I)	On
327	LBSC	LBSC	SCIFA1	Reserved	SCIFB1	Reserved	Reserved	-		I(GPIO)
R2	A18	DREQ1	SCIFA1_RXD_C	-	SCIFB1_RXD_C	-	-	-	GP1_2	3.3V/8mA
	O(L)	I	I	-	I	-	-	-	IO(I)	On
328	LBSC	LBSC	SCIFA1	Reserved	SCIFB1	Reserved	SCIFB1	Reserved		I(Mode Pin)
P7	A19	DACK1	SCIFA1_TXD_C	-	SCIFB1_TXD_C	-	SCIFB1_SCK_B	-	GP1_3	3.3V/8mA
MD14	O(L)	O	O	-	O	-	IO	-	IO(I)	Off
329	LBSC	QSPI	Reserved	-	-	-	-	-		I(GPIO)
P6	A20	SPCLK	-	-	-	-	-	-	GP1_4	3.3V/8mA
	O(L)	IO	-	-	-	-	-	-	IO(I)	On
330	LBSC	LBSC	QSPI	Reserved	-	-	-	-		I(GPIO)
P5	A21	ATAWR0#_B	MOSI/IO0	-	-	-	-	-	GP1_5	3.3V/8mA
	O(L)	O	IO	-	-	-	-	-	IO(I)	On
331	LBSC	QSPI	Reserved	SCIF0	SCIFA0	Reserved	-	-		I(GPIO)
P4	A22	MISO/IO1	-	TX0	SCIFA0_TXD	-	-	-	GP1_6	3.3V/8mA
	O(L)	IO	-	O	O	-	-	-	IO(I)	On
332	LBSC	QSPI	Reserved	SCIF0	SCIFA0	Reserved	-	-		I(GPIO)
P3	A23	IO2	-	RX0	SCIFA0_RXD	-	-	-	GP1_7	3.3V/8mA
	O(L)	IO	-	I	I	-	-	-	IO(I)	On
333	LBSC	LBSC	QSPI	SCIF1	SCIFA1	Reserved	-	-		I(GPIO)
P2	A24	DREQ2	IO3	TX1	SCIFA1_TXD	-	-	-	GP1_8	3.3V/8mA
	O(L)	I	IO	O	O	-	-	-	IO(I)	On
334	LBSC	LBSC	QSPI	LBSC	SCIF1	SCIFA1	-	-		I(GPIO)
P1	A25	DACK2	SSL	DREQ1_C	RX1	SCIFA1_RXD	-	-	GP1_9	3.3V/8mA
	O(L)	O	IO	I	I	I	-	-	IO(I)	On
335	LBSC	-	-	-	-	-	-	-		O
U1	CLKOUT	-	-	-	-	-	-	-	-	3.3V/8mA
	O	-	-	-	-	-	-	-	-	-
336	LBSC	LBSC	I2C1	-	-	-	-	-		I(GPIO)
T1	CS0#	ATAG0#_B	I2C1_SCL	-	-	-	-	-	GP1_10	3.3V/4mA
	O(H)	O	IO	-	-	-	-	-	IO(I)	On
337	LBSC	LBSC	I2C1	-	-	-	-	-		I(GPIO)
R1	CS1#/A26	ATADIR0#_B	I2C1_SDA	-	-	-	-	-	GP1_11	3.3V/4mA
	O(H/L)*1	O	IO	-	-	-	-	-	IO(I)	On
338*2	LBSC	-	-	-	-	-	-	-		I(GPIO)
V1	EX_CS0#	-	-	-	-	-	-	-	GP1_12	3.3V/4mA
	O	-	-	-	-	-	-	-	IO(I)	Off
339*2	LBSC	MSIOF2	Reserved	-	-	-	-	-		I(GPIO)
N1	EX_CS1#	MSIOF2_SCK	-	-	-	-	-	-	GP1_13	3.3V/8mA
	O	IO	-	-	-	-	-	-	IO(I)	On
340*2	LBSC	LBSC	MSIOF	Reserved	-	-	-	-		I(GPIO)
N2	EX_CS2#	ATAWR0#	MSIOF2_SYNC	-	-	-	-	-	GP1_14	3.3V/4mA
	O	O	IO	-	-	-	-	-	IO(I)	On
341*2	LBSC	LBSC	MSIOF	LBSC	Reserved	LBSC	-	-		I(Mode Pin)
V3	EX_CS3#	ATADIR0#	MSIOF2_TXD	ATAG0#	-	EX_WAIT1	-	-	GP1_15	3.3V/4mA
MD9	O	O	O	O	-	I	-	-	IO(I)	Off
342*2	LBSC	LBSC	MSIOF	Reserved	LBSC	Reserved	-	-		I(GPIO)
V4	EX_CS4#	ATARD0#	MSIOF2_RXD	-	EX_WAIT2	-	-	-	GP1_16	3.3V/4mA
	O	O	I	-	I	-	-	-	IO(I)	On
343*2	LBSC	LBSC	MSIOF	HSCIF1	SCIFB1	PWM1	TPU	Reserved		I(Mode Pin)
V5	EX_CS5#	ATACS00#	MSIOF2_SS1	HRX1_B	SCIFB1_RXD_B	PWM1	TPU_TO1	-	GP1_17	3.3V/4mA
MD8	O	O	O	I	I	O	O	-	IO(I)	Off

Notes: 1. (No.337): Output value of CS1#/A26 pin after power-on reset is 'H' when MD4 = 0, 'L' when MD4 = 1.
2. (No.338 to 343): These pins are set for GPIO even if MD[3:1] = 000 after power-on reset. For details, refer to GPSR1 register in section 5, Pin Function Controller (PFC).

LBSC, MSIOF, I2C, SCIFA, SCIFB, QSPI, SCIF, HSCIF, PWM, TPU, GPIO (No.344 to 360): Up to 9-Function Multiplexed and Mode Pins assigned (No.344, 345, 347, 348, 351)

These pins default function (function 1 or GPIO) after power-on reset depends on MD[3:1] pins setting except for No.346 and 350 to 360 pins.

	Function									
	1	2	3	4	5	6	7	8	GPIO	
	MD[3:1]=000								MD[3:1]≠000	
No.	Module									During POR
Pin No.	Pin Name									V/|IOH|
Mode Pin	I/O									Pull-up
344	LBSC	LBSC	MSIOF2	HSCIF1	SCIFB1	PWM2	TPU	Reserved		I(Mode Pin)
N3	BS#	ATACS10#	MSIOF2_SS2	HTX1_B	SCIFB1_TXD_B	PWM2	TPU_TO2	-	GP1_18	3.3V/4mA
MD10	O(H)	O	O	O	O	O	O	-	IO(I)	Off
345	LBSC	-	-	-	-	-	-	-		I(Mode Pin)
V2	RD#	-	-	-	-	-	-	-	GP1_19	3.3V/4mA
MD12	O(H)	-	-	-	-	-	-	-	IO(I)	Off
346*	LBSC	HSCIF2	Reserved	SCIFB0	LBSC	HSCIF2	-	-		I(GPIO)
N4	RD/WR#	HRX2_B	-	SCIFB0_RXD_B	DREQ1_D	HRX2_D	-	-	GP1_20	3.3V/4mA
	O	I	-	I	I	I	-	-	IO(I)	On
347	LBSC	HSCIF2	SCIFB0	-	-	-	-	-		I(Mode Pin)
N5	WE0#	HCTS2#_B	SCIFB0_TXD_B	-	-	-	-	-	GP1_21	3.3V/4mA
MD6	O(H)	IO	O	-	-	-	-	-	IO(I)	Off
348	LBSC	LBSC	HSCIF2	SCIFB0	-	-	-	-		I(Mode Pin)
N6	WE1#	ATARD0#_B	HTX2_B	SCIFB0_RTS#_B	-	-	-	-	GP1_22	3.3V/4mA
MD4	O(H)	O	O	O	-	-	-	-	IO(I)	Off
349	LBSC	HSCIF2	SCIFB0	-	-	-	-	-		I(GPIO)
U3	EX_WAIT0	HRTS2#_B	SCIFB0_CTS#_B	-	-	-	-	-	GP1_23	3.3V/4mA
	I(I)	IO	I	-	-	-	-	-	IO(I)	On
350*	LBSC	PWM3	TPU	-	-	-	-	-		I(GPIO)
U4	DREQ0	PWM3	TPU_TO3	-	-	-	-	-	GP1_24	3.3V/4mA
	I	O	O	-	-	-	-	-	IO(I)	On
351*	LBSC	LBSC	Reserved	-	-	-	-	-		I(Mode Pin)
N7	DACK0	DRACK0	-	-	-	-	-	-	GP1_25	3.3V/4mA
MD7	O	O	-	-	-	-	-	-	IO(I)	Off
352*	Reserved	Reserved	HSCIF0	HSCIF2	SCIFB0	SCIFB2	LBSC	HSCIF2		I(GPIO)
T25	-	-	HSCK0_C	HSCK2_C	SCIFB0_SCK_B	SCIFB2_SCK_B	DREQ2_C	HTX2_D	GP5_31	3.3V/4mA
	-	-	IO	IO	O	O	I	O	IO(I)	On
353*	SSI	HSCIF0	HSCIF2	SCIFB0	SCIFB2	-	-	-		I(GPIO)
V31	SSI_SCK0129	HRX0_C	HRX2_C	SCIFB0_RXD_C	SCIFB2_RXD_C	-	-	-	GP2_0	3.3V/8mA
	IO	I	I	I	I	-	-	-	IO(I)	On
354*	SSI	HSCIF0	HSCIF2	SCIFB0	SCIFB2	-	-	-		I(GPIO)
V30	SSI_WS0129	HTX0_C	HTX2_C	SCIFB0_TXD_C	SCIFB2_TXD_C	-	-	-	GP2_1	3.3V/8mA
	IO	O	O	O	O	-	-	-	IO(I)	On
355*	SSI	I2C0	IIC0(I2C7)	MSIOF2	-	-	-	-		I(GPIO)
V29	SSI_SDATA0	I2C0_SCL_B	IIC0_SCL_B	MSIOF2_SCK_C	-	-	-	-	GP2_2	3.3V/8mA
	IO	IO	IO	IO	-	-	-	-	IO(I)	On
356*	SSI	I2C0	IIC0(I2C7)	MSIOF2	Reserved	-	-	-		I(GPIO)
W31	SSI_SCK1	I2C0_SDA_B	IIC0_SDA_B	MSIOF2_SYNC_C	-	-	-	-	GP2_3	3.3V/8mA
	IO	IO	IO	IO	-	-	-	-	IO(I)	On
357*	SSI	I2C1	IIC1(I2C8)	MSIOF2	Reserved	-	-	-		I(GPIO)
V28	SSI_WS1	I2C1_SCL_B	IIC1_SCL_B	MSIOF2_TXD_C	-	-	-	-	GP2_4	3.3V/8mA
	IO	IO	IO	O	-	-	-	-	IO(I)	On
358*	SSI	I2C1	IIC1(I2C8)	MSIOF2	-	-	-	-		I(GPIO)
V27	SSI_SDATA1	I2C1_SDA_B	IIC1_SDA_B	MSIOF2_RXD_C	-	-	-	-	GP2_5	3.3V/8mA
	IO	IO	IO	I	-	-	-	-	IO(I)	On
359*	SSI	I2C2	Reserved	Reserved	HSCIF1	-	-	-		I(GPIO)
W30	SSI_SCK2	I2C2_SCL	-	-	HSCK1_E	-	-	-	GP2_6	3.3V/8mA
	IO	IO	-	-	IO	-	-	-	IO(I)	On
360*	SSI	I2C2	Reserved	SCIF2	Reserved	HSCIF1	Reserved	-		I(GPIO)
W29	SSI_WS2	I2C2_SDA	-	RX2_E	-	HCTS1#_E	-	-	GP2_7	3.3V/8mA
	IO	IO	-	I	-	IO	-	-	IO(I)	On

Note: * (No.346 and 350 to 360): These pins are set for GPIO even if MD[3:1] = 000 after power-on reset. For details, refer to GPSR1, GPSR2 and GPSR5 registers in section 5, Pin Function Controller (PFC).

SSI, SCIF, HSCIF, MSIOF, TSIF, VIN, RCAN and GPIO (No.361 to 380): Up to 8-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR2 register in section 5, Pin Function Controller (PFC).

	Function								
	1	2	3	4	5	6	7	GPIO	
No.	Module								During POR
Pin No.	Pin Name								V/|IOH|
	I/O								Pull-up
361	SSI	Reserved	SCIF2	HSCIF1	Reserved	-	-		I(GPIO)
W28	SSI_SDATA2	-	TX2_E	HRTS1#_E	-	-	-	GP2_8	3.3V/8mA
	IO	-	O	IO	-	-	-	IO(I)	On
362	SSI	Reserved	-	-	-	-	-		I(GPIO)
W27	SSI_SCK34	-	-	-	-	-	-	GP2_9	3.3V/8mA
	IO	-	-	-	-	-	-	IO(I)	On
363	SSI	Reserved	-	-	-	-	-		I(GPIO)
W26	SSI_WS34	-	-	-	-	-	-	GP2_10	3.3V/8mA
	IO	-	-	-	-	-	-	IO(I)	On
364	SSI	Reserved	-	-	-	-	-		I(GPIO)
W25	SSI_SDATA3	-	-	-	-	-	-	GP2_11	3.3V/8mA
	IO	-	-	-	-	-	-	IO(I)	On
365	SSI	Reserved	Reserved	-	-	-	-		I(GPIO)
Y31	SSI_SCK4	-	-	-	-	-	-	GP2_12	3.3V/8mA
	IO	-	-	-	-	-	-	IO(I)	Off
366	SSI	Reserved	Reserved	-	-	-	-		I(GPIO)
Y30	SSI_WS4	-	-	-	-	-	-	GP2_13	3.3V/8mA
	IO	-	-	-	-	-	-	IO(I)	Off
367	SSI	MSIOF2	Reserved	-	-	-	-		I(GPIO)
Y29	SSI_SDATA4	MSIOF2_SCK_D	-	-	-	-	-	GP2_14	3.3V/8mA
	IO	IO	-	-	-	-	-	IO(I)	On
368	SSI	MSIOF1	TSIF0	Reserved	MSIOF2	VIN1	Reserved		I(GPIO)
Y28	SSI_SCK5	MSIOF1_SCK_C	TS_SDATA0	-	MSIOF2_SYNC_D	VI1_R2_B	-	GP2_15	3.3V/8mA
	IO	IO	I	-	IO	I	-	IO(I)	On
369	SSI	MSIOF1	TSIF0	Reserved	MSIOF2	VIN1	Reserved		I(GPIO)
Y27	SSI_WS5	MSIOF1_SYNC_C	TS_SCK0	-	MSIOF2_TXD_D	VI1_R3_B	-	GP2_16	3.3V/8mA
	IO	IO	I	-	O	I	-	IO(I)	On
370	SSI	MSIOF1	TSIF0	Reserved	MSIOF2	VIN1	Reserved		I(GPIO)
Y26	SSI_SDATA5	MSIOF1_TXD_C	TS_SDEN0	-	MSIOF2_SS1_D	VI1_R4_B	-	GP2_17	3.3V/8mA
	IO	O	I	-	O	I	-	IO(I)	On
371	SSI	MSIOF1	TSIF0	Reserved	MSIOF2	VIN1	Reserved		I(GPIO)
AA31	SSI_SCK6	MSIOF1_RXD_C	TS_SPSYNC0	-	MSIOF2_RXD_D	VI1_R5_B	-	GP2_18	3.3V/8mA
	IO	I	I	-	I	I	-	IO(I)	On
372	SSI	Reserved	MSIOF2	VIN1	Reserved	-	-		I(GPIO)
AA30	SSI_WS6	-	MSIOF2_SS2_D	VI1_R6_B	-	-	-	GP2_19	3.3V/8mA
	IO	-	O	I	-	-	-	IO(I)	Off
373	SSI	Reserved	Reserved	VIN1	Reserved	-	-		I(GPIO)
AA29	SSI_SDATA6	-	-	VI1_R7_B	-	-	-	GP2_20	3.3V/8mA
	IO	-	-	I	-	-	-	IO(I)	Off
374	SSI	Reserved	Reserved	Reserved	-	-	-		I(GPIO)
AA27	SSI_SCK78	-	-	-	-	-	-	GP2_21	3.3V/8mA
	IO	-	-	-	-	-	-	IO(I)	Off
375	SSI	SCIF0	Reserved	Reserved	Reserved	-	-		I(GPIO)
AA26	SSI_WS78	TX0_D	-	-	-	-	-	GP2_22	3.3V/8mA
	IO	O	-	-	-	-	-	IO(I)	Off
376	SSI	SCIF0	Reserved	Reserved	-	-	-		I(GPIO)
Y25	SSI_SDATA7	RX0_D	-	-	-	-	-	GP2_23	3.3V/8mA
	IO	I	-	-	-	-	-	IO(I)	On
377	SSI	SCIF1	Reserved	Reserved	-	-	-		I(GPIO)
AA25	SSI_SDATA8	TX1_D	-	-	-	-	-	GP2_24	3.3V/8mA
	IO	O	-	-	-	-	-	IO(I)	On
378	SSI	SCIF1	Reserved	Reserved	-	-	-		I(GPIO)
AB31	SSI_SCK9	RX1_D	-	-	-	-	-	GP2_25	3.3V/8mA
	IO	I	-	-	-	-	-	IO(I)	Off
379	SSI	SCIF3	RCAN0	Reserved	Reserved	Reserved	-		I(GPIO)
AB30	SSI_WS9	TX3_D	CAN0_TX_D	-	-	-	-	GP2_26	3.3V/8mA
	IO	O	O	-	-	-	-	IO(I)	Off
380	SSI	SCIF3	RCAN0	Reserved	Reserved	-	-		I(GPIO)
AB29	SSI_SDATA9	RX3_D	CAN0_RX_D	-	-	-	-	GP2_27	3.3V/8mA
	IO	I	I	-	-	-	-	IO(I)	On

ADG, MSIOF, SCIF, SCU, SCIFB, SCIFA, INTC, I2C, HSCIF, DU, RCAN and GPIO (No.381 to 395): Up to 8-Function Multiplexed and Mode Pin assigned (No.384)

These pins are set for GPIO except for No.385 (NMI) after power-on reset. For details, refer to GPSR2 and GPSR7 registers in section 5, Pin Function Controller (PFC).

	Function								
	1	2	3	4	5	6	7	GPIO	
No.	Module								During POR
Pin No.	Pin Name								V/|IOH|
Mode Pin	I/O								Pull-up
381	ADG	-	-	-	-	-	-		I(GPIO)
AD31	AUDIO_CLKA	-	-	-	-	-	-	GP2_28	3.3V/8mA
	I	-	-	-	-	-	-	IO(I)	On
382	ADG	Reserved	MSIOF1	SCIF	SCU	Reserved	Reserved		I(GPIO)
AC30	AUDIO_CLKB	-	MSIOF1_SCK_B	SCIF_CLK	DVC_MUTE	-	-	GP2_29	3.3V/8mA
	I	-	IO	I	I	-	-	IO(I)	On
383	ADG	SCIFB0	MSIOF1	SCIF2	SCIFA2	Reserved	Reserved		I(GPIO)
AD30	AUDIO_CLKC	SCIFB0_SCK_C	MSIOF1_SYNC_B	RX2	SCIFA2_RXD	-	-	GP2_30	3.3V/8mA
	I	O	IO	I	I	-	-	IO(I)	On
384	ADG	MSIOF	SCIF2	SCIFA2	-	-	-		I(Mode Pin)
AE31	AUDIO_CLKOUT	MSIOF1_SS1_B	TX2	SCIFA2_TXD	-	-	-	GP2_31	3.3V/8mA
MD5	O	O	O	O	-	-	-	IO(I)	Off
385	INTC	-	-	-	-	-	-	-	I(S)
AL16	NMI	-	-	-	-	-	-	-	1.8V/-
	I(S)	-	-	-	-	-	-	-	-
386	INTC	SCIFB1	Reserved	-	-	-	-		I(GPIO)
AE30	IRQ0	SCIFB1_RXD_D	-	-	-	-	-	GP7_10	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
387	INTC	SCIFB1	Reserved	-	-	-	-		I(GPIO)
AE29	IRQ1	SCIFB1_SCK_C	-	-	-	-	-	GP7_11	3.3V/4mA
	I	O	-	-	-	-	-	IO(I)	On
388	INTC	SCIFB1	Reserved	-	-	-	-		I(GPIO)
AD29	IRQ2	SCIFB1_TXD_D	-	-	-	-	-	GP7_12	3.3V/4mA
	I	O	-	-	-	-	-	IO(I)	On
389	INTC	I2C4	MSIOF2	Reserved	-	-	-		I(GPIO)
AD28	IRQ3	I2C4_SCL_C	MSIOF2_TXD_E	-	-	-	-	GP7_13	3.3V/4mA
	I	IO	O	-	-	-	-	IO(I)	On
390	INTC	HSCIF1	I2C4	MSIOF2	HSCIF1	Reserved	-		I(GPIO)
AC29	IRQ4	HRX1_C	I2C4_SDA_C	MSIOF2_RXD_E	HRX1_E	-	-	GP7_14	3.3V/4mA
	I	I	IO	I	I	-	-	IO(I)	On
391	INTC	HSCIF1	I2C1	MSIOF2	HSCIF1	-	-		I(GPIO)
AC28	IRQ5	HTX1_C	I2C1_SCL_E	MSIOF2_SCK_E	HTX1_E	-	-	GP7_15	3.3V/8mA
	I	O	IO	IO	O	-	-	IO(I)	On
392	INTC	HSCIF1	MSIOF1	I2C1	MSIOF2	-	-		I(GPIO)
AC27	IRQ6	HSCK1_C	MSIOF1_SS2_B	I2C1_SDA_E	MSIOF2_SYNC_E	-	-	GP7_16	3.3V/4mA
	I	IO	O	IO	IO	-	-	IO(I)	On
393	INTC	HSCIF1	MSIOF1	Reserved	Reserved	-	-		I(GPIO)
AB26	IRQ7	HCTS1#_C	MSIOF1_TXD_B	-	-	-	-	GP7_17	3.3V/4mA
	I	IO	O	-	-	-	-	IO(I)	On
394	INTC	HSCIF1	MSIOF1	Reserved	Reserved	-	-		I(GPIO)
AB27	IRQ8	HRTS1#_C	MSIOF1_RXD_B	-	-	-	-	GP7_18	3.3V/4mA
	I	IO	I	-	-	-	-	IO(I)	On
395	INTC	DU1	RCAN	Reserved	SCIF	Reserved	-		I(GPIO)
AB28	IRQ9	DU1_DOTCLKIN_B	CAN_CLK_D	-	SCIF_CLK_B	-	-	GP7_19	3.3V/4mA
	I	I	I	-	I	-	-	IO(I)	On

DU, VIN, SCIF, MSIOF, SSI, HSCIF, RCAN and GPIO (No.396 to 415): Up to 7-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR3 register in section 5, Pin Function Controller (PFC).

	Function							
	1	2	3	4	5	6	GPIO	
No.	Module							During POR
Pin No.	Pin Name							V/|IOH|
	I/O							Pull-up
396	DU1	Reserved	VIN1	SCIF0	SCIFA0	MSIOF2		I(GPIO)
AL12	DU1_DR0	-	VI1_DATA0_B	TX0_B	SCIFA0_TXD_B	MSIOF2_SCK_B	GP3_0	3.3V/8mA
	O	-	I	O	O	IO	IO(I)	On
397	DU1	Reserved	VIN1	SCIF0	SCIFA0	MSIOF2		I(GPIO)
AK12	DU1_DR1	-	VI1_DATA1_B	RX0_B	SCIFA0_RXD_B	MSIOF2_SYNC_B	GP3_1	3.3V/8mA
	O	-	I	I	I	IO	IO(I)	On
398	DU1	Reserved	SSI	-	-	-		I(GPIO)
AJ12	DU1_DR2	-	SSI_SCK0129_B	-	-	-	GP3_2	3.3V/8mA
	O	-	IO	-	-	-	IO(I)	On
399	DU1	Reserved	SSI	-	-	-		I(GPIO)
AH12	DU1_DR3	-	SSI_WS0129_B	-	-	-	GP3_3	3.3V/8mA
	O	-	IO	-	-	-	IO(I)	On
400	DU1	Reserved	SSI	-	-	-		I(GPIO)
AG12	DU1_DR4	-	SSI_SDATA0_B	-	-	-	GP3_4	3.3V/8mA
	O	-	IO	-	-	-	IO(I)	On
401	DU1	Reserved	SSI	-	-	-		I(GPIO)
AF12	DU1_DR5	-	SSI_SCK1_B	-	-	-	GP3_5	3.3V/8mA
	O	-	IO	-	-	-	IO(I)	On
402	DU1	Reserved	SSI	-	-	-		I(GPIO)
AE12	DU1_DR6	-	SSI_WS1_B	-	-	-	GP3_6	3.3V/8mA
	O	-	IO	-	-	-	IO(I)	On
403	DU1	Reserved	SSI	-	-	-		I(GPIO)
AE11	DU1_DR7	-	SSI_SDATA1_B	-	-	-	GP3_7	3.3V/8mA
	O	-	IO	-	-	-	IO(I)	On
404	DU1	Reserved	VIN1	SCIF1	SCIFA1	MSIOF2		I(GPIO)
AL11	DU1_DG0	-	VI1_DATA2_B	TX1_B	SCIFA1_TXD_B	MSIOF2_SS1_B	GP3_8	3.3V/8mA
	O	-	I	O	O	O	IO(I)	On
405	DU1	Reserved	VIN1	SCIF1	SCIFA1	MSIOF2		I(GPIO)
AK11	DU1_DG1	-	VI1_DATA3_B	RX1_B	SCIFA1_RXD_B	MSIOF2_SS2_B	GP3_9	3.3V/8mA
	O	-	I	I	I	O	IO(I)	On
406	DU1	Reserved	VIN1	SCIF1	SCIFA1	SSI		I(GPIO)
AJ11	DU1_DG2	-	VI1_DATA4_B	SCIF1_SCK_B	SCIFA1_SCK	SSI_SCK78_B	GP3_10	3.3V/8mA
	O	-	I	IO	O	IO	IO(I)	On
407	DU1	Reserved	VIN1	Reserved	SSI	-		I(GPIO)
AH11	DU1_DG3	-	VI1_DATA5_B	-	SSI_WS78_B	-	GP3_11	3.3V/8mA
	O	-	I	-	IO	-	IO(I)	On
408	DU1	Reserved	VIN1	HSCIF0	SCIFB2	SSI		I(GPIO)
AG11	DU1_DG4	-	VI1_DATA6_B	HRX0_B	SCIFB2_RXD_B	SSI_SDATA7_B	GP3_12	3.3V/8mA
	O	-	I	I	I	IO	IO(I)	On
409	DU1	Reserved	VIN1	HSCIF0	SCIFB2	SSI		I(GPIO)
AF11	DU1_DG5	-	VI1_DATA7_B	HCTS0#_B	SCIFB2_TXD_B	SSI_SDATA8_B	GP3_13	3.3V/8mA
	O	-	I	IO	O	IO	IO(I)	On
410	DU1	Reserved	HSCIF0	SCIFB2	SSI	-		I(GPIO)
AF10	DU1_DG6	-	HRTS0#_B	SCIFB2_CTS#_B	SSI_SCK9_B	-	GP3_14	3.3V/8mA
	O	-	IO	I	IO	-	IO(I)	On
411	DU1	Reserved	HSCIF0	SCIFB2	SSI	-		I(GPIO)
AE10	DU1_DG7	-	HTX0_B	SCIFB2_RTS#_B	SSI_WS9_B	-	GP3_15	3.3V/8mA
	O	-	O	O	IO	-	IO(I)	On
412	DU1	Reserved	VIN1	SCIF2	SCIFA2	MSIOF2		I(GPIO)
AJ9	DU1_DB0	-	VI1_CLK_B	TX2_B	SCIFA2_TXD_B	MSIOF2_TXD_B	GP3_16	3.3V/8mA
	O	-	I	O	O	O	IO(I)	On
413	DU1	Reserved	VIN1	SCIF2	SCIFA2	MSIOF2		I(GPIO)
AH9	DU1_DB1	-	VI1_HSYNC#_B	RX2_B	SCIFA2_RXD_B	MSIOF2_RXD_B	GP3_17	3.3V/8mA
	O	-	I	I	I	I	IO(I)	On
414	DU1	Reserved	VIN1	SCIF2	SCIFA2	SSI		I(GPIO)
AG9	DU1_DB2	-	VI1_VSYNC#_B	SCIF2_SCK_B	SCIFA2_SCK	SSI_SDATA9_B	GP3_18	3.3V/8mA
	O	-	I	IO	O	IO	IO(I)	On
415	DU1	Reserved	VIN1	Reserved	-	-		I(GPIO)
AF9	DU1_DB3	-	VI1_CLKENB_B	-	-	-	GP3_19	3.3V/8mA
	O	-	I	-	-	-	IO(I)	On

DU, I2C, SCIF, SCIFA, RCAN, PWM, TSIF and GPIO (No.416 to 435): Up to 8-Function Multiplexed and Mode Pins assigned (No.417, 423, 426, 427)

These pins are set for GPIO after power-on reset. For details, refer to GPSR3 and GPSR4 registers in section 5, Pin Function Controller (PFC).

	Function								
	1	2	3	4	5	6	7	GPIO	
No.	Module								During POR
Pin No.	Pin Name								V/|IOH|
Mode Pin	I/O								Pull-up
416	DU1	Reserved	VIN1	RCAN1	-	-	-		I(GPIO)
AE9	DU1_DB4	-	VI1_FIELD_B	CAN1_RX	-	-	-	GP3_20	3.3V/8mA
	O	-	I	I	-	-	-	IO(I)	On
417	DU1	Reserved	SCIF3	SCIFA3	RCAN1	Reserved	-		I(Mode Pin)
AJ10	DU1_DB5	-	TX3	SCIFA3_TXD	CAN1_TX	-	-	GP3_21	3.3V/8mA
MD11	O	-	O	O	O	-	-	IO(I)	Off
418	DU1	Reserved	I2C3	SCIF3	SCIFA3	Reserved	-		I(GPIO)
AH10	DU1_DB6	-	I2C3_SCL_C	RX3	SCIFA3_RXD	-	-	GP3_22	3.3V/8mA
	O	-	IO	I	I	-	-	IO(I)	On
419	DU1	Reserved	I2C3	SCIF3	SCIFA3	Reserved	-		I(GPIO)
AG10	DU1_DB7	-	I2C3_SDA_C	SCIF3_SCK	SCIFA3_SCK	-	-	GP3_23	3.3V/8mA
	O	-	IO	IO	O	-	-	IO(I)	On
420	DU1	Reserved	-	-	-	-	-		I(GPIO)
AL9	DU1_DOTCLKIN	-	-	-	-	-	-	GP3_24	3.3V/8mA
	I	-	-	-	-	-	-	IO(I)	On
421	DU1	Reserved	-	-	-	-	-		I(GPIO)
AL10	DU1_DOTCLKOUT0	-	-	-	-	-	-	GP3_25	3.3V/8mA
	O	-	-	-	-	-	-	IO(I)	On
422	DU1	Reserved	RCAN0	SCIF3	I2C2	PWM4	Reserved		I(GPIO)
AK10	DU1_DOTCLKOUT1	-	CAN0_TX	TX3_B	I2C2_SCL_B	PWM4	-	GP3_26	3.3V/8mA
	O	-	O	O	IO	O	-	IO(I)	On
423	DU1	Reserved	-	-	-	-	-		I(Mode Pin)
AE8	DU1_EXHSYNC/DU1_HSYNC	-	-	-	-	-	-	GP3_27	3.3V/8mA
MD3	IO	-	-	-	-	-	-	IO(I)	Off
424	DU1	Reserved	-	-	-	-	-		I(Mode Pin)
AF8	DU1_EXVSYNC/DU1_VSYNC	-	-	-	-	-	-	GP3_28	3.3V/8mA
MD2	IO	-	-	-	-	-	-	IO(I)	Off
425	DU1	Reserved	RCAN0	SCIF3	I2C2	Reserved	-		I(GPIO)
AG8	DU1_EXODDF/DU1_ODDF/DISP/CDE	-	CAN0_RX	RX3_B	I2C2_SDA_B	-	-	GP3_29	3.3V/8mA
	IO	-	I	I	IO	-	-	IO(I)	On
426	DU1	Reserved	-	-	-	-	-		I(Mode Pin)
AH8	DU1_DISP	-	-	-	-	-	-	GP3_30	3.3V/8mA
MD1	O	-	-	-	-	-	-	IO(I)	Off
427	DU1	Reserved	PWM4	-	-	-	-		I(Mode Pin)
AJ8	DU1_CDE	-	PWM4_B	-	-	-	-	GP3_31	3.3V/8mA
MD0	O	-	O	-	-	-	-	IO(I)	Off
428	VIN0	-	-	-	-	-	-		I(GPIO)
AC1	VI0_CLK	-	-	-	-	-	-	GP4_0	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
429	VIN0	SCIF4	SCIFA4	TSIF0	-	-	-		I(GPIO)
AB1	VI0_CLKENB	TX4	SCIFA4_TXD	TS_SDATA0_D	-	-	-	GP4_1	3.3V/4mA
	I	O	O	I	-	-	-	IO(I)	On
430	VIN0	SCIF4	SCIFA4	TSIF0	-	-	-		I(GPIO)
AC2	VI0_FIELD	RX4	SCIFA4_RXD	TS_SCK0_D	-	-	-	GP4_2	3.3V/4mA
	I	I	I	I	-	-	-	IO(I)	On
431	VIN0	SCIF5	SCIFA5	TSIF0	-	-	-		I(GPIO)
AB2	VI0_HSYNC#	TX5	SCIFA5_TXD	TS_SDEN0_D	-	-	-	GP4_3	3.3V/4mA
	I	O	O	I	-	-	-	IO(I)	On
432	VIN0	SCIF5	SCIFA5	TSIF0	-	-	-		I(GPIO)
AB3	VI0_VSYNC#	RX5	SCIFA5_RXD	TS_SPSYNC0_D	-	-	-	GP4_4	3.3V/4mA
	I	I	I	I	-	-	-	IO(I)	On
433	VIN0	-	-	-	-	-	-		I(GPIO)
AB4	VI0_DATA0/VI0_B0	-	-	-	-	-	-	GP4_5	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
434	VIN0	-	-	-	-	-	-		I(GPIO)
AB5	VI0_DATA1/VI0_B1	-	-	-	-	-	-	GP4_6	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
435	VIN0	-	-	-	-	-	-		I(GPIO)
AB6	VI0_DATA2/VI0_B2	-	-	-	-	-	-	GP4_7	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On

VIN, I2C, HSCIF, SCIFB, LBSC, RCAN and GPIO (No.436 to 455): Up to 8-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR4 register in section 5, Pin Function Controller (PFC).

	Function								
	1	2	3	4	5	6	7	GPIO	
No.	Module								During POR
Pin No.	Pin Name								V/|IOH|
	I/O								Pull-up
436	VIN0	SCIF3	SCIFA3	Reserved	-	-	-		I(GPIO)
AC3	VI0_DATA3/VI0_B3	SCIF3_SCK_B	SCIFA3_SCK_B	-	-	-	-	GP4_8	3.3V/4mA
	I	IO	O	-	-	-	-	IO(I)	On
437	VIN0	-	-	-	-	-	-		I(GPIO)
AB7	VI0_DATA4/VI0_B4	-	-	-	-	-	-	GP4_9	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
438	VIN0	-	-	-	-	-	-		I(GPIO)
AC4	VI0_DATA5/VI0_B5	-	-	-	-	-	-	GP4_10	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
439	VIN0	-	-	-	-	-	-		I(GPIO)
AC6	VI0_DATA6/VI0_B6	-	-	-	-	-	-	GP4_11	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
440	VIN0	-	-	-	-	-	-		I(GPIO)
AC7	VI0_DATA7/VI0_B7	-	-	-	-	-	-	GP4_12	3.3V/4mA
	I	-	-	-	-	-	-	IO(I)	On
441	VIN0	IIC1(I2C8)	Reserved	I2C4	HSCIF2	SCIFB2	LBSC		I(GPIO)
AD1	VI0_G0	IIC1_SCL	-	I2C4_SCL	HCTS2#	SCIFB2_CTS#	ATAWR1#	GP4_13	3.3V/4mA
	I	IO	-	IO	IO	I	O	IO(I)	On
442	VIN0	IIC1(I2C8)	Reserved	I2C4	HSCIF2	SCIFB2	LBSC		I(GPIO)
AD2	VI0_G1	IIC1_SDA	-	I2C4_SDA	HRTS2#	SCIFB2_RTS#	ATADIR1#	GP4_14	3.3V/4mA
	I	IO	-	IO	IO	O	O	IO(I)	On
443	VIN0	VIN2	Reserved	I2C3	HSCIF2	SCIFB2	LBSC		I(GPIO)
AD3	VI0_G2	VI2_HSYNC#	-	I2C3_SCL_B	HSCK2	SCIFB2_SCK	ATARD1#	GP4_15	3.3V/4mA
	I	I	-	IO	IO	O	O	IO(I)	On
444	VIN0	VIN2	Reserved	I2C3	HSCIF2	SCIFB2	LBSC		I(GPIO)
AD4	VI0_G3	VI2_VSYNC#	-	I2C3_SDA_B	HRX2	SCIFB2_RXD	ATACS01#	GP4_16	3.3V/4mA
	I	I	-	IO	I	I	O	IO(I)	On
445	VIN0	VIN2	Reserved	HSCIF2	SCIFB2	SCIFB0	-		I(GPIO)
AD5	VI0_G4	VI2_CLKENB	-	HTX2	SCIFB2_TXD	SCIFB0_SCK_D	-	GP4_17	3.3V/4mA
	I	I	-	O	O	O	-	IO(I)	On
446	VIN0	VIN2	Reserved	Reserved	RCAN0	HSCIF1	SCIFB0		I(GPIO)
AD6	VI0_G5	VI2_FIELD	-	-	CAN0_TX_E	HTX1_D	SCIFB0_TXD_D	GP4_18	3.3V/4mA
	I	I	-	-	O	O	O	IO(I)	On
447	VIN0	VIN2	Reserved	-	-	-	-		I(GPIO)
AE6	VI0_G6	VI2_CLK	-	-	-	-	-	GP4_19	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
448	VIN0	VIN2	Reserved	-	-	-	-		I(GPIO)
AD7	VI0_G7	VI2_DATA0	-	-	-	-	-	GP4_20	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
449	VIN0	VIN2	Reserved	TSIF0	LBSC	-	-		I(GPIO)
AE1	VI0_R0	VI2_DATA1	-	TS_SDATA0_C	ATACS11#	-	-	GP4_21	3.3V/4mA
	I	I	-	I	O	-	-	IO(I)	On
450	VIN0	VIN2	Reserved	TSIF0	LBSC	-	-		I(GPIO)
AE3	VI0_R1	VI2_DATA2	-	TS_SCK0_C	ATAG1#	-	-	GP4_22	3.3V/4mA
	I	I	-	I	O	-	-	IO(I)	On
451	VIN0	VIN2	Reserved	TSIF0	-	-	-		I(GPIO)
AE4	VI0_R2	VI2_DATA3	-	TS_SDEN0_C	-	-	-	GP4_23	3.3V/4mA
	I	I	-	I	-	-	-	IO(I)	On
452	VIN0	VIN2	Reserved	TSIF0	-	-	-		I(GPIO)
AE5	VI0_R3	VI2_DATA4	-	TS_SPSYNC0_C	-	-	-	GP4_24	3.3V/4mA
	I	I	-	I	-	-	-	IO(I)	On
453	VIN0	VIN2	Reserved	SCIF0	I2C1	-	-		I(GPIO)
AF3	VI0_R4	VI2_DATA5	-	TX0_C	I2C1_SCL_D	-	-	GP4_25	3.3V/4mA
	I	I	-	O	IO	-	-	IO(I)	Off
454	VIN0	VIN2	Reserved	SCIF0	I2C1	-	-		I(GPIO)
AF4	VI0_R5	VI2_DATA6	-	RX0_C	I2C1_SDA_D	-	-	GP4_26	3.3V/4mA
	I	I	-	I	IO	-	-	IO(I)	Off
455	VIN0	VIN2	Reserved	SCIF1	I2C4	-	-		I(GPIO)
AF5	VI0_R6	VI2_DATA7	-	TX1_C	I2C4_SCL_B	-	-	GP4_27	3.3V/4mA
	I	I	-	O	IO	-	-	IO(I)	Off

VIN, EtherAVB, TSIF, I2C, RCAN, MSIOF, SCIFA, TMU and GPIO (No.456 to 475): Up to 8-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR5 register in section 5, Pin Function Controller (PFC).

	Function								
	1	2	3	4	5	6	7	GPIO	
No.	Module								During POR
Pin No.	Pin Name								V/|IOH|
	I/O								Pull-up
456	VIN0	Reserved	SCIF1	RCAN0	I2C4	HSCIF1	SCIFB0		I(GPIO)
AG4	VI0_R7	-	RX1_C	CAN0_RX_E	I2C4_SDA_B	HRX1_D	SCIFB0_RXD_D	GP4_28	3.3V/4mA
	I	-	I	I	IO	I	I	IO(I)	Off
457	VIN1	EtherAVB	TSIF0	SCIF4	SCIFA4	-	-		I(GPIO)
AF1	VI1_HSYNC#	AVB_RXD0	TS_SDATA0_B	TX4_B	SCIFA4_TXD_B	-	-	GP5_0	3.3V/4mA
	I	I	I	O	O	-	-	IO(I)	On
458	VIN1	EtherAVB	TSIF0	SCIF4	SCIFA4	-	-		I(GPIO)
AF2	VI1_VSYNC#	AVB_RXD1	TS_SCK0_B	RX4_B	SCIFA4_RXD_B	-	-	GP5_1	3.3V/4mA
	I	I	I	I	I	-	-	IO(I)	On
459	VIN1	EtherAVB	TSIF0	-	-	-	-		I(GPIO)
AG3	VI1_CLKENB	AVB_RXD2	TS_SDEN0_B	-	-	-	-	GP5_2	3.3V/4mA
	I	I	I	-	-	-	-	IO(I)	On
460	VIN1	EtherAVB	TSIF0	-	-	-	-		I(GPIO)
AH2	VI1_FIELD	AVB_RXD3	TS_SPSYNC0_B	-	-	-	-	GP5_3	3.3V/4mA
	I	I	I	-	-	-	-	IO(I)	On
461	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AG1	VI1_CLK	AVB_RXD4	-	-	-	-	-	GP5_4	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
462	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AH3	VI1_DATA0	AVB_RXD5	-	-	-	-	-	GP5_5	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
463	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AH1	VI1_DATA1	AVB_RXD6	-	-	-	-	-	GP5_6	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
464	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AJ1	VI1_DATA2	AVB_RXD7	-	-	-	-	-	GP5_7	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
465	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AJ2	VI1_DATA3	AVB_RX_ER	-	-	-	-	-	GP5_8	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
466	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AK1	VI1_DATA4	AVB_MDIO	-	-	-	-	-	GP5_9	3.3V/8mA
	I	IO	-	-	-	-	-	IO(I)	On
467	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AL2	VI1_DATA5	AVB_RX_DV	-	-	-	-	-	GP5_10	3.3V/4mA
	I	I	-	-	-	-	-	IO(I)	On
468	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AK3	VI1_DATA6	AVB_MAGIC	-	-	-	-	-	GP5_11	3.3V/8mA
	I	O	-	-	-	-	-	IO(I)	On
469	VIN1	EtherAVB	-	-	-	-	-		I(GPIO)
AJ4	VI1_DATA7	AVB_MDC	-	-	-	-	-	GP5_12	3.3V/8mA
	I	O	-	-	-	-	-	IO(I)	On
470	EtherMAC	EtherAVB	I2C2	-	-	-	-		I(GPIO)
AL3	ETH_MDIO	AVB_RX_CLK	I2C2_SCL_C	-	-	-	-	GP5_13	3.3V/4mA
	IO	I	IO	-	-	-	-	IO(I)	On
471	EtherMAC	EtherAVB	I2C2	-	-	-	-		I(GPIO)
AK4	ETH_CRS_DV	AVB_LINK	I2C2_SDA_C	-	-	-	-	GP5_14	3.3V/4mA
	I	I	IO	-	-	-	-	IO(I)	On
472	EtherMAC	EtherAVB	I2C3	IIC0(I2C7)	-	-	-		I(GPIO)
AL4	ETH_RX_ER	AVB_CRS	I2C3_SCL	IIC0_SCL	-	-	-	GP5_15	3.3V/4mA
	I	I	IO	IO	-	-	-	IO(I)	On
473	EtherMAC	EtherAVB	I2C3	IIC0(I2C7)	-	-	-		I(GPIO)
AH5	ETH_RXD0	AVB_PHY_INT	I2C3_SDA	IIC0_SDA	-	-	-	GP5_16	3.3V/4mA
	I	I	IO	IO	-	-	-	IO(I)	On
474	EtherMAC	EtherAVB	RCAN0	I2C2	MSIOF1	-	-		I(GPIO)
AL5	ETH_RXD1	AVB_GTXREFCLK	CAN0_TX_C	I2C2_SCL_D	MSIOF1_RXD_E	-	-	GP5_17	3.3V/4mA
	I	I	O	IO	I	-	-	IO(I)	On
475	EtherMAC	EtherAVB	RCAN0	I2C2	MSIOF1	-	-		I(GPIO)
AH6	ETH_LINK	AVB_TXD0	CAN0_RX_C	I2C2_SDA_D	MSIOF1_SCK_E	-	-	GP5_18	3.3V/8mA
	I	O	I	IO	IO	-	-	IO(I)	On

EtherMAC, EtherAVB, SCIFA, RCAN, MSIOF, TMU, SCIFB, PWM, SDHI, QSPI, MMC, USB2.0 and GPIO (No.476 to 495): Up to 9-Function Multiplexed

These pins are set for GPIO after power-on reset except for QSPI pin during QSPI boot operation. For details, refer to GPSR5 and GPSR6 registers in section 5, PFC and section 18, Booting.

	Function									
	1	2	3	4	5	6	7	8	GPIO	
No.	Module									During POR
Pin No.	Pin Name									V/|IOH|
	I/O									Pull-up
476	EtherMAC	EtherAVB	SCIFA3	RCAN1	MSIOF1	-	-	-		I(GPIO)
AL6	ETH_REFCLK	AVB_TXD1	SCIFA3_RXD_B	CAN1_RX_C	MSIOF1_SYNC_E	-	-	-	GP5_19	3.3V/8mA
	I	O	I	I	O	-	-	-	IO(I)	On
477	EtherMAC	EtherAVB	SCIFA3	RCAN1	MSIOF1	-	-	-		I(GPIO)
AJ5	ETH_TXD1	AVB_TXD2	SCIFA3_TXD_B	CAN1_TX_C	MSIOF1_TXD_E	-	-	-	GP5_20	3.3V/8mA
	O	O	O	O	O	-	-	-	IO(I)	On
478	EtherMAC	EtherAVB	TMU	RCAN	-	-	-	-		I(GPIO)
AG6	ETH_TX_EN	AVB_TXD3	TCLK1_B	CAN_CLK_B	-	-	-	-	GP5_21	3.3V/8mA
	O	O	I	I	-	-	-	-	IO(I)	On
479	EtherMAC	EtherAVB	Reserved	-	-	-	-	-		I(GPIO)
AJ6	ETH_MAGIC	AVB_TXD4	-	-	-	-	-	-	GP5_22	3.3V/8mA
	O	O	-	-	-	-	-	-	IO(I)	On
480	EtherMAC	EtherAVB	Reserved	-	-	-	-	-		I(GPIO)
AG7	ETH_TXD0	AVB_TXD5	-	-	-	-	-	-	GP5_23	3.3V/8mA
	O	O	-	-	-	-	-	-	IO(I)	On
481	EtherMAC	EtherAVB	Reserved	-	-	-	-	-		I(GPIO)
AF7	ETH_MDC	AVB_TXD6	-	-	-	-	-	-	GP5_24	3.3V/8mA
	O	O	-	-	-	-	-	-	IO(I)	On
482	Reserved	EtherAVB	SCIFB2	Reserved	MSIOF0	-	-	-		I(GPIO)
AK8	-	AVB_TXD7	SCIFB2_TXD_D	-	MSIOF0_SYNC_C	-	-	-	GP5_25	3.3V/8mA
	-	O	O	-	IO	-	-	-	IO(I)	On
483	Reserved	EtherAVB	SCIFB2	Reserved	MSIOF0	-	-	-		I(GPIO)
AL8	-	AVB_TX_EN	SCIFB2_RXD_D	-	MSIOF0_SCK_C	-	-	-	GP5_26	3.3V/8mA
	-	O	I	-	IO	-	-	-	IO(I)	On
484	Reserved	EtherAVB	SCIFB2	Reserved	MSIOF0	-	-	-		I(GPIO)
AH7	-	AVB_TX_ER	SCIFB2_SCK_C	-	MSIOF0_SS1_C	-	-	-	GP5_27	3.3V/8mA
	-	O	O	-	O	-	-	-	IO(I)	On
485	Reserved	EtherAVB	Reserved	MSIOF0	-	-	-	-		I(GPIO)
AJ7	-	AVB_TX_CLK	-	MSIOF0_SS2_C	-	-	-	-	GP5_28	3.3V/8mA
	-	I	-	O	-	-	-	-	IO(I)	On
486	Reserved	EtherAVB	Reserved	MSIOF0	-	-	-	-		I(GPIO)
AK7	-	AVB_COL	-	MSIOF0_RXD_C	-	-	-	-	GP5_29	3.3V/4mA
	-	I	-	I	-	-	-	-	IO(I)	On
487	Reserved	EtherAVB	PWM0	Reserved	MSIOF0	-	-	-		I(GPIO)
AL7	-	AVB_GTX_CLK	PWM0_B	-	MSIOF0_TXD_C	-	-	-	GP5_30	3.3V/8mA
	-	O	O	-	O	-	-	-	IO(I)	On
488	SDHI0	QSPI	-	-	-	-	-	-		I(GPIO)
AL15	SD0_CLK	SPCLK_B	-	-	-	-	-	-	GP6_0	1.8/3.3V*/16mA
	O	IO	-	-	-	-	-	-	IO(I)	Off
489	SDHI0	QSPI	-	-	-	-	-	-		I(GPIO)
AH16	SD0_CMD	MOSI/IO0_B	-	-	-	-	-	-	GP6_1	1.8/3.3V*/16mA
	IO	IO	-	-	-	-	-	-	IO(I)	Off
490	SDHI0	QSPI	-	-	-	-	-	-		I(GPIO)
AG16	SD0_DATA0	MISO/IO1_B	-	-	-	-	-	-	GP6_2	1.8/3.3V*/16mA
	IO	IO	-	-	-	-	-	-	IO(I)	Off
491	SDHI0	QSPI	-	-	-	-	-	-		I(GPIO)
AF16	SD0_DATA1	IO2_B	-	-	-	-	-	-	GP6_3	1.8/3.3V*/16mA
	IO	IO	-	-	-	-	-	-	IO(I)	Off
492	SDHI0	QSPI	-	-	-	-	-	-		I(GPIO)
AE16	SD0_DATA2	IO3_B	-	-	-	-	-	-	GP6_4	1.8/3.3V*/16mA
	IO	IO	-	-	-	-	-	-	IO(I)	Off
493	SDHI0	QSPI	-	-	-	-	-	-		I(GPIO)
AH15	SD0_DATA3	SSL_B	-	-	-	-	-	-	GP6_5	1.8/3.3V*/16mA
	IO	IO	-	-	-	-	-	-	IO(I)	Off
494	SDHI0	MMC	Reserved	RCAN0	SCIFA5	SCIF3	Reserved	Reserved		I(GPIO)
AJ15	SD0_CD	MMC_D6_B	-	CAN0_RX_F	SCIFA5_TXD_B	TX3_C	-	-	GP6_6	1.8/3.3V*/16mA
	I	IO	-	I	O	O	-	-	IO(I)	Off
495	SDHI0	MMC	Reserved	RCAN0	SCIFA5	SCIF3	Reserved	Reserved		I(GPIO)
AJ16	SD0_WP	MMC_D7_B	-	CAN0_TX_F	SCIFA5_RXD_B	RX3_C	-	-	GP6_7	1.8/3.3V*/16mA
	I	IO	-	O	I	I	-	-	IO(I)	Off

Note: * (No.488 to 495) V/|IOH|: Pin voltage is selectable (3.3V: default). For details, refer to IOCTRL6 register in section 5, Pin Function Controller (PFC).

SDHI, PWM, TPU, I2C, MMC, SCIF, SCIFA and GPIO (No.496 to 514): Up to 6-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR6 register in section 5, Pin Function Controller (PFC).

	Function 1	2	3	4	5	GPIO	
No.	**Module**						**During POR**
Pin No.	**Pin Name**						**V/|IOH|**
	I/O						**Pull-up**
496	SDHI0 Power	-	-	-	-		P
AD16	VCCQ_SD0	-	-	-	-	-	-
	P	-	-	-	-	-	-
497*	SDHI2	-	-	-	-		I(GPIO)/Z(DBG)*1
AL14	SD2_CLK	-	-	-	-	GP6_8	1.8/3.3V*2/16mA
	O	-	-	-	-	IO(I)	Off/-*
498*	SDHI2	Reserved	-	-	-		I(GPIO)/I(DBG)*
AH14	SD2_CMD	-	-	-	-	GP6_9	1.8/3.3V*2/16mA
	IO	-	-	-	-	IO(I)	Off/-*1
499*	SDHI2	Reserved	Reserved	-	-		I(GPIO)/I(DBG)*1
AG15	SD2_DATA0	-	-	-	-	GP6_10	1.8/3.3V*2/16mA
	IO	-	-	-	-	IO(I)	Off/-*1
500*	SDHI2	Reserved	-	-	-		I(GPIO)/I(DBG)*1
AF15	SD2_DATA1	-	-	-	-	GP6_11	1.8/3.3V*2/16mA
	IO	-	-	-	-	IO(I)	Off/-*1
501*	SDHI2	Reserved	-	-	-		I(GPIO)/I(DBG)*1
AE15	SD2_DATA2	-	-	-	-	GP6_12	1.8/3.3V*2/16mA
	IO	-	-	-	-	IO(I)	Off/-*1
502*	SDHI2	Reserved	-	-	-		I(GPIO)/I(DBG)*1
AG14	SD2_DATA3	-	-	-	-	GP6_13	1.8/3.3V*2/16mA
	IO	-	-	-	-	IO(I)	Off/-*1
503	SDHI2	PWM0	TPU	I2C1	Reserved		I(GPIO)
AJ14	SD2_CD	PWM0	TPU_TO0	I2C1_SCL_C	-	GP6_14	1.8/3.3V*2/16mA
	I	O	O	IO	-	IO(I)	Off
504	SDHI2	PWM1	I2C1	-	-		I(GPIO)
AF14	SD2_WP	PWM1_B	I2C1_SDA_C	-	-	GP6_15	1.8/3.3V*2/16mA
	I	O	IO	-	-	IO(I)	Off
505	SDHI2 Power	-	-	-	-		P
AD15	VCCQ_SD2	-	-	-	-	-	-
	P	-	-	-	-	-	-
506	SDHI3	MMC	-	-	-		I(GPIO)/Z(DBG)*1
AL13	SD3_CLK	MMC_CLK	-	-	-	GP6_16	1.8/3.3V*2/16mA
	O	O	-	-	-	IO(I)	Off/-*1
507	SDHI3	MMC	-	-	-		I(GPIO)/I(DBG)*1
AH13	SD3_CMD	MMC_CMD	-	-	-	GP6_17	1.8/3.3V*2/16mA
	IO	IO	-	-	-	IO(I)	Off/-*1
508	SDHI3	MMC	-	-	-		I(GPIO)/I(DBG)*1
AG13	SD3_DATA0	MMC_D0	-	-	-	GP6_18	1.8/3.3V*2/16mA
	IO	IO	-	-	-	IO(I)	Off/-*1
509	SDHI3	MMC	-	-	-		I(GPIO)/I(DBG)*1
AF13	SD3_DATA1	MMC_D1	-	-	-	GP6_19	1.8/3.3V*2/16mA
	IO	IO	-	-	-	IO(I)	Off/-*1
510	SDHI3	MMC	-	-	-		I(GPIO)/I(DBG)*1
AE14	SD3_DATA2	MMC_D2	-	-	-	GP6_20	1.8/3.3V**/16mA
	IO	IO	-	-	-	IO(I)	Off/-*1
511	SDHI3	MMC	-	-	-		I(GPIO)/I(DBG)*1
AE13	SD3_DATA3	MMC_D3	-	-	-	GP6_21	1.8/3.3V*2/16mA
	IO	IO	-	-	-	IO(I)	Off/-*1
512	SDHI3	MMC	IIC1(I2C8)	SCIF5	SCIFA5		I(GPIO)
AK13	SD3_CD	MMC_D4	IIC1_SCL_C	TX5_B	SCIFA5_TXD_C	GP6_22	1.8/3.3V*2/16mA
	I	IO	IO	O	O	IO(I)	Off
513	SDHI3	MMC	IIC1(I2C8)	SCIF5	SCIFA5		I(GPIO)
AJ13	SD3_WP	MMC_D5	IIC1_SDA_C	RX5_B	SCIFA5_RXD_C	GP6_23	1.8/3.3V*2/16mA
	I	IO	IO	I	I	IO(I)	Off
514	SDHI3 Power	-	-	-	-		P
AD13	VCCQ_SD3	-	-	-	-	-	-
	P	-	-	-	-	-	-

Notes: 1. (No.497 to 502 and 506 to 511): Debugging function is multiplexed. For details, refer to section 62, CoreSight. The default pin state after power-on reset depends on MD[21:20], MD[12:10] and MDT[1:0] pins setting. For details of mode pin settings, refer to section 3.3, Mode Pin Settings. Default pull-up state of No.497 to 502 and No.506 to 511 are "-" only in debugging operation.

2. (No.497 to 504 and 506 to 513) V/|IOH|: Pin voltage is selectable (3.3V: default). For details, refer to IOCTRL6 register in section 5, Pin Function Controller (PFC).

MSIOF, SCIF, VIN, MMC, I2C, IIC, RCAN, DU, ADG, PWM, SCIFA, HSCIF, SCIFB, TMU and GPIO (No.515 to 533): Up to 8-Function Multiplexed and Mode Pins assigned (No.521, 522)

These pins are set for GPIO except for No.527 to 530 (I2C5 and IIC3 pins) after power-on reset. For details, refer to GPSR4, GPSR6 and GPSR7 registers in section 5, Pin Function Controller (PFC).

	Function								
	1	2	3	4	5	6	7	GPIO	
No.	Module								During POR
Pin No.	Pin Name								V/|IOH|
Mode Pin	I/O								Pull-up
515	MSIOF0	SCIF2	Reserved	Reserved	VIN1	VIN1	-		I(GPIO)
T31	MSIOF0_SCK	RX2_C	-	-	VI1_CLK_C	VI1_G0_B	-	GP6_24	3.3V/8mA
	IO	I	-	-	I	I	-	IO(I)	On
516	MSIOF0	SCIF2	Reserved	Reserved	VIN1	VIN1	-		I(GPIO)
T30	MSIOF0_SYNC	TX2_C	-	-	VI1_CLKENB_C	VI1_G1_B	-	GP6_25	3.3V/4mA
	IO	O	-	-	I	I	-	IO(I)	On
517	MSIOF0	Reserved	Reserved	VIN1	VIN1	-	-		I(GPIO)
T29	MSIOF0_TXD	-	-	VI1_FIELD_C	VI1_G2_B	-	-	GP6_26	3.3V/4mA
	O	-	-	I	I	-	-	IO(I)	On
518	MSIOF0	Reserved	Reserved	VIN1	VIN1	-	-		I(GPIO)
T28	MSIOF0_RXD	-	-	VI1_DATA0_C	VI1_G3_B	-	-	GP6_27	3.3V/4mA
	I	-	-	I	I	-	-	IO(I)	On
519	MSIOF0	MMC	Reserved	SCIF0	VIN1	I2C7(IIC0)	VIN1		I(GPIO)
T27	MSIOF0_SS1	MMC_D6	-	TX0_E	VI1_HSYNC#_C	IIC0_SCL_C	VI1_G4_B	GP6_28	3.3V/8mA
	O	IO	-	O	I	IO	I	IO(I)	On
520	MSIOF0	MMC	Reserved	SCIF0	VIN1	I2C7(IIC0)	VIN1		I(GPIO)
T26	MSIOF0_SS2	MMC_D7	-	RX0_E	VI1_VSYNC#_C	IIC0_SDA_C	VI1_G5_B	GP6_29	3.3V/8mA
	O	IO	-	I	I	IO	I	IO(I)	On
521	Reserved	Reserved	RCAN1	-	-	-	-		I(Mode Pin)
R26	-	-	CAN1_TX_D	-	-	-	-	GP4_29	3.3V/4mA
MDT1	-	-	O	-	-	-	-	IO(I)	Off
522	Reserved	Reserved	RCAN	-	-	-	-		I(Mode Pin)
R28	-	-	CAN_CLK_C	-	-	-	-	GP4_30	3.3V/4mA
MDT0	-	-	I	-	-	-	-	IO(I)	Off
523	Reserved	Reserved	RCAN1	-	-	-	-		I(GPIO)
R27	-	-	CAN1_RX_D	-	-	-	-	GP4_31	3.3V/4mA
	-	-	I	-	-	-	-	IO(I)	On
524	Reserved	DU1	ADG	PWM5	SCIFA3	-	-		I(GPIO)
R31	-	DU1_DOTCLKIN_C	AUDIO_CLKB_B	PWM5_B	SCIFA3_TXD_C	-	-	GP7_20	3.3V/4mA
	-	I	I	O	O	-	-	IO(I)	On
525	Reserved	SCIF4	SCIFA4	PWM5	VIN1	SCIFA3	-		I(GPIO)
R30	-	TX4_C	SCIFA4_TXD_C	PWM5	VI1_G6_B	SCIFA3_RXD_C	-	GP7_21	3.3V/4mA
	-	O	O	O	I	I	-	IO(I)	On
526	Reserved	SCIF4	SCIFA4	PWM6	VIN1	SCIFA3	-		I(GPIO)
R29	-	RX4_C	SCIFA4_RXD_C	PWM6	VI1_G7_B	SCIFA3_SCK_C	-	GP7_22	3.3V/4mA
	-	I	I	O	I	O	-	IO(I)	On
527	I2C5_OD	-	-	-	-	-	-		Z
AJ18	I2C5_SCL	-	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	-	-	-	-	-	-	-	-
528	I2C5_OD	-	-	-	-	-	-		Z
AH18	I2C5_SDA	-	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	-	-	-	-	-	-	-	-
529	IIC3(I2C6 DVFS)	-	-	-	-	-	-		Z
AJ19	IIC3_SCL	-	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	-	-	-	-	-	-	-	-
530	IIC3(I2C6 DVFS)	-	-	-	-	-	-		Z
AH19	IIC3_SDA	-	-	-	-	-	-	-	1.8V/-
	IO(OD, Z)	-	-	-	-	-	-	-	-
531	HSCIF0	SCIFB0	Reserved	Reserved	TMU	VIN1	-		I(GPIO)
P28	HCTS0#	SCIFB0_CTS#	-	-	TCLK1	VI1_DATA1_C	-	GP7_0	3.3V/8mA
	IO	I	-	-	I	I	-	IO(I)	On
532	HSCIF0	SCIFB0	Reserved	Reserved	VIN1	-	-		I(GPIO)
R25	HRTS0#	SCIFB0_RTS#	-	-	VI1_DATA2_C	-	-	GP7_1	3.3V/8mA
	IO	O	-	-	I	-	-	IO(I)	On
533	HSCIF0	SCIFB0	Reserved	Reserved	RCAN	TMU	VIN1		I(GPIO)
P31	HSCK0	SCIFB0_SCK	-	-	CAN_CLK	TCLK2	VI1_DATA3_C	GP7_2	3.3V/8mA
	IO	O	-	-	I	I	I	IO(I)	On

HSCIF, SCIFB, VIN, RCAN and GPIO (No.534 to 540): Up to 7-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR7 register in section 5, Pin Function Controller (PFC).

	Function							
	1	2	3	4	5	6	GPIO	
No.	Module							During POR
Pin No.	Pin Name							V/|IOH|
	I/O							Pull-up
534	HSCIF0	SCIFB0	Reserved	Reserved	RCAN0	VIN1		I(GPIO)
P29	HRX0	SCIFB0_RXD	-	-	CAN0_RX_B	VI1_DATA4_C	GP7_3	3.3V/8mA
	I	I	-	-	I	I	IO(I)	On
535	HSCIF0	SCIFB0	Reserved	Reserved	RCAN0	VIN1		I(GPIO)
P30	HTX0	SCIFB0_TXD	-	-	CAN0_TX_B	VI1_DATA5_C	GP7_4	3.3V/8mA
	O	O	-	-	O	I	IO(I)	Off
536	HSCIF1	SCIFB1	VIN1	Reserved	VIN1	-		I(GPIO)
V25	HRX1	SCIFB1_RXD	VI1_R0_B	-	VI1_DATA6_C	-	GP7_5	3.3V/8mA
	I	I	I	-	I	-	IO(I)	Off
537	HSCIF1	SCIFB1	VIN1	Reserved	VIN1	-		I(GPIO)
V26	HTX1	SCIFB1_TXD	VI1_R1_B	-	VI1_DATA7_C	-	GP7_6	3.3V/8mA
	O	O	I	-	I	-	IO(I)	Off
538	HSCIF1	SCIFB1	Reserved	Reserved	-	-		I(GPIO)
U31	HSCK1	SCIFB1_SCK	-	-	-	-	GP7_7	3.3V/16mA
	IO	O	-	-	-	-	IO(I)	-
539	HSCIF1	SCIFB1	Reserved	RCAN1	-	-		I(GPIO)
U29	HCTS1#	SCIFB1_CTS#	-	CAN1_TX_B	-	-	GP7_8	3.3V/16mA
	IO	I	-	O	-	-	IO(I)	-
540	HSCIF1	SCIFB1	Reserved	RCAN1	-	-		I(GPIO)
U28	HRTS1#	SCIFB1_RTS#	-	CAN1_RX_B	-	-	GP7_9	3.3V/16mA
	IO	O	-	I	-	-	IO(I)	-

Thermal Sensor (No.541 to 562): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
541	Power	P
AK16	VSS	-
	P	-
542	Reserved	IO
U27	-	3.3V/16mA
	-	-
543	-	P
U26	VDD_MLBPLL	-
	P	-
544	-	P
U25	VSS_MLBPLL	-
	P	-
545	Reserved	Z
L31	-	1.8/3.3V/-
	-	-
546	Reserved	Z
K31	-	1.8/3.3V/-
	-	-
547	Reserved	Z
N31	-	1.8/3.3V/-
	-	-
548	Reserved	Z
M31	-	1.8/3.3V/-
	-	-
549	Reserved	Z
L29	-	1.8/3.3V/-
	-	-
550	Reserved	Z
L28	-	1.8/3.3V/-
	-	-
551	Reserved	Z
M29	-	1.8/3.3V/-
	-	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V/|IOH|
	I/O	Pull-up
552	Reserved	Z
M28	-	1.8/3.3V/-
	-	-
553	-	P
N25	VDD_MLBPPLL0	-
	P	-
554	-	P
P25	VSS_MLBPPLL0	-
	P	-
555	-	P
N26	VDD_MLBPPLL1	-
	P	-
556	-	P
P26	VSS_MLBPPLL1	-
	P	-
557	-	P
K28	VCCQ18_MLBP	-
	P	-
558	-	P
N28	VCCQ18_MLBP	-
	P	-
559	-	P
K29	VCCQ33_MLBP	-
	P	-
560	-	P
N29	VCCQ33_MLBP	-
	P	-
561	Thermal Sensor	O
P27	VTHSENSE0	1.8V/-
	O(analog)	-
562	Thermal Sensor	O
N27	VTHREF0	1.8V/-
	O(analog)	-

- End of Table 4.1 -

4.2 Pin States

Table 4.2 is pin state of the RZ/G1M.

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Pin Name: Pin name of function 1 in pin in Table 4.1, I/O: Input or output direction considered about all multiplexed pin functions of the pin.

During POR: Pin state during power-on reset (PRESET# pin input is low-level).

Default Pin Function: Pin function after power-on reset

Default State: Pin state of default pin function

Default pull-up: Internal pull-up control function is available or not from a power-on reset and its pull-up state.

"On": Pull-up control function is available and default state is pulled-up.

(No.212, ACK pin is available internal pull-down function.)

"Off": Pull-up control function is available and default state is not pulled-up.

"-": Pull-up control function is not available.

For details of pull-up control function, refer to PUPR0 through PUPR7 registers in section 5, Pin Function Controller (PFC).

I: Input, IO: Input and output, O: Output, H: High level output, L: Low level output, X: Undefined value output, Z: High impedance, P: Power supply pin.

Notes:
1. All power supply pins and ground pins include VCCQ, VCCQ18, VDD, VDD_DVFS, VDDQ_M0, VDDQ_M1, VDDQ_M1A, and VSS pins which does not describe in Table 4.2 must be used.
2. All mode pins (MD[14:0], [24:19], [28:27], and MDT[1:0]) must be used during power-on reset. For details of mode pin settings, refer to section 3.3, Mode Pin Settings.
3. Boot module related pins (LBSC area 0 or QSPI) should be used during boot operation. For details of QSPI boot, refer to section 18, Booting.
4. For multiplexed pins and modules of each pin, refer to Table 4.1.

Table 4.2 Pin States

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
1	F20	M0CKE0	O	X	M0CKE0	L	-
2	C19	M0CKE1	O	X	M0CKE1	L	-
3	G16	VSS	-	P	VSS	P	-
4	H18	M0BKPRST#	I	I	M0BKPRST#	I	-
5	E19	M0RESET#	O	H	M0RESET#	H to L	-
6	G20	M0CK0	O	X	M0CK0	O	-
7	G19	M0CK0#	O	X	M0CK0#	O	-
8	G17	M0CK1	O	X	M0CK1	O	-
9	G18	M0CK1#	O	X	M0CK1#	O	-
10	B20	M0CS0#	O	H	M0CS0#	H	-
11	A19	M0CS1#	O	H	M0CS1#	H	-
12	D20	M0ODT0	O	L	M0ODT0	L	-
13	E18	M0ODT1	O	L	M0ODT1	L	-
14	H16	M0ZQ	IO	IO	M0ZQ	IO	-
15	E21	M0WE#	O	H	M0WE#	H	-
16	D22	M0RAS#	O	H	M0RAS#	H	-
17	C22	M0CAS#	O	H	M0CAS#	H	-
18	E17	M0A0	O	L	M0A0	L	-
19	B22	M0A1	O	L	M0A1	L	-
20	A22	M0A2	O	L	M0A2	L	-
21	D17	M0A3	O	L	M0A3	L	-
22	A21	M0A4	O	L	M0A4	L	-
23	D16	M0A5	O	L	M0A5	L	-
24	B17	M0A6	O	L	M0A6	L	-
25	B21	M0A7	O	L	M0A7	L	-
26	A16	M0A8	O	L	M0A8	L	-
27	B18	M0A9	O	L	M0A9	L	-
28	C18	M0A10	O	L	M0A10	L	-
29	A18	M0A11	O	L	M0A11	L	-
30	E16	M0A12	O	L	M0A12	L	-
31	A17	M0A13	O	L	M0A13	L	-
32	B16	M0A14	O	L	M0A14	L	-
33	D18	M0A15	O	L	M0A15	L	-
34	C21	M0BA0	O	L	M0BA0	L	-
35	C16	M0BA1	O	L	M0BA1	L	-
36	D21	M0BA2	O	L	M0BA2	L	-
37	G21	VDDQ_M0APLL	-	P	VDDQ_M0APLL	P	-
38	H21	VSSQ_M0APLL	-	P	VSSQ_M0APLL	P	-
39	A27	M0DQ0	IO	Z	M0DQ0	Z	-
40	C28	M0DQ1	IO	Z	M0DQ1	Z	-
41	D27	M0DQ2	IO	Z	M0DQ2	Z	-
42	A29	M0DQ3	IO	Z	M0DQ3	Z	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
43	B27	M0DQ4	IO	Z	M0DQ4	Z	-
44	B29	M0DQ5	IO	Z	M0DQ5	Z	-
45	C27	M0DQ6	IO	Z	M0DQ6	Z	-
46	A30	M0DQ7	IO	Z	M0DQ7	Z	-
47	E26	M0DQS0	IO	Z	M0DQS0	Z	-
48	E25	M0DQS0#	IO	Z	M0DQS0#	Z	-
49	A28	M0DM0	O	Z	M0DM0	Z	-
50	G22	VDDQ_M0DPLL0	-	P	VDDQ_M0DPLL0	P	-
51	G23	VSSQ_M0DPLL0	-	P	VSSQ_M0DPLL0	P	-
52	G24	M0VREFDQ0	-	P	M0VREFDQ0	P	-
53	B23	M0DQ8	IO	Z	M0DQ8	Z	-
54	A24	M0DQ9	IO	Z	M0DQ9	Z	-
55	C24	M0DQ10	IO	Z	M0DQ10	Z	-
56	D24	M0DQ11	IO	Z	M0DQ11	Z	-
57	B26	M0DQ12	IO	Z	M0DQ12	Z	-
58	D26	M0DQ13	IO	Z	M0DQ13	Z	-
59	B24	M0DQ14	IO	Z	M0DQ14	Z	-
60	A25	M0DQ15	IO	Z	M0DQ15	Z	-
61	E23	M0DQS1	IO	Z	M0DQS1	Z	-
62	E24	M0DQS1#	IO	Z	M0DQS1#	Z	-
63	C25	M0DM1	O	Z	M0DM1	Z	-
64	F22	VDDQ_M0DPLL1	-	P	VDDQ_M0DPLL1	P	-
65	F23	VSSQ_M0DPLL1	-	P	VSSQ_M0DPLL1	P	-
66	E31	M0DQ16	IO	Z	M0DQ16	Z	-
67	C30	M0DQ17	IO	Z	M0DQ17	Z	-
68	E29	M0DQ18	IO	Z	M0DQ18	Z	-
69	B31	M0DQ19	IO	Z	M0DQ19	Z	-
70	E30	M0DQ20	IO	Z	M0DQ20	Z	-
71	C31	M0DQ21	IO	Z	M0DQ21	Z	-
72	E28	M0DQ22	IO	Z	M0DQ22	Z	-
73	D29	M0DQ23	IO	Z	M0DQ23	Z	-
74	F27	M0DQS2	IO	Z	M0DQS2	Z	-
75	G27	M0DQS2#	IO	Z	M0DQS2#	Z	-
76	D31	M0DM2	O	Z	M0DM2	Z	-
77	K25	VDDQ_M0DPLL2	-	P	VDDQ_M0DPLL2	P	-
78	J25	VSSQ_M0DPLL2	-	P	VSSQ_M0DPLL2	P	-
79	H25	M0VREFDQ1	-	P	M0VREFDQ1	P	-
80	F28	M0DQ24	IO	Z	M0DQ24	Z	-
81	G31	M0DQ25	IO	Z	M0DQ25	Z	-
82	F30	M0DQ26	IO	Z	M0DQ26	Z	-
83	H30	M0DQ27	IO	Z	M0DQ27	Z	-
84	H28	M0DQ28	IO	Z	M0DQ28	Z	-
85	J30	M0DQ29	IO	Z	M0DQ29	Z	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
86	H29	M0DQ30	IO	Z	M0DQ30	Z	-
87	H31	M0DQ31	IO	Z	M0DQ31	Z	-
88	J27	M0DQS3	IO	Z	M0DQS3	Z	-
89	H27	M0DQS3#	IO	Z	M0DQS3#	Z	-
90	G29	M0DM3	O	Z	M0DM3	Z	-
91	K26	VDDQ_M0DPLL3	-	P	VDDQ_M0DPLL3	P	-
92	J26	VSSQ_M0DPLL3	-	P	VSSQ_M0DPLL3	P	-
93	H19	VDDQ_M0BKUP	-	P	VDDQ_M0BKUP	P	-
94	F5	M1CKE0	O	X	M1CKE0/GP_DDR1*1	L/O	-
95	G3	M1CKE1	O	X	M1CKE1/GP_DDR2*1	L/O	-
96	H7	M1VREFCA	-	P	M1VREFCA	P	-
97	J7	M1BKPRST#	I	I	M1BKPRST#	I	-
98	G5	M1RESET#	O	H/X	M1RESET#/GP_DDR3*1	H to L/O	-
99	J5	M1CK0	O	X	M1CK0/Reserved*1	O/O	-
100	H5	M1CK0#	O	X	M1CK0#/Reserved*1	O/O	-
101	L5	M1CK1	O	X	M1CK1/Reserved*1	O/O	-
102	K5	M1CK1#	O	X	M1CK1#/Reserved*1	O/O	-
103	F2	M1CS0#	IO	H/I	M1CS0#/GP_DDR5*1	H/I	-
104	G1	M1CS1#	IO	H/I	M1CS1#/GP_DDR8*1	H/I	-
105	F4	M1ODT0	IO	L/I	M1ODT0/GP_DDR6*1	L/I	-
106	H4	M1ODT1	IO	L/I	M1ODT1/GP_DDR10*1	L/I	-
107	L8	M1ZQ	IO	IO	M1ZQ	IO	-
108	E3	M1WE#	O	H/Z	M1WE#/GP_DDR9*1	H/Z	-
109	D3	M1RAS#	O	H/Z	M1RAS#/GP_DDR12*1	H/Z	-
110	E4	M1CAS#	IO	H/I	M1CAS#/GP_DDR4*1	H/I	-
111	B1	M1A0	O	L/Z	M1A0/GP_DDR7*1	L/Z	-
112	H2	M1A1	IO	L/I	M1A1/GP_DDR13*1	L/I	-
113	E2	M1A2	O	L/Z	M1A2/GP_DDR15*1	L/Z	-
114	M3	M1A3	IO	L/I	M1A3/GP_DDR23*1	L/I	-
115	E1	M1A4	O	L/Z	M1A4/GP_DDR17*1	L/Z	-
116	D1	M1A5	O	L/Z	M1A5/GP_DDR11*1	L/Z	-
117	K2	M1A6	O	L/Z	M1A6/GP_DDR24*1	L/Z	-
118	H1	M1A7	IO	L/I	M1A7/GP_DDR14*1	L/I	-
119	M1	M1A8	IO	L/I	M1A8/GP_DDR25*1	L/I	-
120	J2	M1A9	O	L/Z	M1A9/GP_DDR26*1	L/Z	-
121	L3	M1A10	IO	L/I	M1A10/GP_DDR22*1	L/I	-
122	K1	M1A11	O	L/Z	M1A11/GP_DDR21*1	L/Z	-
123	C2	M1A12	O	L/Z	M1A12/GP_DDR16*1	L/Z	-
124	L1	M1A13	IO	L/I	M1A13/GP_DDR27*1	L/I	-
125	M2	M1A14	IO	L/I	M1A14/GP_DDR28*1	L/I	-
126	K3	M1A15	O	L/Z	M1A15/GP_DDR29*1	L/Z	-
127	J3	M1BA0	O	L/Z	M1BA0/GP_DDR20*1	L/Z	-
128	C1	M1BA1	O	L/Z	M1BA1/GP_DDR19*1	L/Z	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
129	H3	M1BA2	IO	L/I	M1BA2/GP_DDR18*[1]	L/I	-
130	L7	VDDQ_M1APLL	-	P	VDDQ_M1APLL	P	-
131	K7	VSSQ_M1APLL	-	P	VSSQ_M1APLL	P	-
132	L6	VDDQ_M1MPLL	-	P	VDDQ_M1MPLL	P	-
133	K6	VSSQ_M1MPLL	-	P	VSSQ_M1MPLL	P	-
134	B12	M1DQ0	IO	Z	M1DQ0/M0DQ32/Reserved*[2]	Z/Z/Z	-
135	B11	M1DQ1	IO	Z	M1DQ1/M0DQ33/Reserved*[2]	Z/Z/Z	-
136	D12	M1DQ2	IO	Z	M1DQ2/M0DQ34/Reserved*[2]	Z/Z/Z	-
137	A10	M1DQ3	IO	Z	M1DQ3/M0DQ35/Reserved*[2]	Z/Z/Z	-
138	C11	M1DQ4	IO	Z	M1DQ4/M0DQ36/Reserved*[2]	Z/Z/Z	-
139	D10	M1DQ5	IO	Z	M1DQ5/M0DQ37/Reserved*[2]	Z/Z/Z	-
140	C10	M1DQ6	IO	Z	M1DQ6/M0DQ38/Reserved*[2]	Z/Z/Z	-
141	D11	M1DQ7	IO	Z	M1DQ7/M0DQ39/Reserved*[2]	Z/Z/Z	-
142	E12	M1DQS0	IO	Z	M1DQS0/M0DQS4/Reserved*[2]	Z/Z/Z	-
143	E11	M1DQS0#	IO	Z	M1DQS0#/M0DQS4#/Reserved*[2]	Z/Z/Z	-
144	A11	M1DM0	O	Z	M1DM0/M0DM4/Reserved*[2]	Z/Z/Z	-
145	G13	VDDQ_M1DPLL0	-	P	VDDQ_M1DPLL0/VDDQ_M0DPLL4/VDDQ_M0DPLL4*[2]	P	-
146	G12	VSSQ_M1DPLL0	-	P	VSSQ_M1DPLL0/VSSQ_M0DPLL4/VSSQ_M0DPLL4*[2]	P	-
147	G14	M1VREFDQ0	-	P	M1VREFDQ0/M0VREFDQ2/M0VREFDQ2*[2]	P	-
148	A13	M1DQ8	IO	Z	M1DQ8/M0DQ40/Reserved*[2]	Z/Z/Z	-
149	A14	M1DQ9	IO	Z	M1DQ9/M0DQ41/Reserved*[2]	Z/Z/Z	-
150	D14	M1DQ10	IO	Z	M1DQ10/M0DQ42/Reserved*[2]	Z/Z/Z	-
151	B14	M1DQ11	IO	Z	M1DQ11/M0DQ43/Reserved*[2]	Z/Z/Z	-
152	C14	M1DQ12	IO	Z	M1DQ12/M0DQ44/Reserved*[2]	Z/Z/Z	-
153	B15	M1DQ13	IO	Z	M1DQ13/M0DQ45/Reserved*[2]	Z/Z/Z	-
154	D15	M1DQ14	IO	Z	M1DQ14/M0DQ46/Reserved*[2]	Z/Z/Z	-
155	A15	M1DQ15	IO	Z	M1DQ15/M0DQ47/Reserved*[2]	Z/Z/Z	-
156	E14	M1DQS1	IO	Z	M1DQS1/M0DQS5/Reserved*[2]	Z/Z/Z	-
157	E13	M1DQS1#	IO	Z	M1DQS1#/M0DQS5#/Reserved*[2]	Z/Z/Z	-
158	C13	M1DM1	O	Z	M1DM1/M0DM5/Reserved*[2]	Z/Z/Z	-
159	F13	VDDQ_M1DPLL1	-	P	VDDQ_M1DPLL1/VDDQ_M0DPLL5/VDDQ_M0DPLL5*[2]	P	-
160	F12	VSSQ_M1DPLL1	-	P	VSSQ_M1DPLL1/VSSQ_M0DPLL5/VSSQ_M0DPLL5*[2]	P	-
161	B6	M1DQ16	IO	Z	M1DQ16/M1DQ48/Reserved*[2]	Z/Z/Z	-
162	A7	M1DQ17	IO	Z	M1DQ17/M0DQ49/Reserved*[2]	Z/Z/Z	-
163	C8	M1DQ18	IO	Z	M1DQ18/M0DQ50/Reserved*[2]	Z/Z/Z	-
164	B8	M1DQ19	IO	Z	M1DQ19/M0DQ51/Reserved*[2]	Z/Z/Z	-
165	D8	M1DQ20	IO	Z	M1DQ20/M0DQ52/Reserved*[2]	Z/Z/Z	-
166	A8	M1DQ21	IO	Z	M1DQ21/M0DQ53/Reserved*[2]	Z/Z/Z	-
167	D6	M1DQ22	IO	Z	M1DQ22/M0DQ54/Reserved*[2]	Z/Z/Z	-
168	B9	M1DQ23	IO	Z	M1DQ23/M0DQ55/Reserved*[2]	Z/Z/Z	-
169	E8	M1DQS2	IO	Z	M1DQS2/M0DQS6/Reserved*[2]	Z/Z/Z	-
170	E9	M1DQS2#	IO	Z	M1DQS2#/M0DQS6#/Reserved*[2]	Z/Z/Z	-
171	C7	M1DM2	O	Z	M1DM2/M0DM6/Reserved*[2]	Z/Z/Z	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
172	F10	VDDQ_M1DPLL2	-	P	VDDQ_M1DPLL2/VDDQ_M0DPLL6/VDDQ_M0DPLL6*2	P	-
173	F9	VSSQ_M1DPLL2	-	P	VSSQ_M1DPLL2/VSSQ_M0DPLL6/VSSQ_M0DPLL6*2	P	-
174	G8	M1VREFDQ1	-	P	M1VREFDQ1/M0VREFDQ3/M0VREFDQ3*2	P	-
175	B3	M1DQ24	IO	Z	M1DQ24/M0DQ56/Reserved*2	Z/Z/Z	-
176	D5	M1DQ25	IO	Z	M1DQ25/M0DQ57/Reserved*2	Z/Z/Z	-
177	C4	M1DQ26	IO	Z	M1DQ26/M0DQ58/Reserved*2	Z/Z/Z	-
178	C5	M1DQ27	IO	Z	M1DQ27/M0DQ59/Reserved*2	Z/Z/Z	-
179	A5	M1DQ28	IO	Z	M1DQ28/M0DQ60/Reserved*2	Z/Z/Z	-
180	A3	M1DQ29	IO	Z	M1DQ29/M0DQ61/Reserved*2	Z/Z/Z	-
181	B5	M1DQ30	IO	Z	M1DQ30/M0DQ62/Reserved*2	Z/Z/Z	-
182	A2	M1DQ31	IO	Z	M1DQ31/M0DQ63/Reserved*2	Z/Z/Z	-
183	E7	M1DQS3	IO	Z	M1DQS3/M0DQS7/Reserved*2	Z/Z/Z	-
184	E6	M1DQS3#	IO	Z	M1DQS3#/M0DQS7#/Reserved*2	Z/Z/Z	-
185	A4	M1DM3	O	Z	M1DM3/M0DM7/Reserved*2	Z/Z/Z	-
186	G10	VDDQ_M1DPLL3	-	P	VDDQ_M1DPLL3/VDDQ_M0DPLL7/VDDQ_M0DPLL7*2	P	-
187	G9	VSSQ_M1DPLL3	-	P	VSSQ_M1DPLL3/VSSQ_M0DPLL7/VSSQ_M0DPLL7*2	P	-
188	G6	VDDQ_M1BKUP	-	P	VDDQ_M1BKUP	P	-
189	AL18	EXTAL	I	I	EXTAL	I	-
190	AL17	XTAL	O	O	XTAL	O	-
191	F16	VDD_CPGPLL1	-	P	VDD_CPGPLL1	P	-
192	F15	VSS_CPGPLL1	-	P	VSS_CPGPLL1	P	-
193	H15	VDD_CPGPLL2	-	P	VDD_CPGPLL2	P	-
194	G15	VSS_CPGPLL2	-	P	VSS_CPGPLL2	P	-
195	L25	VDD_CPGPLL0	-	P	VDD_CPGPLL0	P	-
196	M25	VSS_CPGPLL0	-	P	VSS_CPGPLL0	P	-
197	L26	VDD_CPGPLL3	-	P	VDD_CPGPLL3	P	-
198	M26	VSS_CPGPLL3	-	P	VSS_CPGPLL3	P	-
199	AE19	PRESET#	I	I(L)	PRESET#	I	-
200	U5	PRESETOUT#	O	L	PRESETOUT#	L to H	-
201	AG19	MPMD0	I	I(L)	MPMD0	I(L)	-
202	AG18	MPMD1	I	I(L)	MPMD1	I(L)	-
203	AF17	BSMODE	I	I	BSMODE	I	-
204	U6	AVS1	O	L	AVS1	H or L*3	Off
205	U7	AVS2	O	L	AVS2	H or L*3	Off
206	AD19	VCCQ_ISO	-	P	VCCQ_ISO	P	-
207	AF19	TRST#	I	I(L)	TRST#	I	On
208	AE18	TCK	I	I	TCK	I	On
209	AF18	TMS	I	I	TMS	I	On
210	AH17	TDI	I	I	TDI	I	On
211	AJ17	TDO	O	Z	TDO	Z	-
212	AE17	ACK	IO	I	[ACK]	I	On (pull-down)
213	AL23	RIDP1_SATA	I	I	RIDP1_SATA/RIDP1_PCIe*4	I/I	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
214	AL24	RIDN1_SATA	I	I	RIDN1_SATA/RIDN1_PCIe*4	I/I	-
215	AL25	TODP1_SATA	O	O	TODP1_SATA/TODP1_PCIe*4	O/O	-
216	AL26	TODN1_SATA	O	O	TODN1_SATA/TODN1_PCIe*4	O/O	-
217	AJ26	CICREFP1_SATA	I	I	CICREFP1_SATA/CICREFP1_PCIe*4	I/I	-
218	AJ25	CICREFN1_SATA	I	I	CICREFN1_SATA/CICREFN1_PCIe*4	I/I	-
219	AE23	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*4	P	-
220	AF24	VDDA_SATA1	-	P	VDDA_SATA1/VDDA_PCIe*4	P	-
221	AG24	VDDA_SATA1	-	P	VDDA_SATA1/VDDA_PCIe*4	P	-
222	AF23	VDDD_SATA1	-	P	VDDD_SATA1/VDDD_PCIe*4	P	-
223	AG23	VDDD_SATA1	-	P	VDDD_SATA1/VDDD_PCIe*4	P	-
224	AH24	VDDD_SATA1	-	P	VDDD_SATA1/VDDD_PCIe*4	P	-
225	AD23	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*4	P	-
226	AE24	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*4	P	-
227	AJ24	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*4	P	-
228	AK24	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*4	P	-
229	AK25	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*4	P	-
230	AK26	VSS_SATA1	-	P	VSS_SATA1/VSS_PCIe*4	P	-
231	AK23	VSS_SATA1	-	P	VSS_SATA1/ VSS_PCIe*4	P	-
232	AL27	RIDP0_SATA	I	I	RIDP0_SATA/RIDP0_USB3*4	I/I	-
233	AL28	RIDN0_SATA	I	I	RIDN0_SATA/RIDN0_USB3*4	I/I	-
234	AL29	TODP0_SATA	O	O	TODP0_SATA/TODP0_USB3*4	O/O	-
235	AL30	TODN0_SATA	O	O	TODN0_SATA/TODN0_USB3*4	O/O	-
236	AJ28	CICREFP0_SATA	I	I	CICREFP0_SATA/CICREFP0_USB3*4	I/I	-
237	AJ27	CICREFN0_SATA	I	I	CICREFN0_SATA/CICREFN0_USB3*4	I/I	-
238	AF25	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
239	AG26	VDDA_SATA0	-	P	VDDA_SATA0/VDDA_USB3*4	P	-
240	AH27	VDDA_SATA0	-	P	VDDA_SATA0/VDDA_USB3*4	P	-
241	AH25	VDDD_SATA0	-	P	VDDD_SATA0/VDDD_USB3*4	P	-
242	AH26	VDDD_SATA0	-	P	VDDD_SATA0/VDDD_USB3*4	P	-
243	AG25	VDDD_SATA0	-	P	VDDD_SATA0/VDDD_USB3*4	P	-
244	AD24	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
245	AE25	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
246	AF26	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
247	AG27	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
248	AK27	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
249	AH28	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
250	AK28	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
251	AJ29	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
252	AK29	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
253	AK30	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
254	AL31	VSS_SATA0	-	P	VSS_SATA0/VSS_USB3*4	P	-
255	AL20	USB_EXTAL	I	I	USB_EXTAL	I	-
256	AL19	USB_XTAL	O	O	USB_XTAL	O	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
257	AG31	USB0_DP	IO	I	USB0_DP	I	-
258	AH31	USB0_DM	IO	I	USB0_DM	I	-
259	AG29	USB0_RREF	-	I	USB0_RREF	P	-
260	AE27	VD331	-	P	VD331	P	-
261	AD26	VD181	-	P	VD181	P	-
262	AB24	AVDD	-	P	AVDD	P	-
263	AC24	AVSS	-	P	AVSS	P	-
264	AF31	USB0_PWEN	O	L	USB0_PWEN	L	Off
265	AF30	USB0_OVC/VBUS	I	I	[USB0_OVC/VBUS]	I	On
266	AJ31	USB1_DP	IO	I	USB1_DP	I	-
267	AK31	USB1_DM	IO	I	USB1_DM	I	-
268	AH29	USB1_RREF	-	I	USB1_RREF	P	-
269	AF28	VD331	-	P	VD331	P	-
270	AC25	AVDD	-	P	AVDD	P	-
271	AD25	AVSS	-	P	AVSS	P	-
272	AE26	AVSS	-	P	AVSS	P	-
273	AF27	AVSS	-	P	AVSS	P	-
274	AG28	AVSS	-	P	AVSS	P	-
275	AE28	USB1_PWEN	O	L	USB1_PWEN	L	Off
276	AD27	USB1_OVC	I	I	USB1_OVC	I	On
277	AE20	DU0_LVDS_CLK_P	O	Z	DU0_LVDS_CLK_P	Z	-
278	AF20	DU0_LVDS_CLK_N	O	Z	DU0_LVDS_CLK_N	Z	-
279	AJ23	DU0_LVDS_CH0_P	O	Z	DU0_LVDS_CH0_P	Z	-
280	AJ22	DU0_LVDS_CH0_N	O	Z	DU0_LVDS_CH0_N	Z	-
281	AL21	DU0_LVDS_CH1_P	O	Z	DU0_LVDS_CH1_P	Z	-
282	AL22	DU0_LVDS_CH1_N	O	Z	DU0_LVDS_CH1_N	Z	-
283	AJ20	DU0_LVDS_CH2_P	O	Z	DU0_LVDS_CH2_P	Z	-
284	AJ21	DU0_LVDS_CH2_N	O	Z	DU0_LVDS_CH2_N	Z	-
285	AG22	DU0_LVDS_CH3_P	O	Z	DU0_LVDS_CH3_P	Z	-
286	AG21	DU0_LVDS_CH3_N	O	Z	DU0_LVDS_CH3_N	Z	-
287	AG17	DU0_DOTCLKIN	IO	I	GP6_31	I	On
288	AD22	VDDQ_LVDS	-	P	VDDQ_LVDS	P	-
289	AE22	VDDQ_LVDS	-	P	VDDQ_LVDS	P	-
290	AF22	VDDQ_LVDS	-	P	VDDQ_LVDS	P	-
291	AD20	DU0_LVDS_PLL1_VCC	-	P	DU0_LVDS_PLL1_VCC	P	-
292	AD21	DU0_LVDS_PLL1_VSS	-	P	DU0_LVDS_PLL1_VSS	P	-
293	AA7	D0	IO	I	D0/GP0_0*[5]	I/I	On
294	AA6	D1	IO	I	D1/GP0_1*[5]	I/I	On
295	AA5	D2	IO	I	D2/GP0_2*[5]	I/I	On
296	AA4	D3	IO	I	D3/GP0_3*[5]	I/I	On
297	AA3	D4	IO	I	D4/GP0_4*[5]	I/I	On
298	AA2	D5	IO	I	D5/GP0_5*[5]	I/I	On
299	AA1	D6	IO	I	D6/GP0_6*[5]	I/I	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
300	Y7	D7	IO	I	D7/GP0_7*5	I/I	On
301	Y6	D8	IO	I	D8/GP0_8*5	I/I	On
302	Y5	D9	IO	I	D9/GP0_9*5	I/I	On
303	Y4	D10	IO	I	D10/GP0_10*5	I/I	On
304	Y3	D11	IO	I	D11/GP0_11*5	I/I	On
305	Y2	D12	IO	I	D12/GP0_12*5	I/I	On
306	Y1	D13	IO	I	D13/GP0_13*5	I/I	On
307	W2	D14	IO	I	D14/GP0_14*5	I/I	On
308	W1	D15	IO	I	D15/GP0_15*5	I/I	On
309	T7	A0	IO	I	A0/GP0_16*5	L/I	On
310	W7	A1	IO	I(MD28)	A1/GP0_17*5	L/I	Off
311	W6	A2	IO	I(MD23)	A2/GP0_18*5	L/I	Off
312	W5	A3	IO	I(MD13)	A3/GP0_19*5	L/I	Off
313	W4	A4	IO	I(MD24)	A4/GP0_20*5	L/I	Off
314	W3	A5	IO	I	A5/GP0_21*5	L/I	On
315	T6	A6	IO	I	A6/GP0_22*5	L/I	On
316	V7	A7	IO	I(MD27)	A7/GP0_23*5	L/I	Off
317	T5	A8	IO	I	A8/GP0_24*5	L/I	On
318	T4	A9	IO	I	A9/GP0_25*5	L/I	On
319	V6	A10	IO	I(MD22)	A10/GP0_26*5	L/I	Off
320	T3	A11	IO	I	A11/GP0_27*5	L/I	On
321	T2	A12	IO	I	A12/GP0_28*5	L/I	On
322	R7	A13	IO	I(MD21)	A13/GP0_29*5	L/I	Off
323	R6	A14	IO	I(MD19)	A14/GP0_30*5	L/I	Off
324	R5	A15	IO	I(MD20)	A15/GP0_31*5	L/I	Off
325	R4	A16	IO	I	A16/GP1_0*5	L/I	On
326	R3	A17	IO	I	A17/GP1_1*5	L/I	On
327	R2	A18	IO	I	A18/GP1_2*5	L/I	On
328	P7	A19	IO	I(MD14)	A19/GP1_3*5	L/I	Off
329	P6	A20	IO	I	A20/GP1_4*5	L/I	On
330	P5	A21	IO	I	A21/GP1_5*5	L/I	On
331	P4	A22	IO	I	A22/GP1_6*5	L/I	On
332	P3	A23	IO	I	A23/GP1_7*5	L/I	On
333	P2	A24	IO	I	A24/GP1_8*5	L/I	On
334	P1	A25	IO	I	A25/GP1_9*5	L/I	On
335	U1	CLKOUT	O	O	CLKOUT	O	-
336	T1	CS0#	IO	I	CS0#/GP1_10*5	H/I	On
337	R1	CS1#/A26	IO	I	[CS1#/A26]/GP1_11*5	[H or L] *6/I	On
338	V1	EX_CS0#	IO	I	GP1_12	I	Off
339	N1	EX_CS1#	IO	I	GP1_13	I	On
340	N2	EX_CS2#	IO	I	GP1_14	I	On
341	V3	EX_CS3#	IO	I(MD9)	GP1_15	I	Off

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
342	V4	EX_CS4#	IO	I	GP1_16	I	On
343	V5	EX_CS5#	IO	I(MD8)	GP1_17	I	Off
344	N3	BS#	IO	I(MD10)	BS#/GP1_18*5	H/I	Off
345	V2	RD#	IO	I(MD12)	RD#/GP1_19*5	H/I	Off
346	N4	RD/WR#	IO	I	GP1_20	I	On
347	N5	WE0#	IO	I(MD6)	WE0#/GP1_21*5	H/I	Off
348	N6	WE1#	IO	I(MD4)	WE1#/GP1_22*5	H/I	Off
349	U3	EX_WAIT0	IO	I	EX_WAIT0/GP1_23*5	I/I	On
350	U4	DREQ0	IO	I	GP1_24	I	On
351	N7	DACK0	IO	I(MD7)	GP1_25	I	Off
352	T25	SPEEDIN	IO	I	GP5_31	I	On
353	V31	SSI_SCK0129	IO	I	GP2_0	I	On
354	V30	SSI_WS0129	IO	I	GP2_1	I	On
355	V29	SSI_SDATA0	IO	I	GP2_2	I	On
356	W31	SSI_SCK1	IO	I	GP2_3	I	On
357	V28	SSI_WS1	IO	I	GP2_4	I	On
358	V27	SSI_SDATA1	IO	I	GP2_5	I	On
359	W30	SSI_SCK2	IO	I	GP2_6	I	On
360	W29	SSI_WS2	IO	I	GP2_7	I	On
361	W28	SSI_SDATA2	IO	I	GP2_8	I	On
362	W27	SSI_SCK34	IO	I	GP2_9	I	On
363	W26	SSI_WS34	IO	I	GP2_10	I	On
364	W25	SSI_SDATA3	IO	I	GP2_11	I	On
365	Y31	SSI_SCK4	IO	I	GP2_12	I	Off
366	Y30	SSI_WS4	IO	I	GP2_13	I	Off
367	Y29	SSI_SDATA4	IO	I	GP2_14	I	On
368	Y28	SSI_SCK5	IO	I	GP2_15	I	On
369	Y27	SSI_WS5	IO	I	GP2_16	I	On
370	Y26	SSI_SDATA5	IO	I	GP2_17	I	On
371	AA31	SSI_SCK6	IO	I	GP2_18	I	On
372	AA30	SSI_WS6	IO	I	GP2_19	I	Off
373	AA29	SSI_SDATA6	IO	I	GP2_20	I	Off
374	AA27	SSI_SCK78	IO	I	GP2_21	I	Off
375	AA26	SSI_WS78	IO	I	GP2_22	I	Off
376	Y25	SSI_SDATA7	IO	I	GP2_23	I	On
377	AA25	SSI_SDATA8	IO	I	GP2_24	I	On
378	AB31	SSI_SCK9	IO	I	GP2_25	I	Off
379	AB30	SSI_WS9	IO	I	GP2_26	I	Off
380	AB29	SSI_SDATA9	IO	I	GP2_27	I	On
381	AD31	AUDIO_CLKA	IO	I	GP2_28	I	On
382	AC30	AUDIO_CLKB	IO	I	GP2_29	I	On
383	AD30	AUDIO_CLKC	IO	I	GP2_30	I	On
384	AE31	AUDIO_CLKOUT	IO	I(MD5)	GP2_31	I	Off

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
385	AL16	NMI	I	I	NMI	I	-
386	AE30	IRQ0	IO	I	GP7_10	I	On
387	AE29	IRQ1	IO	I	GP7_11	I	On
388	AD29	IRQ2	IO	I	GP7_12	I	On
389	AD28	IRQ3	IO	I	GP7_13	I	On
390	AC29	IRQ4	IO	I	GP7_14	I	On
391	AC28	IRQ5	IO	I	GP7_15	I	On
392	AC27	IRQ6	IO	I	GP7_16	I	On
393	AB26	IRQ7	IO	I	GP7_17	I	On
394	AB27	IRQ8	IO	I	GP7_18	I	On
395	AB28	IRQ9	IO	I	GP7_19	I	On
396	AL12	DU1_DR0	IO	I	GP3_0	I	On
397	AK12	DU1_DR1	IO	I	GP3_1	I	On
398	AJ12	DU1_DR2	IO	I	GP3_2	I	On
399	AH12	DU1_DR3	IO	I	GP3_3	I	On
400	AG12	DU1_DR4	IO	I	GP3_4	I	On
401	AF12	DU1_DR5	IO	I	GP3_5	I	On
402	AE12	DU1_DR6	IO	I	GP3_6	I	On
403	AE11	DU1_DR7	IO	I	GP3_7	I	On
404	AL11	DU1_DG0	IO	I	GP3_8	I	On
405	AK11	DU1_DG1	IO	I	GP3_9	I	On
406	AJ11	DU1_DG2	IO	I	GP3_10	I	On
407	AH11	DU1_DG3	IO	I	GP3_11	I	On
408	AG11	DU1_DG4	IO	I	GP3_12	I	On
409	AF11	DU1_DG5	IO	I	GP3_13	I	On
410	AF10	DU1_DG6	IO	I	GP3_14	I	On
411	AE10	DU1_DG7	IO	I	GP3_15	I	On
412	AJ9	DU1_DB0	IO	I	GP3_16	I	On
413	AH9	DU1_DB1	IO	I	GP3_17	I	On
414	AG9	DU1_DB2	IO	I	GP3_18	I	On
415	AF9	DU1_DB3	IO	I	GP3_19	I	On
416	AE9	DU1_DB4	IO	I	GP3_20	I	On
417	AJ10	DU1_DB5	IO	I(MD11)	GP3_21	I	Off
418	AH10	DU1_DB6	IO	I	GP3_22	I	On
419	AG10	DU1_DB7	IO	I	GP3_23	I	On
420	AL9	DU1_DOTCLKIN	IO	I	GP3_24	I	On
421	AL10	DU1_DOTCLKOUT0	IO	I	GP3_25	I	On
422	AK10	DU1_DOTCLKOUT1	IO	I	GP3_26	I	On
423	AE8	DU1_EXHSYNC/DU1_HSYNC	IO	I(MD3)	GP3_27	I	Off
424	AF8	DU1_EXVSYNC/DU1_VSYNC	IO	I(MD2)	GP3_28	I	Off
425	AG8	DU1_EXODDF/DU1_ODDF/DISP/CDE	IO	I	GP3_29	I	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
426	AH8	DU1_DISP	IO	I(MD1)	GP3_30	I	Off
427	AJ8	DU1_CDE	IO	I(MD0)	GP3_31	I	Off
428	AC1	VI0_CLK	IO	I	GP4_0	I	On
429	AB1	VI0_CLKENB	IO	I	GP4_1	I	On
430	AC2	VI0_FIELD	IO	I	GP4_2	I	On
431	AB2	VI0_HSYNC#	IO	I	GP4_3	I	On
432	AB3	VI0_VSYNC#	IO	I	GP4_4	I	On
433	AB4	VI0_DATA0/VI0_B0	IO	I	GP4_5	I	On
434	AB5	VI0_DATA1/VI0_B1	IO	I	GP4_6	I	On
435	AB6	VI0_DATA2/VI0_B2	IO	I	GP4_7	I	On
436	AC3	VI0_DATA3/VI0_B3	IO	I	GP4_8	I	On
437	AB7	VI0_DATA4/VI0_B4	IO	I	GP4_9	I	On
438	AC4	VI0_DATA5/VI0_B5	IO	I	GP4_10	I	On
439	AC6	VI0_DATA6/VI0_B6	IO	I	GP4_11	I	On
440	AC7	VI0_DATA7/VI0_B7	IO	I	GP4_12	I	On
441	AD1	VI0_G0	IO	I	GP4_13	I	On
442	AD2	VI0_G1	IO	I	GP4_14	I	On
443	AD3	VI0_G2	IO	I	GP4_15	I	On
444	AD4	VI0_G3	IO	I	GP4_16	I	On
445	AD5	VI0_G4	IO	I	GP4_17	I	On
446	AD6	VI0_G5	IO	I	GP4_18	I	On
447	AE6	VI0_G6	IO	I	GP4_19	I	On
448	AD7	VI0_G7	IO	I	GP4_20	I	On
449	AE1	VI0_R0	IO	I	GP4_21	I	On
450	AE3	VI0_R1	IO	I	GP4_22	I	On
451	AE4	VI0_R2	IO	I	GP4_23	I	On
452	AE5	VI0_R3	IO	I	GP4_24	I	On
453	AF3	VI0_R4	IO	I	GP4_25	I	Off
454	AF4	VI0_R5	IO	I	GP4_26	I	Off
455	AF5	VI0_R6	IO	I	GP4_27	I	Off
456	AG4	VI0_R7	IO	I	GP4_28	I	Off
457	AF1	VI1_HSYNC#	IO	I	GP5_0	I	On
458	AF2	VI1_VSYNC#	IO	I	GP5_1	I	On
459	AG3	VI1_CLKENB	IO	I	GP5_2	I	On
460	AH2	VI1_FIELD	IO	I	GP5_3	I	On
461	AG1	VI1_CLK	IO	I	GP5_4	I	On
462	AH3	VI1_DATA0	IO	I	GP5_5	I	On
463	AH1	VI1_DATA1	IO	I	GP5_6	I	On
464	AJ1	VI1_DATA2	IO	I	GP5_7	I	On
465	AJ2	VI1_DATA3	IO	I	GP5_8	I	On
466	AK1	VI1_DATA4	IO	I	GP5_9	I	On
467	AL2	VI1_DATA5	IO	I	GP5_10	I	On
468	AK3	VI1_DATA6	IO	I	GP5_11	I	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
469	AJ4	VI1_DATA7	IO	I	GP5_12	I	On
470	AL3	ETH_MDIO	IO	I	GP5_13	I	On
471	AK4	ETH_CRS_DV	IO	I	GP5_14	I	On
472	AL4	ETH_RX_ER	IO	I	GP5_15	I	On
473	AH5	ETH_RXD0	IO	I	GP5_16	I	On
474	AL5	ETH_RXD1	IO	I	GP5_17	I	On
475	AH6	ETH_LINK	IO	I	GP5_18	I	On
476	AL6	ETH_REFCLK	IO	I	GP5_19	I	On
477	AJ5	ETH_TXD1	IO	I	GP5_20	I	On
478	AG6	ETH_TX_EN	IO	I	GP5_21	I	On
479	AJ6	ETH_MAGIC	IO	I	GP5_22	I	On
480	AG7	ETH_TXD0	IO	I	GP5_23	I	On
481	AF7	ETH_MDC	IO	I	GP5_24	I	On
482	AK8	STP_IVCXO27_0	IO	I	GP5_25	I	On
483	AL8	STP_ISCLK_0	IO	I	GP5_26	I	On
484	AH7	STP_ISD_0	IO	I	GP5_27	I	On
485	AJ7	STP_ISEN_0	IO	I	GP5_28	I	On
486	AK7	STP_ISSYNC_0	IO	I	GP5_29	I	On
487	AL7	STP_OPWM_0	IO	I	GP5_30	I	On
488	AL15	SD0_CLK	IO	I	GP6_0	I	Off
489	AH16	SD0_CMD	IO	I	GP6_1	I	Off
490	AG16	SD0_DATA0	IO	I	GP6_2	I	Off
491	AF16	SD0_DATA1	IO	I	GP6_3	I	Off
492	AE16	SD0_DATA2	IO	I	GP6_4	I	Off
493	AH15	SD0_DATA3	IO	I	GP6_5	I	Off
494	AJ15	SD0_CD	IO	I	GP6_6	I	Off
495	AJ16	SD0_WP	IO	I	GP6_7	I	Off
496	AD16	VCCQ_SD0	-	-	VCCQ_SD0	-	-
497	AL14	SD2_CLK	IO	I/Z*7	GP6_8/TDO2*[8]	I/Z*[7]	Off/-*[9]
498	AH14	SD2_CMD	IO	I	GP6_9/TRST2#*[8]	I/I	Off/-*[9]
499	AG15	SD2_DATA0	IO	I	GP6_10/TCK2*[8]	I/I	Off/-*[9]
500	AF15	SD2_DATA1	IO	I	GP6_11/TMS2*[8]	I/I	Off/-*[9]
501	AE15	SD2_DATA2	IO	I	GP6_12/TDI2*[8]	I/I	Off/-*[9]
502	AG14	SD2_DATA3	IO	I	GP6_13*[8]	I/I	Off/-*[9]
503	AJ14	SD2_CD	IO	I	GP6_14	I	Off
504	AF14	SD2_WP	IO	I	GP6_15	I	Off
505	AD15	VCCQ_SD2	-	P	VCCQ_SD2	P	-
506	AL13	SD3_CLK	IO	I/Z*7	GP6_16/TDO3*[8]	I/Z*[7]	Off/-*[9]
507	AH13	SD3_CMD	IO	I	GP6_17/TRST3#*[8]	I/I	Off/-*[9]
508	AG13	SD3_DATA0	IO	I	GP6_18/TCK3*[8]	I/I	Off/-*[9]
509	AF13	SD3_DATA1	IO	I	GP6_19/TMS3*[8]	I/I	Off/-*[9]
510	AE14	SD3_DATA2	IO	I	GP6_20/TDI3*[8]	I/I	Off/-*[9]
511	AE13	SD3_DATA3	IO	I	GP6_21*[8]	I/I	Off/-*[9]

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
512	AK13	SD3_CD	IO	I	GP6_22	I	Off
513	AJ13	SD3_WP	IO	I	GP6_23	I	Off
514	AD13	VCCQ_SD3	-	P	VCCQ_SD3	P	-
515	T31	MSIOF0_SCK	IO	I	GP6_24	I	On
516	T30	MSIOF0_SYNC	IO	I	GP6_25	I	On
517	T29	MSIOF0_TXD	IO	I	GP6_26	I	On
518	T28	MSIOF0_RXD	IO	I	GP6_27	I	On
519	T27	MSIOF0_SS1	IO	I	GP6_28	I	On
520	T26	MSIOF0_SS2	IO	I	GP6_29	I	On
521	R26	SIM0_RST	IO	I(MDT1)	GP4_29	I	Off
522	R28	SIM0_CLK	IO	I(MDT0)	GP4_30	I	Off
523	R27	SIM0_D	IO	I	GP4_31	I	On
524	R31	GPS_CLK	IO	I	GP7_20	I	On
525	R30	GPS_SIGN	IO	I	GP7_21	I	On
526	R29	GPS_MAG	IO	I	GP7_22	I	On
527	AJ18	I2C5_SCL	IO	Z	I2C5_SCL	Z	-
528	AH18	I2C5_SDA	IO	Z	I2C5_SDA	Z	-
529	AJ19	IIC3_SCL	IO	Z	IIC3_SCL	Z	-
530	AH19	IIC3_SDA	IO	Z	IIC3_SDA	Z	-
531	P28	HCTS0#	IO	I	GP7_0	I	On
532	R25	HRTS0#	IO	I	GP7_1	I	On
533	P31	HSCK0	IO	I	GP7_2	I	On
534	P29	HRX0	IO	I	GP7_3	I	On
535	P30	HTX0	IO	I	GP7_4	I	Off
536	V25	HRX1	IO	I	GP7_5	I	Off
537	V26	HTX1	IO	I	GP7_6	I	Off
538	U31	HSCK1	IO	I	GP7_7	I	-
539	U29	HCTS1#	IO	I	GP7_8	I	-
540	U28	HRTS1#	IO	I	GP7_9	I	-
541	AK16	VSS	-	P	VSS	P	-
542	U27	NC	-	IO	Reserved	IO	-
543	U26	VDD_MLBPLL	-	P	VDD_MLBPLL	P	-
544	U25	VSS_MLBPLL	-	P	VSS_MLBPLL	P	-
545	L31	NC	-	Z	Reserved	Z	-
546	K31	NC	-	Z	Reserved	Z	-
547	N31	NC	-	Z	Reserved	Z	-
548	M31	NC	-	Z	Reserved	Z	-
549	L29	NC	-	Z	Reserved	Z	-
550	L28	NC	-	Z	Reserved	Z	-
551	M29	NC	-	Z	Reserved	Z	-
552	M28	NC	-	Z	Reserved	Z	-
553	N25	VDD_MLBPPLL0	-	P	VDD_MLBPPLL0	P	-
554	P25	VSS_MLBPPLL0	-	P	VSS_MLBPPLL0	P	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
555	N26	VDD_MLBPPLL1	-	P	VDD_MLBPPLL1	P	-
556	P26	VSS_MLBPPLL1	-	P	VSS_MLBPPLL1	P	-
557	K28	VCCQ18_MLBP	-	P	VCCQ18_MLBP	P	-
558	N28	VCCQ18_MLBP	-	P	VCCQ18_MLBP	P	-
559	K29	VCCQ33_MLBP	-	P	VCCQ33_MLBP	P	-
560	N29	VCCQ33_MLBP	-	P	VCCQ33_MLBP	P	-
561	P27	VTHSENSE0	O	O	VTHSENSE0	O	-
562	N27	VTHREF0	O	O	VTHREF0	O	-

Notes:
1. No.94, 95, 98 to 106 and 108 to 129: Default Pin Function
   MD[28:27],[22] = 111: DBSC3 channel 1 32-bit operation
   MD[28:27],[22] = 011 or 110: GP_DDRn (n = 1 to 29) operation
2. No.134 to 187: Default Pin Function
   MD[28:27],[22] = 111: DBSC3 channel 1 32-bit operation
   MD[28:27],[22] = 011: DBSC channel 0 64-bit (M0DQ[63:32] enable) operation
   MD[28:27],[22] = 110: Reserved except for power supply pins.
3. No.204 and 205: AVS Default State
   The output is high or low, depending on product.
4. No.213 to 254: Default Pin Function
   MD[24:23] = 00: SATA1 and SATA0
   MD[24:23] = 01: SATA1 and USB3.0
   MD[24:23] = 10: PCIe and SATA0
   MD[24:23] = 11: PCIe and USB3.0
5. No.293 to 334, 336, 337, 344, 345 and 347 to 349: Default Pin Function
   MD[3:1] = 000: LBSC (D[15:0], A[25:0], CS0#, CS1#/A26, BS#, RD#, WE[1:0]# and EX_WAIT0
   MD[3:1] ≠ 000: GPIO (GP0_[31:0], GP1_[11:0], [19:18] and [23:21])
6. No.337 CS1#/A26: Default State
   MD4 = 0: (64-Mbyte mode): high output
   MD4 = 1: (128-Mbyte mode): low output
7. No.497 and 506: Default State
   "I" is in function mode (SDHI), "Z" is in debug mode.
8. No.497 to 502 and 506 to 511: Default Pin Function
   Depends on MD[21:20], MD[12:10], and MDT[1:0] settings.
9. No.497 to 502 and No.506 to 511: Default Pull-up
   "-" is in debugging operation only; "Off" is in other than debugging operation.

4.3 Handling of Unused Pins

Table 4.3 shows a handling of unused pins of the RZ/G1M.

"Unused pin" means all modules that are multiplexed to the pin should be disable and unused in this section. For handling of some unused pin which belongs to the enable module should be handled following the notification of the module manual. Unless otherwise specified in the module manual, follow the Table 4.3 for handling of unused pins.

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Pin Name: Pin name of function 1 in pin multiplex table, I/O: Input or output direction considered about all multiplexed pin functions of the pin.

Mode Pin: All mode pins must be used during power-on reset.

Boot: These pins must be used in boot operation (LBSC area 0 or QSPI).

Default pull-up: Internal pull-up control function is available or not from a power-on reset and its pull-up state.

"On": Pull-up control function is available and default state is pulled-up.

(No.212, ACK pin is available internal pull-down function.)

"Off": Pull-up control function is available and default state is not pulled-up.

"-": Pull-up control function is not available.

For details of pull-up control function, refer to PUPR0 through PUPR7 registers in section 5, Pin Function Controller (PFC).

Notes:
1. All power supply pins and ground pins include VCCQ, VCCQ18, VDD, VDD_DVFS, VDDQ_M0, VDDQ_M1, VDDQ_M1A and VSS pins must be used.
2. All mode pins (MD[14:0], [24:19], [28:27] and MDT[1:0]) must be used during power-on reset. For details of mode pin setting, refer to section 3.3, Mode Pin Settings.
3. Boot module related pins (LBSC or QSPI) should be used during boot operation. For details of QSPI boot, refer to section 18, Booting.
4. Refer to Table 4.1, List of Multiplexed Pin Functions for multiplexed pin and module of each pin.

Table 4.3 Handling of Unused Pins

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
1	F20	M0CKE0	L	-	-	-	Open
2	C19	M0CKE1	L	-	-	-	Open
3	G16	VSS	P	-	-	-	Must be used
4	H18	M0BKPRST#	I	-	-	-	Pulled-up to VDDQ_M0BKUP or pulled-down to VSS
5	E19	M0RESET#	H to L	-	-	-	Open
6	G20	M0CK0	O	-	-	-	Open
7	G19	M0CK0#	O	-	-	-	Open
8	G17	M0CK1	O	-	-	-	Open
9	G18	M0CK1#	O	-	-	-	Open
10	B20	M0CS0#	H	-	-	-	Open
11	A19	M0CS1#	H	-	-	-	Open
12	D20	M0ODT0	L	-	-	-	Open
13	E18	M0ODT1	L	-	-	-	Open
14	H16	M0ZQ	IO	-	-	-	Must be used
15	E21	M0WE#	H	-	-	-	Open
16	D22	M0RAS#	H	-	-	-	Open
17	C22	M0CAS#	H	-	-	-	Open
18	E17	M0A0	L	-	-	-	Open
19	B22	M0A1	L	-	-	-	Open
20	A22	M0A2	L	-	-	-	Open
21	D17	M0A3	L	-	-	-	Open
22	A21	M0A4	L	-	-	-	Open
23	D16	M0A5	L	-	-	-	Open
24	B17	M0A6	L	-	-	-	Open
25	B21	M0A7	L	-	-	-	Open
26	A16	M0A8	L	-	-	-	Open
27	B18	M0A9	L	-	-	-	Open
28	C18	M0A10	L	-	-	-	Open
29	A18	M0A11	L	-	-	-	Open
30	E16	M0A12	L	-	-	-	Open
31	A17	M0A13	L	-	-	-	Open
32	B16	M0A14	L	-	-	-	Open
33	D18	M0A15	L	-	-	-	Open
34	C21	M0BA0	L	-	-	-	Open
35	C16	M0BA1	L	-	-	-	Open
36	D21	M0BA2	L	-	-	-	Open
37	G21	VDDQ_M0APLL	P	-	-	-	Must be used
38	H21	VSSQ_M0APLL	P	-	-	-	Must be used
39	A27	M0DQ0	Z	-	-	-	Open
40	C28	M0DQ1	Z	-	-	-	Open
41	D27	M0DQ2	Z	-	-	-	Open
42	A29	M0DQ3	Z	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
43	B27	M0DQ4	Z	-	-	-	Open
44	B29	M0DQ5	Z	-	-	-	Open
45	C27	M0DQ6	Z	-	-	-	Open
46	A30	M0DQ7	Z	-	-	-	Open
47	E26	M0DQS0	Z	-	-	-	Open
48	E25	M0DQS0#	Z	-	-	-	Open
49	A28	M0DM0	Z	-	-	-	Open
50	G22	VDDQ_M0DPLL0	P	-	-	-	Must be used
51	G23	VSSQ_M0DPLL0	P	-	-	-	Must be used
52	G24	M0VREFDQ0	P	-	-	-	Must be used
53	B23	M0DQ8	Z	-	-	-	Open
54	A24	M0DQ9	Z	-	-	-	Open
55	C24	M0DQ10	Z	-	-	-	Open
56	D24	M0DQ11	Z	-	-	-	Open
57	B26	M0DQ12	Z	-	-	-	Open
58	D26	M0DQ13	Z	-	-	-	Open
59	B24	M0DQ14	Z	-	-	-	Open
60	A25	M0DQ15	Z	-	-	-	Open
61	E23	M0DQS1	Z	-	-	-	Open
62	E24	M0DQS1#	Z	-	-	-	Open
63	C25	M0DM1	Z	-	-	-	Open
64	F22	VDDQ_M0DPLL1	P	-	-	-	Must be used
65	F23	VSSQ_M0DPLL1	P	-	-	-	Must be used
66	E31	M0DQ16	Z	-	-	-	Open
67	C30	M0DQ17	Z	-	-	-	Open
68	E29	M0DQ18	Z	-	-	-	Open
69	B31	M0DQ19	Z	-	-	-	Open
70	E30	M0DQ20	Z	-	-	-	Open
71	C31	M0DQ21	Z	-	-	-	Open
72	E28	M0DQ22	Z	-	-	-	Open
73	D29	M0DQ23	Z	-	-	-	Open
74	F27	M0DQS2	Z	-	-	-	Open
75	G27	M0DQS2#	Z	-	-	-	Open
76	D31	M0DM2	Z	-	-	-	Open
77	K25	VDDQ_M0DPLL2	P	-	-	-	Must be used
78	J25	VSSQ_M0DPLL2	P	-	-	-	Must be used
79	H25	M0VREFDQ1	P	-	-	-	Must be used
80	F28	M0DQ24	Z	-	-	-	Open
81	G31	M0DQ25	Z	-	-	-	Open
82	F30	M0DQ26	Z	-	-	-	Open
83	H30	M0DQ27	Z	-	-	-	Open
84	H28	M0DQ28	Z	-	-	-	Open
85	J30	M0DQ29	Z	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
86	H29	M0DQ30	Z	-	-	-	Open
87	H31	M0DQ31	Z	-	-	-	Open
88	J27	M0DQS3	Z	-	-	-	Open
89	H27	M0DQS3#	Z	-	-	-	Open
90	G29	M0DM3	Z	-	-	-	Open
91	K26	VDDQ_M0DPLL3	P	-	-	-	Must be used
92	J26	VSSQ_M0DPLL3	P	-	-	-	Must be used
93	H19	VDDQ_M0BKUP	P	-	-	-	Must be used
94	F5	M1CKE0	O	-	-	-	Open
95	G3	M1CKE1	O	-	-	-	Open
96	H7	M1VREFCA	P	-	-	-	Must be used
97	J7	M1BKPRST#	I	-	-	-	Pulled-up to VDDQ_M1BKUP or pulled-down to VSS
98	G5	M1RESET#	O	-	-	-	Open
99	J5	M1CK0	O	-	-	-	Open
100	H5	M1CK0#	O	-	-	-	Open
101	L5	M1CK1	O	-	-	-	Open
102	K5	M1CK1#	O	-	-	-	Open
103	F2	M1CS0#	H/I	-	-	-	Open
104	G1	M1CS1#	H/I	-	-	-	Open
105	F4	M1ODT0	L/I	-	-	-	Open
106	H4	M1ODT1	L/I	-	-	-	Open
107	L8	M1ZQ	IO	-	-	-	Must be used
108	E3	M1WE#	H/Z	-	-	-	Open
109	D3	M1RAS#	H/Z	-	-	-	Open
110	E4	M1CAS#	H/I	-	-	-	Open
111	B1	M1A0	L/Z	-	-	-	Open
112	H2	M1A1	L/I	-	-	-	Open
113	E2	M1A2	L/Z	-	-	-	Open
114	M3	M1A3	L/I	-	-	-	Open
115	E1	M1A4	L/Z	-	-	-	Open
116	D1	M1A5	L/Z	-	-	-	Open
117	K2	M1A6	L/Z	-	-	-	Open
118	H1	M1A7	L/I	-	-	-	Open
119	M1	M1A8	L/I	-	-	-	Open
120	J2	M1A9	L/Z	-	-	-	Open
121	L3	M1A10	L/I	-	-	-	Open
122	K1	M1A11	L/Z	-	-	-	Open
123	C2	M1A12	L/Z	-	-	-	Open
124	L1	M1A13	L/I	-	-	-	Open
125	M2	M1A14	L/I	-	-	-	Open
126	K3	M1A15	L/Z	-	-	-	Open
127	J3	M1BA0	L/Z	-	-	-	Open
128	C1	M1BA1	L/Z	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
129	H3	M1BA2	L/I	-	-	-	Open
130	L7	VDDQ_M1APLL	P	-	-	-	Must be used
131	K7	VSSQ_M1APLL	P	-	-	-	Must be used
132	L6	VDDQ_M1MPLL	P	-	-	-	Must be used
133	K6	VSSQ_M1MPLL	P	-	-	-	Must be used
134	B12	M1DQ0	Z	-	-	-	Open
135	B11	M1DQ1	Z	-	-	-	Open
136	D12	M1DQ2	Z	-	-	-	Open
137	A10	M1DQ3	Z	-	-	-	Open
138	C11	M1DQ4	Z	-	-	-	Open
139	D10	M1DQ5	Z	-	-	-	Open
140	C10	M1DQ6	Z	-	-	-	Open
141	D11	M1DQ7	Z	-	-	-	Open
142	E12	M1DQS0	Z	-	-	-	Open
143	E11	M1DQS0#	Z	-	-	-	Open
144	A11	M1DM0	Z	-	-	-	Open
145	G13	VDDQ_M1DPLL0	P	-	-	-	Must be used
146	G12	VSSQ_M1DPLL0	P	-	-	-	Must be used
147	G14	M1VREFDQ0	P	-	-	-	Must be used
148	A13	M1DQ8	Z	-	-	-	Open
149	A14	M1DQ9	Z	-	-	-	Open
150	D14	M1DQ10	Z	-	-	-	Open
151	B14	M1DQ11	Z	-	-	-	Open
152	C14	M1DQ12	Z	-	-	-	Open
153	B15	M1DQ13	Z	-	-	-	Open
154	D15	M1DQ14	Z	-	-	-	Open
155	A15	M1DQ15	Z	-	-	-	Open
156	E14	M1DQS1	Z	-	-	-	Open
157	E13	M1DQS1#	Z	-	-	-	Open
158	C13	M1DM1	Z	-	-	-	Open
159	F13	VDDQ_M1DPLL1	P	-	-	-	Must be used
160	F12	VSSQ_M1DPLL1	P	-	-	-	Must be used
161	B6	M1DQ16	Z	-	-	-	Open
162	A7	M1DQ17	Z	-	-	-	Open
163	C8	M1DQ18	Z	-	-	-	Open
164	B8	M1DQ19	Z	-	-	-	Open
165	D8	M1DQ20	Z	-	-	-	Open
166	A8	M1DQ21	Z	-	-	-	Open
167	D6	M1DQ22	Z	-	-	-	Open
168	B9	M1DQ23	Z	-	-	-	Open
169	E8	M1DQS2	Z	-	-	-	Open
170	E9	M1DQS2#	Z	-	-	-	Open
171	C7	M1DM2	Z	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
172	F10	VDDQ_M1DPLL2	P	-	-	-	Must be used
173	F9	VSSQ_M1DPLL2	P	-	-	-	Must be used
174	G8	M1VREFDQ1	P	-	-	-	Must be used
175	B3	M1DQ24	Z	-	-	-	Open
176	D5	M1DQ25	Z	-	-	-	Open
177	C4	M1DQ26	Z	-	-	-	Open
178	C5	M1DQ27	Z	-	-	-	Open
179	A5	M1DQ28	Z	-	-	-	Open
180	A3	M1DQ29	Z	-	-	-	Open
181	B5	M1DQ30	Z	-	-	-	Open
182	A2	M1DQ31	Z	-	-	-	Open
183	E7	M1DQS3	Z	-	-	-	Open
184	E6	M1DQS3#	Z	-	-	-	Open
185	A4	M1DM3	Z	-	-	-	Open
186	G10	VDDQ_M1DPLL3	P	-	-	-	Must be used
187	G9	VSSQ_M1DPLL3	P	-	-	-	Must be used
188	G6	VDDQ_M1BKUP	P	-	-	-	Must be used
189	AL18	EXTAL	I	-	-	-	Must be used
190	AL17	XTAL	O	-	-	-	Open
191	F16	VDD_CPGPLL1	P	-	-	-	Must be used
192	F15	VSS_CPGPLL1	P	-	-	-	Must be used
193	H15	VDD_CPGPLL2	P	-	-	-	Must be used
194	G15	VSS_CPGPLL2	P	-	-	-	Must be used
195	L25	VDD_CPGPLL0	P	-	-	-	Must be used
196	M25	VSS_CPGPLL0	P	-	-	-	Must be used
197	L26	VDD_CPGPLL3	P	-	-	-	Must be used
198	M26	VSS_CPGPLL3	P	-	-	-	Must be used
199	AE19	PRESET#	I	-	-	-	Must be used
200	U5	PRESETOUT#	L to H	-	-	-	Open
201	AG19	MPMD0	I	-	-	-	Must be used (pulled-down to VSS)
202	AG18	MPMD1	I	-	-	-	Must be used (pulled-down to VSS)
203	AF17	BSMODE	I	-	-	-	Must be used
204	U6	AVS1	O	-	-	Off	Open
205	U7	AVS2	O	-	-	Off	Open
206	AD19	VCCQ_ISO	P	-	-	-	Must be used
207	AF19	TRST#	I	-	-	On	Pulled-down to VSS
208	AE18	TCK	I	-	-	On	Open
209	AF18	TMS	I	-	-	On	Open
210	AH17	TDI	I	-	-	On	Open
211	AJ17	TDO	Z	-	-	-	Open
212	AE17	ACK	I	-	-	On (pull-down)	Open
213	AL23	RIDP1_SATA	I	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
214	AL24	RIDN1_SATA	I	-	-	-	Open
215	AL25	TODP1_SATA	O	-	-	-	Open
216	AL26	TODN1_SATA	O	-	-	-	Open
217	AJ26	CICREFP1_SATA	I	-	-	-	Fixed to VSS_SATA1
218	AJ25	CICREFN1_SATA	I	-	-	-	Fixed to VSS_SATA1
219	AE23	VSS_SATA1	P	-	-	-	Must be used
220	AF24	VDDA_SATA1	P	-	-	-	Must be used
221	AG24	VDDA_SATA1	P	-	-	-	Must be used
222	AF23	VDDD_SATA1	P	-	-	-	Must be used
223	AG23	VDDD_SATA1	P	-	-	-	Must be used
224	AH24	VDDD_SATA1	P	-	-	-	Must be used
225	AD23	VSS_SATA1	P	-	-	-	Must be used
226	AE24	VSS_SATA1	P	-	-	-	Must be used
227	AJ24	VSS_SATA1	P	-	-	-	Must be used
228	AK24	VSS_SATA1	P	-	-	-	Must be used
229	AK25	VSS_SATA1	P	-	-	-	Must be used
230	AK26	VSS_SATA1	P	-	-	-	Must be used
231	AK23	VSS_SATA1	P	-	-	-	Must be used
232	AL27	RIDP0_SATA	I	-	-	-	Open
233	AL28	RIDN0_SATA	I	-	-	-	Open
234	AL29	TODP0_SATA	O	-	-	-	Open
235	AL30	TODN0_SATA	O	-	-	-	Open
236	AJ28	CICREFP0_SATA	I	-	-	-	Fixed to VSS_SATA0
237	AJ27	CICREFN0_SATA	I	-	-	-	Fixed to VSS_SATA0
238	AF25	VSS_SATA0	P	-	-	-	Must be used
239	AG26	VDDA_SATA0	P	-	-	-	Must be used
240	AH27	VDDA_SATA0	P	-	-	-	Must be used
241	AH25	VDDD_SATA0	P	-	-	-	Must be used
242	AH26	VDDD_SATA0	P	-	-	-	Must be used
243	AG25	VDDD_SATA0	P	-	-	-	Must be used
244	AD24	VSS_SATA0	P	-	-	-	Must be used
245	AE25	VSS_SATA0	P	-	-	-	Must be used
246	AF26	VSS_SATA0	P	-	-	-	Must be used
247	AG27	VSS_SATA0	P	-	-	-	Must be used
248	AK27	VSS_SATA0	P	-	-	-	Must be used
249	AH28	VSS_SATA0	P	-	-	-	Must be used
250	AK28	VSS_SATA0	P	-	-	-	Must be used
251	AJ29	VSS_SATA0	P	-	-	-	Must be used
252	AK29	VSS_SATA0	P	-	-	-	Must be used
253	AK30	VSS_SATA0	P	-	-	-	Must be used
254	AL31	VSS_SATA0	P	-	-	-	Must be used
255	AL20	USB_EXTAL	I	-	-	-	Pulled-down to VSS
256	AL19	USB_XTAL	O	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
257	AG31	USB0_DP	I	-	-	-	Open
258	AH31	USB0_DM	I	-	-	-	Open
259	AG29	USB0_RREF	P	-	-	-	Must be used
260	AE27	VD331	P	-	-	-	Must be used
261	AD26	VD181	P	-	-	-	Must be used
262	AB24	AVDD	P	-	-	-	Must be used
263	AC24	AVSS	P	-	-	-	Must be used
264	AF31	USB0_PWEN	L	-	-	Off	Open
265	AF30	USB0_OVC/VBUS	I	-	-	On	Open
266	AJ31	USB1_DP	I	-	-	-	Open
267	AK31	USB1_DM	I	-	-	-	Open
268	AH29	USB1_RREF	P	-	-	-	Must be used
269	AF28	VD331	P	-	-	-	Must be used
270	AC25	AVDD	P	-	-	-	Must be used
271	AD25	AVSS	P	-	-	-	Must be used
272	AE26	AVSS	P	-	-	-	Must be used
273	AF27	AVSS	P	-	-	-	Must be used
274	AG28	AVSS	P	-	-	-	Must be used
275	AE28	USB1_PWEN	L	-	-	Off	Open
276	AD27	USB1_OVC	I	-	-	On	Open
277	AE20	DU0_LVDS_CLK_P	Z	-	-	-	Open
278	AF20	DU0_LVDS_CLK_N	Z	-	-	-	Open
279	AJ23	DU0_LVDS_CH0_P	Z	-	-	-	Open
280	AJ22	DU0_LVDS_CH0_N	Z	-	-	-	Open
281	AL21	DU0_LVDS_CH1_P	Z	-	-	-	Open
282	AL22	DU0_LVDS_CH1_N	Z	-	-	-	Open
283	AJ20	DU0_LVDS_CH2_P	Z	-	-	-	Open
284	AJ21	DU0_LVDS_CH2_N	Z	-	-	-	Open
285	AG22	DU0_LVDS_CH3_P	Z	-	-	-	Open
286	AG21	DU0_LVDS_CH3_N	Z	-	-	-	Open
287	AG17	DU0_DOTCLKIN	I	-	-	On	Open
288	AD22	VDDQ_LVDS	P	-	-	-	Must be used
289	AE22	VDDQ_LVDS	P	-	-	-	Must be used
290	AF22	VDDQ_LVDS	P	-	-	-	Must be used
291	AD20	DU0_LVDS_PLL1_VCC	P	-	-	-	Must be used
292	AD21	DU0_LVDS_PLL1_VSS	P	-	-	-	Must be used
293	AA7	D0	I	-	Area 0*1	On	Open
294	AA6	D1	I	-	Area 0*1	On	Open
295	AA5	D2	I	-	Area 0*1	On	Open
296	AA4	D3	I	-	Area 0*1	On	Open
297	AA3	D4	I	-	Area 0*1	On	Open
298	AA2	D5	I	-	Area 0*1	On	Open
299	AA1	D6	I	-	Area 0*1	On	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
300	Y7	D7	I	-	Area 0*1	On	Open
301	Y6	D8	I	-	Area 0*1	On	Open
302	Y5	D9	I	-	Area 0*1	On	Open
303	Y4	D10	I	-	Area 0*1	On	Open
304	Y3	D11	I	-	Area 0*1	On	Open
305	Y2	D12	I	-	Area 0*1	On	Open
306	Y1	D13	I	-	Area 0*1	On	Open
307	W2	D14	I	-	Area 0*1	On	Open
308	W1	D15	I	-	Area 0*1	On	Open
309	T7	A0	L/I	-	Area 0*1	On	Open
310	W7	A1	L/I	MD28	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
311	W6	A2	L/I	MD23	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
312	W5	A3	L/I	MD13	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
313	W4	A4	L/I	MD24	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
314	W3	A5	L/I	-	Area 0*1	On	Open
315	T6	A6	L/I	-	Area 0*1	On	Open
316	V7	A7	L/I	MD27	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
317	T5	A8	L/I	-	Area 0*1	On	Open
318	T4	A9	L/I	-	Area 0*1	On	Open
319	V6	A10	L/I	MD22	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
320	T3	A11	L/I	-	Area 0*1	On	Open
321	T2	A12	L/I	-	Area 0*1	On	Open
322	R7	A13	L/I	MD21	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
323	R6	A14	L/I	MD19	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
324	R5	A15	L/I	MD20	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
325	R4	A16	L/I	-	Area 0*1	On	Open
326	R3	A17	L/I	-	-	On	Open
327	R2	A18	L/I	-	-	On	Open
328	P7	A19	L/I	MD14	-	Off	Pulled-up to VCCQ or pulled-down to VSS
329	P6	A20	L/I	-	QSPI*2	On	Open
330	P5	A21	L/I	-	QSPI*2	On	Open
331	P4	A22	L/I	-	QSPI*2	On	Open
332	P3	A23	L/I	-	QSPI*2	On	Open
333	P2	A24	L/I	-	QSPI*2	On	Open
334	P1	A25	L/I	-	QSPI*2	On	Open
335	U1	CLKOUT	O	-	Area 0*1	-	Open
336	T1	CS0#	H/I	-	Area 0*1	On	Open
337	R1	[CS1#/A26]	[O]/I	-	Area 0*1	On	Open
338	V1	EX_CS0#	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
339	N1	EX_CS1#	I	-	-	On	Open
340	N2	EX_CS2#	I	-	-	On	Open
341	V3	EX_CS3#	I	MD9	-	Off	Pulled-up to VCCQ or pulled-down to VSS
342	V4	EX_CS4#	I	-	-	On	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
343	V5	EX_CS5#	I	MD8	-	Off	Pulled-up to VCCQ or pulled-down to VSS
344	N3	BS#	H/I	MD10	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
345	V2	RD#	H/I	MD12	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
346	N4	RD/WR#	I	-	-	On	Open
347	N5	WE0#	H/I	MD6	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
348	N6	WE1#	H/I	MD4	Area 0*1	Off	Pulled-up to VCCQ or pulled-down to VSS
349	U3	EX_WAIT0	I	-	Area 0*1	On	Open
350	U4	DREQ0	I	-	-	On	Open
351	N7	DACK0	I	MD7	-	Off	Pulled-up to VCCQ or pulled-down to VSS
352	T25	SPEEDIN	I	-	-	On	Open
353	V31	SSI_SCK0129	I	-	-	On	Open
354	V30	SSI_WS0129	I	-	-	On	Open
355	V29	SSI_SDATA0	I	-	-	On	Open
356	W31	SSI_SCK1	I	-	-	On	Open
357	V28	SSI_WS1	I	-	-	On	Open
358	V27	SSI_SDATA1	I	-	-	On	Open
359	W30	SSI_SCK2	I	-	-	On	Open
360	W29	SSI_WS2	I	-	-	On	Open
361	W28	SSI_SDATA2	I	-	-	On	Open
362	W27	SSI_SCK34	I	-	-	On	Open
363	W26	SSI_WS34	I	-	-	On	Open
364	W25	SSI_SDATA3	I	-	-	On	Open
365	Y31	SSI_SCK4	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
366	Y30	SSI_WS4	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
367	Y29	SSI_SDATA4	I	-	-	On	Open
368	Y28	SSI_SCK5	I	-	-	On	Open
369	Y27	SSI_WS5	I	-	-	On	Open
370	Y26	SSI_SDATA5	I	-	-	On	Open
371	AA31	SSI_SCK6	I	-	-	On	Open
372	AA30	SSI_WS6	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
373	AA29	SSI_SDATA6	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
374	AA27	SSI_SCK78	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
375	AA26	SSI_WS78	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
376	Y25	SSI_SDATA7	I	-	-	On	Open
377	AA25	SSI_SDATA8	I	-	-	On	Open
378	AB31	SSI_SCK9	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
379	AB30	SSI_WS9	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
380	AB29	SSI_SDATA9	I	-	-	On	Open
381	AD31	AUDIO_CLKA	I	-	-	On	Open
382	AC30	AUDIO_CLKB	I	-	-	On	Open
383	AD30	AUDIO_CLKC	I	-	-	On	Open
384	AE31	AUDIO_CLKOUT	I	MD5	-	Off	Pulled-up to VCCQ or pulled-down to VSS
385	AL16	NMI	I	-	-	-	Must be used

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
386	AE30	IRQ0	I	-	-	On	Open
387	AE29	IRQ1	I	-	-	On	Open
388	AD29	IRQ2	I	-	-	On	Open
389	AD28	IRQ3	I	-	-	On	Open
390	AC29	IRQ4	I	-	-	On	Open
391	AC28	IRQ5	I	-	-	On	Open
392	AC27	IRQ6	I	-	-	On	Open
393	AB26	IRQ7	I	-	-	On	Open
394	AB27	IRQ8	I	-	-	On	Open
395	AB28	IRQ9	I	-	-	On	Open
396	AL12	DU1_DR0	I	-	-	On	Open
397	AK12	DU1_DR1	I	-	-	On	Open
398	AJ12	DU1_DR2	I	-	-	On	Open
399	AH12	DU1_DR3	I	-	-	On	Open
400	AG12	DU1_DR4	I	-	-	On	Open
401	AF12	DU1_DR5	I	-	-	On	Open
402	AE12	DU1_DR6	I	-	-	On	Open
403	AE11	DU1_DR7	I	-	-	On	Open
404	AL11	DU1_DG0	I	-	-	On	Open
405	AK11	DU1_DG1	I	-	-	On	Open
406	AJ11	DU1_DG2	I	-	-	On	Open
407	AH11	DU1_DG3	I	-	-	On	Open
408	AG11	DU1_DG4	I	-	-	On	Open
409	AF11	DU1_DG5	I	-	-	On	Open
410	AF10	DU1_DG6	I	-	-	On	Open
411	AE10	DU1_DG7	I	-	-	On	Open
412	AJ9	DU1_DB0	I	-	-	On	Open
413	AH9	DU1_DB1	I	-	-	On	Open
414	AG9	DU1_DB2	I	-	-	On	Open
415	AF9	DU1_DB3	I	-	-	On	Open
416	AE9	DU1_DB4	I	-	-	On	Open
417	AJ10	DU1_DB5	I	MD11	-	Off	Pulled-up to VCCQ or pulled-down to VSS
418	AH10	DU1_DB6	I	-	-	On	Open
419	AG10	DU1_DB7	I	-	-	On	Open
420	AL9	DU1_DOTCLKIN	I	-	-	On	Open
421	AL10	DU1_DOTCLKOUT0	I	-	-	On	Open
422	AK10	DU1_DOTCLKOUT1	I	-	-	On	Open
423	AE8	DU1_EXHSYNC/DU1_HSYNC	I	MD3	-	Off	Pulled-up to VCCQ or pulled-down to VSS
424	AF8	DU1_EXVSYNC/DU1_VSYNC	I	MD2	-	Off	Pulled-up to VCCQ or pulled-down to VSS
425	AG8	DU1_EXODDF/DU1_ODDF/DISP/CDE	I	-	-	On	Open
426	AH8	DU1_DISP	I	MD1	-	Off	Pulled-up to VCCQ or pulled-down to VSS

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
427	AJ8	DU1_CDE	I	MD0	-	Off	Pulled-up to VCCQ or pulled-down to VSS
428	AC1	VI0_CLK	I	-	-	On	Open
429	AB1	VI0_CLKENB	I	-	-	On	Open
430	AC2	VI0_FIELD	I	-	-	On	Open
431	AB2	VI0_HSYNC#	I	-	-	On	Open
432	AB3	VI0_VSYNC#	I	-	-	On	Open
433	AB4	VI0_DATA0/VI0_B0	I	-	-	On	Open
434	AB5	VI0_DATA1/VI0_B1	I	-	-	On	Open
435	AB6	VI0_DATA2/VI0_B2	I	-	-	On	Open
436	AC3	VI0_DATA3/VI0_B3	I	-	-	On	Open
437	AB7	VI0_DATA4/VI0_B4	I	-	-	On	Open
438	AC4	VI0_DATA5/VI0_B5	I	-	-	On	Open
439	AC6	VI0_DATA6/VI0_B6	I	-	-	On	Open
440	AC7	VI0_DATA7/VI0_B7	I	-	-	On	Open
441	AD1	VI0_G0	I	-	-	On	Open
442	AD2	VI0_G1	I	-	-	On	Open
443	AD3	VI0_G2	I	-	-	On	Open
444	AD4	VI0_G3	I	-	-	On	Open
445	AD5	VI0_G4	I	-	-	On	Open
446	AD6	VI0_G5	I	-	-	On	Open
447	AE6	VI0_G6	I	-	-	On	Open
448	AD7	VI0_G7	I	-	-	On	Open
449	AE1	VI0_R0	I	-	-	On	Open
450	AE3	VI0_R1	I	-	-	On	Open
451	AE4	VI0_R2	I	-	-	On	Open
452	AE5	VI0_R3	I	-	-	On	Open
453	AF3	VI0_R4	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
454	AF4	VI0_R5	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
455	AF5	VI0_R6	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
456	AG4	VI0_R7	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
457	AF1	VI1_HSYNC#	I	-	-	On	Open
458	AF2	VI1_VSYNC#	I	-	-	On	Open
459	AG3	VI1_CLKENB	I	-	-	On	Open
460	AH2	VI1_FIELD	I	-	-	On	Open
461	AG1	VI1_CLK	I	-	-	On	Open
462	AH3	VI1_DATA0	I	-	-	On	Open
463	AH1	VI1_DATA1	I	-	-	On	Open
464	AJ1	VI1_DATA2	I	-	-	On	Open
465	AJ2	VI1_DATA3	I	-	-	On	Open
466	AK1	VI1_DATA4	I	-	-	On	Open
467	AL2	VI1_DATA5	I	-	-	On	Open
468	AK3	VI1_DATA6	I	-	-	On	Open
469	AJ4	VI1_DATA7	I	-	-	On	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
470	AL3	ETH_MDIO	I	-	-	On	Open
471	AK4	ETH_CRS_DV	I	-	-	On	Open
472	AL4	ETH_RX_ER	I	-	-	On	Open
473	AH5	ETH_RXD0	I	-	-	On	Open
474	AL5	ETH_RXD1	I	-	-	On	Open
475	AH6	ETH_LINK	I	-	-	On	Open
476	AL6	ETH_REFCLK	I	-	-	On	Open
477	AJ5	ETH_TXD1	I	-	-	On	Open
478	AG6	ETH_TX_EN	I	-	-	On	Open
479	AJ6	ETH_MAGIC	I	-	-	On	Open
480	AG7	ETH_TXD0	I	-	-	On	Open
481	AF7	ETH_MDC	I	-	-	On	Open
482	AK8	STP_IVCXO27_0	I	-	-	On	Open
483	AL8	STP_ISCLK_0	I	-	-	On	Open
484	AH7	STP_ISD_0	I	-	-	On	Open
485	AJ7	STP_ISEN_0	I	-	-	On	Open
486	AK7	STP_ISSYNC_0	I	-	-	On	Open
487	AL7	STP_OPWM_0	I	-	-	On	Open
488	AL15	SD0_CLK	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
489	AH16	SD0_CMD	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
490	AG16	SD0_DATA0	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
491	AF16	SD0_DATA1	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
492	AE16	SD0_DATA2	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
493	AH15	SD0_DATA3	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
494	AJ15	SD0_CD	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
495	AJ16	SD0_WP	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
496	AD16	VCCQ_SD0	-	-	-	-	Must be used
497	AL14	SD2_CLK	I	-	-	Off	Pulled-up to VCCQ_SD2 or pulled-down to VSS
498	AH14	SD2_CMD	I	-	-	Off	Pulled-up to VCCQ_SD2 or pulled-down to VSS
499	AG15	SD2_DATA0	I	-	-	Off	Pulled-up to VCCQ_SD2 or pulled-down to VSS
500	AF15	SD2_DATA1	I	-	-	Off	Pulled-up to VCCQ_SD2 or pulled-down to VSS
501	AE15	SD2_DATA2	I	-	-	Off	Pulled-up to VCCQ_SD2 or pulled-down to VSS
502	AG14	SD2_DATA3	I	-	-	Off	Pulled-up to VCCQ_SD2 or pulled-down to VSS
503	AJ14	SD2_CD	I	-	-	Off	Pulled-up to VCCQ_SD2 or pulled-down to VSS
504	AF14	SD2_WP	I	-	-	Off	Pulled-up to VCCQ_SD2 or pulled-down to VSS
505	AD15	VCCQ_SD2	P	-	-	-	Must be used
506	AL13	SD3_CLK	I	-	-	Off	Pulled-up to VCCQ_SD3 or pulled-down to VSS
507	AH13	SD3_CMD	I	-	-	Off	Pulled-up to VCCQ_SD3 or pulled-down to VSS
508	AG13	SD3_DATA0	I	-	-	Off	Pulled-up to VCCQ_SD3 or pulled-down to VSS
509	AF13	SD3_DATA1	I	-	-	Off	Pulled-up to VCCQ_SD3 or pulled-down to VSS
510	AE14	SD3_DATA2	I	-	-	Off	Pulled-up to VCCQ_SD3 or pulled-down to VSS
511	AE13	SD3_DATA3	I	-	-	Off	Pulled-up to VCCQ_SD3 or pulled-down to VSS
512	AK13	SD3_CD	I	-	-	Off	Pulled-up to VCCQ_SD3 or pulled-down to VSS

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
513	AJ13	SD3_WP	I	-	-	Off	Pulled-up to VCCQ_SD3 or pulled-down to VSS
514	AD13	VCCQ_SD3	P	-	-	-	Must be used
515	T31	MSIOF0_SCK	I	-	-	On	Open
516	T30	MSIOF0_SYNC	I	-	-	On	Open
517	T29	MSIOF0_TXD	I	-	-	On	Open
518	T28	MSIOF0_RXD	I	-	-	On	Open
519	T27	MSIOF0_SS1	I	-	-	On	Open
520	T26	MSIOF0_SS2	I	-	-	On	Open
521	R26	SIM0_RST	I	MDT1	-	Off	Pulled-up to VCCQ or pulled-down to VSS
522	R28	SIM0_CLK	I	MDT0	-	Off	Pulled-up to VCCQ or pulled-down to VSS
523	R27	SIM0_D	I	-	-	On	Open
524	R31	GPS_CLK	I	-	-	On	Open
525	R30	GPS_SIGN	I	-	-	On	Open
526	R29	GPS_MAG	I	-	-	On	Open
527	AJ18	I2C5_SCL	Z	-	-	-	Pulled-up to VCCQ18
528	AH18	I2C5_SDA	Z	-	-	-	Pulled-up to VCCQ18
529	AJ19	IIC3_SCL	Z	-	-	-	Pulled-up to VCCQ18
530	AH19	IIC3_SDA	Z	-	-	-	Pulled-up to VCCQ18
531	P28	HCTS0#	I	-	-	On	Open
532	R25	HRTS0#	I	-	-	On	Open
533	P31	HSCK0	I	-	-	On	Open
534	P29	HRX0	I	-	-	On	Open
535	P30	HTX0	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
536	V25	HRX1	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
537	V26	HTX1	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
538	U31	HSCK1	I	-	-	-	Pulled-up to VCCQ or pulled-down to VSS
539	U29	HCTS1#	I	-	-	-	Pulled-up to VCCQ or pulled-down to VSS
540	U28	HRTS1#	I	-	-	-	Pulled-up to VCCQ or pulled-down to VSS
541	AK16	VSS	P	-	-	-	Must be used
542	U27	NC	IO	-	-	-	Open
543	U26	VDD_MLBPLL	P	-	-	-	Must be used
544	U25	VSS_MLBPLL	P	-	-	-	Must be used
545	L31	NC	Z	-	-	-	Open
546	K31	NC	Z	-	-	-	Open
547	N31	NC	Z	-	-	-	Open
548	M31	NC	Z	-	-	-	Open
549	L29	NC	Z	-	-	-	Open
550	L28	NC	Z	-	-	-	Open
551	M29	NC	Z	-	-	-	Open
552	M28	NC	Z	-	-	-	Open
553	N25	VDD_MLBPPLL0	P	-	-	-	Must be used
554	P25	VSS_MLBPPLL0	P	-	-	-	Must be used
555	N26	VDD_MLBPPLL1	P	-	-	-	Must be used

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
556	P26	VSS_MLBPPLL1	P	-	-	-	Must be used
557	K28	VCCQ18_MLBP	P	-	-	-	Must be used
558	N28	VCCQ18_MLBP	P	-	-	-	Must be used
559	K29	VCCQ33_MLBP	P	-	-	-	Must be used
560	N29	VCCQ33_MLBP	P	-	-	-	Must be used
561	P27	VTHSENSE0	O	-	-	-	Open or fixed to VSS*3
562	N27	VTHREF0	O	-	-	-	Open or fixed to VSS*3

Notes: 1. No.293 to 325, 335 to 337, 344, 345 and 347 to 349: Boot
Minimum number of pins that is necessary for area 0 boot operation must be used.

2. No.329 to 334: Boot
These pins must be used for QSPI boot.

3. No.561 and 562: Pin handling when not in use
Thermal sensor should be idle state (THSCR.THIDLE[1:0] = B'11) when fixed to VSS. For details, refer to section 60, Thermal Sensor (THS/TSC).

5. Pin Function Controller (PFC)

5.1 Overview

The pin function controller (PFC) is a module that consists of registers for selecting the function of the multiplexed pins and controlling the pull-up resistor on each LSI pin.

5.1.1 Features

- Register access through the APB bus interface
- Setting multiplexed pin functions for LSI pins

  Function of the RZ/G1M pin selectable by setting the registers in the PFC module

  (The function of the LSI pin can be selected by the GPIO/peripheral function select registers 0 to 7 (GPSR0 to GPSR7) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16) in the PFC module. For details, see sections 5.3.2, GPIO/Peripheral Function Select Register 0 (GPSR0) through 5.3.26, Peripheral Function Select Register 16 (IPSR16).)
- Module selection

  Enable and disable the functions of RZ/G1M LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module.

  (Selection is handled by the module select register (MOD_SEL), module select register 2 (MOD_SEL2), module select register 3 (MOD_SEL3) and module register4 (MOD_SEL4). For details, see sections 5.3.27, Module Select Register (MOD_SEL), through 5.3.30, Module Select Register 4 (MOD_SEL4).
- Pull-up control for each LSI pin.

  On/off of the pull-up or pull-down resistors on each LSI pin can be controlled by setting the registers in the PFC module.

  (The pull-up or pull-down resistors on each LSI pin can be turned on or off individually by setting the LSI pin pull-up/down control registers 0 to 7 (PUPR0 to PUPR7) in the PFC module. For details, see sections 5.3.31, LSI Pin Pull-Up Control Register 0 (PUPR0) through 5.3.38, LSI Pin Pull-Up Control Register 7 (PUPR7).)
- Control of IO functions, including SDHI, IRQ, DU, Ethernet, ADG, SSI and LBSC.

  SDIO functions, including the driving ability, POC of pins, can be controlled by setting registers of the PFC module. For details, see sections 5.3.39, SD Control Register 0 (IOCTRL0) through 5.3.44, IIC3 (DVFS) and TDBG IO Cell Control Register (IOCTRL7).

  DDR3 GPIO function can also be selected by setting registers of the PFC. For details, see sections 5.3.45, DDR3 General Port IO Enable Register (DDR3GPEN) through 5.3.48, DDR3 General Port Input Data Register (DDR3GPID).

5.2 Register Configuration

All the registers in the PFC are mapped into the APB bus space. Table 5.1 shows the configuration of the registers provided in the PFC. For details on the registers of the PFC, see section 5.3, Register Description.

Table 5.1 Configuration of Registers in PFC

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
LSI multiplexed pin setting mask register	PMMR	R/W	H'0000 0000	H'E606 0000	32	—
GPIO/peripheral function select register 0	GPSR0	R/W	H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	H'E606 0004	32	—
GPIO/peripheral function select register 1	GPSR1	R/W	H'00EC 0FFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000), or H'00EC 0FFF (in power-on reset)	H'E606 0008	32	—
GPIO/peripheral function select register 2	GPSR2	R/W	H'0000 0000	H'E606 000C	32	—
GPIO/peripheral function select register 3	GPSR3	R/W	H'0000 0000	H'E606 0010	32	—
GPIO/peripheral function select register 4	GPSR4	R/W	H'0000 0000	H'E606 0014	32	—
GPIO/peripheral function select register 5	GPSR5	R/W	H'0000 0000	H'E606 0018	32	—
GPIO/peripheral function select register 6	GPSR6	R/W	H'4000 0000	H'E606 001C	32	—
GPIO/peripheral function select register 7	GPSR7	R/W	H'0380 0000	H'E606 0074	32	—
Peripheral function select register 0	IPSR0	R/W	H'0000 0000	H'E606 0020	32	—
Peripheral function select register 1	IPSR1	R/W	H'0000 0000	H'E606 0024	32	—
Peripheral function select register 2	IPSR2	R/W	H'0000 0000	H'E606 0028	32	—
Peripheral function select register 3	IPSR3	R/W	H'0000 0000	H'E606 002C	32	—
Peripheral function select register 4	IPSR4	R/W	H'0000 0000	H'E606 0030	32	—
Peripheral function select register 5	IPSR5	R/W	H'0000 0000	H'E606 0034	32	—
Peripheral function select register 6	IPSR6	R/W	H'0000 0000	H'E606 0038	32	—
Peripheral function select register 7	IPSR7	R/W	H'0000 0000	H'E606 003C	32	—

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
Peripheral function select register 8	IPSR8	R/W	H'0000 0000	H'E606 0040	32	—
Peripheral function select register 9	IPSR9	R/W	H'0000 0000	H'E606 0044	32	—
Peripheral function select register 10	IPSR10	R/W	H'0000 0000	H'E606 0048	32	—
Peripheral function select register 11	IPSR11	R/W	H'0000 0000	H'E606 004C	32	—
Peripheral function select register 12	IPSR12	R/W	H'0000 0000	H'E606 0050	32	—
Peripheral function select register 13	IPSR13	R/W	H'0000 0000	H'E606 0054	32	—
Peripheral function select register 14	IPSR14	R/W	H'0000 0000	H'E606 0058	32	—
Peripheral function select register 15	IPSR15	R/W	H'0000 0000	H'E606 005C	32	—
Peripheral function select register 16	IPSR16	R/W	H'0000 0000	H'E606 0160	32	—
Module select register	MOD_SEL	R/W	H'0000 0000	H'E606 0090	32	—
Module select register 2	MOD_SEL2	R/W	H'0000 0000	H'E606 0094	32	—
Module select register 3	MOD_SEL3	R/W	H'0000 0000	H'E606 0098	32	—
Module select register 4	MOD_SEL4	R/W	H'0000 0000	H'E606 009C	32	—
LSI pin pull-up control register 0	PUPR0	R/W	H'D87F FFFF	H'E606 0100	32	—
LSI pin pull-up control register 1	PUPR1	R/W	H'EC8B7DC6	H'E606 0104	32	—
LSI pin pull-up control register 2	PUPR2	R/W	H'DE61 F3FF	H'E606 0108	32	—
LSI pin pull-up control register 3	PUPR3	R/W	H'DFFF FFFF	H'E606 010C	32	—
LSI pin pull-up control register 4	PUPR4	R/W	H'FFFF FF27	H'E606 0110	32	—
LSI pin pull-up control register 5	PUPR5	R/W	H'FFFF FFE1	H'E606 0114	32	—
LSI pin pull-up control register 6	PUPR6	R/W	H'F000 000F	H'E606 0118	32	—
LSI pin pull-up control register 7	PUPR7	R/W	H'015C 0FF3	H'E606 011C	32	—
SD control register 0	IOCTRL0	R/W	H'8000 FFFF	H'E606 0060	32	—
SD control register 1	IOCTRL1	R/W	H'FFFF FFFF	H'E606 0064	32	—
TDSEL control register 4	IOCTRL4	R/W	H'0000 0000	H'E606 0084	32	—
TDSEL control register 5	IOCTRL5	R/W	H'0000 0000	H'E606 0088	32	—
POC control register	IOCTRL6	R/W	H'FFFF FFFF	H'E606 008C	32	—
IIC3 (DVFS) and TDBG IO cell control register	IOCTRL7	R/W	H'0000 0000	H'E606 0070	32	—
DDR3 general port io enable register	DDR3GPEN	R/W	H'0000_0000	H'E606 0240	32	—
DDR3 general port output enable register	DDR3GPOE	R/W	H'0000_0000	H'E606 0244	32	—

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
DDR3 general port output data register	DDR3GPOD	R/W	H'0000_0000	H'E606 0248	32	—
DDR3 general port input data register	DDR3GPID	R	H'XXXX_XXX0	H'E606 024C	32	—

5.3 Register Description

[Legend]

Initial value:	Register value after a reset
:	Undefined value
R/W:	Readable/writable. The written value can be read.
R:	Read-only. The write value should always be 0.
R/WC0:	Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.
R/WC1:	Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.
W:	Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.
—/W:	Write-only. The read value is undefined.

All the bits are active high unless otherwise specified, and deactivated on reset.

All access to registers is made in longword units.

The write value to a reserved bit should always be 0.

5.3.1 LSI Multiplexed Pin Setting Mask Register (PMMR)

Function: PMMR enables/disables writing to the multiplexed pin setting registers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PMPM															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PMPM															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PMPM[31:0]	H'0000 0000	R/W	Multiplexed Pin Setting Mask Writing a value to any register from among the GPIO/peripheral function select registers GPSR0 to GPSR7, peripheral function select registers IPSR0 to IPSR16, module select registers MOD_SEL, MOD_SEL2, MOD_SEL3 and MOD_SEL4, IO cell control registers IOCTRL0, IOCTRL1 and IOCTRL4 to IOCTRL7 is enabled by writing the inverse of the value to this register.

Note: This register must be set before setting each of the GPIO/peripheral function select registers GPSR0 to GPSR7, peripheral function select registers IPSR0 to IPSR16, module select registers MOD_SEL, MOD_SEL2, MOD_SEL3 and MOD_SEL4, IO cell control registers IOCTRL0, IOCTRL1 and IOCTRL4 to IOCTRL7.

5.3.2 GPIO/Peripheral Function Select Register 0 (GPSR0)

Function: GPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP0 [31]	GP0 [30]	GP0 [29]	GP0 [28]	GP0 [27]	GP0 [26]	GP0 [25]	GP0 [24]	GP0 [23]	GP0 [22]	GP0 [21]	GP0 [20]	GP0 [19]	GP0 [18]	GP0 [17]	GP0 [16]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP0 [15]	GP0 [14]	GP0 [13]	GP0 [12]	GP0 [11]	GP0 [10]	GP0 [9]	GP0 [8]	GP0 [7]	GP0 [6]	GP0 [5]	GP0 [4]	GP0 [3]	GP0 [2]	GP0 [1]	GP0 [0]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP0[31:0]	H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000 or power-on reset)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP0[0]	GP-0-0	Peripheral function selected by IP0[0]
GP0[1]	GP-0-1	Peripheral function selected by IP0[1]
GP0[2]	GP-0-2	Peripheral function selected by IP0[2]
GP0[3]	GP-0-3	Peripheral function selected by IP0[3]
GP0[4]	GP-0-4	Peripheral function selected by IP0[4]
GP0[5]	GP-0-5	Peripheral function selected by IP0[5]
GP0[6]	GP-0-6	Peripheral function selected by IP0[6]
GP0[7]	GP-0-7	Peripheral function selected by IP0[7]
GP0[8]	GP-0-8	Peripheral function selected by IP0[8]
GP0[9]	GP-0-9	Peripheral function selected by IP0[9]
GP0[10]	GP-0-10	Peripheral function selected by IP0[10]
GP0[11]	GP-0-11	Peripheral function selected by IP0[11]
GP0[12]	GP-0-12	Peripheral function selected by IP0[12]
GP0[13]	GP-0-13	Peripheral function selected by IP0[13]
GP0[14]	GP-0-14	Peripheral function selected by IP0[14]
GP0[15]	GP-0-15	Peripheral function selected by IP0[15]
GP0[16]	GP-0-16	Peripheral function selected by IP0[18:16]
GP0[17]	GP-0-17	Peripheral function selected by IP0[20:19]
GP0[18]	GP-0-18	Peripheral function selected by IP0[22:21]
GP0[19]	GP-0-19	Peripheral function selected by IP0[24:23]
GP0[20]	GP-0-20	Peripheral function selected by IP0[26:25]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP0[21]	GP-0-21	Peripheral function selected by IP0[28:27]
GP0[22]	GP-0-22	Peripheral function selected by IP0[30:29]
GP0[23]	GP-0-23	Peripheral function selected by IP1[1:0]
GP0[24]	GP-0-24	Peripheral function selected by IP1[3:2]
GP0[25]	GP-0-25	Peripheral function selected by IP1[5:4]
GP0[26]	GP-0-26	Peripheral function selected by IP1[7:6]
GP0[27]	GP-0-27	Peripheral function selected by IP1[10:8]
GP0[28]	GP-0-28	Peripheral function selected by IP1[13:11]
GP0[29]	GP-0-29	Peripheral function selected by IP1[16:14]
GP0[30]	GP-0-30	Peripheral function selected by IP1[19:17]
GP0[31]	GP-0-31	Peripheral function selected by IP1[22:20]

5.3.3 GPIO/Peripheral Function Select Register 1 (GPSR1)

Function: GPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP1 [31]	GP1 [30]	GP1 [29]	GP1 [28]	GP1 [27]	GP1 [26]	GP1 [25]	GP1 [24]	GP1 [23]	GP1 [22]	GP1 [21]	GP1 [20]	GP1 [19]	GP1 [18]	GP1 [17]	GP1 [16]
Initial value:	0	0	0	0	0	0	0	0	1/0	1/0	1/0	0	1/0	1/0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP1 [15]	GP1 [14]	GP1 [13]	GP1 [12]	GP1 [11]	GP1 [10]	GP1 [9]	GP1 [8]	GP1 [7]	GP1 [6]	GP1 [5]	GP1 [4]	GP1 [3]	GP1 [2]	GP1 [1]	GP1 [0]
Initial value:	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP1[31:0]	H'00EC 0FFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000), or H'00EC 0FFF (in power-on reset)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[0]	GP-1-0	Peripheral function selected by IP1[25:23]
GP1[1]	GP-1-1	Peripheral function selected by IP1[28:26]
GP1[2]	GP-1-2	Peripheral function selected by IP1[31:29]
GP1[3]	GP-1-3	Peripheral function selected by IP2[2:0]
GP1[4]	GP-1-4	Peripheral function selected by IP2[4:3]
GP1[5]	GP-1-5	Peripheral function selected by IP2[6:5]
GP1[6]	GP-1-6	Peripheral function selected by IP2[9:7]
GP1[7]	GP-1-7	Peripheral function selected by IP2[12:10]
GP1[8]	GP-1-8	Peripheral function selected by IP2[15:13]
GP1[9]	GP-1-9	Peripheral function selected by IP2[18:16]
GP1[10]	GP-1-10	Peripheral function selected by IP2[20:19]
GP1[11]	GP-1-11	Peripheral function selected by IP2[22:21]
GP1[12]	GP-1-12	EX_CS0#
GP1[13]	GP-1-13	Peripheral function selected by IP2[24:23]
GP1[14]	GP-1-14	Peripheral function selected by IP2[26:25]
GP1[15]	GP-1-15	Peripheral function selected by IP2[29:27]
GP1[16]	GP-1-16	Peripheral function selected by IP3[2:0]
GP1[17]	GP-1-17	Peripheral function selected by IP3[5:3]
GP1[18]	GP-1-18	Peripheral function selected by IP3[8:6]
GP1[19]	GP-1-19	RD#
GP1[20]	GP-1-20	Peripheral function selected by IP3[11:9]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[21]	GP-1-21	Peripheral function selected by IP3[13:12]
GP1[22]	GP-1-22	Peripheral function selected by IP3[15:14]
GP1[23]	GP-1-23	Peripheral function selected by IP3[17:16]
GP1[24]	GP-1-24	Peripheral function selected by IP3[19:18]
GP1[25]	GP-1-25	Peripheral function selected by IP3[21:20]
GP1[26]	—	—
GP1[27]	—	—
GP1[28]	—	—
GP1[29]	—	—
GP1[30]	—	—
GP1[31]	—	—

5.3.4 GPIO/Peripheral Function Select Register 2 (GPSR2)

Function: GPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP2 [31]	GP2 [30]	GP2 [29]	GP2 [28]	GP2 [27]	GP2 [26]	GP2 [25]	GP2 [24]	GP2 [23]	GP2 [22]	GP2 [21]	GP2 [20]	GP2 [19]	GP2 [18]	GP2 [17]	GP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP2 [15]	GP2 [14]	GP2 [13]	GP2 [12]	GP2 [11]	GP2 [10]	GP2 [9]	GP2 [8]	GP2 [7]	GP2 [6]	GP2 [5]	GP2 [4]	GP2 [3]	GP2 [2]	GP2 [1]	GP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP2[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP2[0]	GP-2-0	Peripheral function selected by IP3[27:25]
GP2[1]	GP-2-1	Peripheral function selected by IP3[30:28]
GP2[2]	GP-2-2	Peripheral function selected by IP4[1:0]
GP2[3]	GP-2-3	Peripheral function selected by IP4[4:2]
GP2[4]	GP-2-4	Peripheral function selected by IP4[7:5]
GP2[5]	GP-2-5	Peripheral function selected by IP4[9:8]
GP2[6]	GP-2-6	Peripheral function selected by IP4[12:10]
GP2[7]	GP-2-7	Peripheral function selected by IP4[15:13]
GP2[8]	GP-2-8	Peripheral function selected by IP4[18:16]
GP2[9]	GP-2-9	Peripheral function selected by IP4[19]
GP2[10]	GP-2-10	Peripheral function selected by IP4[20]
GP2[11]	GP-2-11	Peripheral function selected by IP4[21]
GP2[12]	GP-2-12	Peripheral function selected by IP4[23:22]
GP2[13]	GP-2-13	Peripheral function selected by IP4[25:24]
GP2[14]	GP-2-14	Peripheral function selected by IP4[27:26]
GP2[15]	GP-2-15	Peripheral function selected by IP4[30:28]
GP2[16]	GP-2-16	Peripheral function selected by IP5[2:0]
GP2[17]	GP-2-17	Peripheral function selected by IP5[5:3]
GP2[18]	GP-2-18	Peripheral function selected by IP5[8:6]
GP2[19]	GP-2-19	Peripheral function selected by IP5[11:9]
GP2[20]	GP-2-20	Peripheral function selected by IP5[14:12]
GP2[21]	GP-2-21	Peripheral function selected by IP5[16:15]
GP2[22]	GP-2-22	Peripheral function selected by IP5[19:17]
GP2[23]	GP-2-23	Peripheral function selected by IP5[21:20]
GP2[24]	GP-2-24	Peripheral function selected by IP5[23:22]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP2[25]	GP-2-25	Peripheral function selected by IP5[25:24]
GP2[26]	GP-2-26	Peripheral function selected by IP5[28:26]
GP2[27]	GP-2-27	Peripheral function selected by IP5[31:29]
GP2[28]	GP-2-28	AUDIO_CLKA
GP2[29]	GP-2-29	Peripheral function selected by IP6[2:0]
GP2[30]	GP-2-30	Peripheral function selected by IP6[5:3]
GP2[31]	GP-2-31	Peripheral function selected by IP6[7:6]

5.3.5 GPIO/Peripheral Function Select Register 3 (GPSR3)

Function: GPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP3 [31]	GP3 [30]	GP3 [29]	GP3 [28]	GP3 [27]	GP3 [26]	GP3 [25]	GP3 [24]	GP3 [23]	GP3 [22]	GP3 [21]	GP3 [20]	GP3 [19]	GP3 [18]	GP3 [17]	GP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP3 [15]	GP3 [14]	GP3 [13]	GP3 [12]	GP3 [11]	GP3 [10]	GP3 [9]	GP3 [8]	GP3 [7]	GP3 [6]	GP3 [5]	GP3 [4]	GP3 [3]	GP3 [2]	GP3 [1]	GP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP3[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP3[0]	GP-3-0	Peripheral function selected by IP7[5:3]
GP3[1]	GP-3-1	Peripheral function selected by IP7[8:6]
GP3[2]	GP-3-2	Peripheral function selected by IP7[10:9]
GP3[3]	GP-3-3	Peripheral function selected by IP7[12:11]
GP3[4]	GP-3-4	Peripheral function selected by IP7[14:13]
GP3[5]	GP-3-5	Peripheral function selected by IP7[16:15]
GP3[6]	GP-3-6	Peripheral function selected by IP7[18:17]
GP3[7]	GP-3-7	Peripheral function selected by IP7[20:19]
GP3[8]	GP-3-8	Peripheral function selected by IP7[23:21]
GP3[9]	GP-3-9	Peripheral function selected by IP7[26:24]
GP3[10]	GP-3-10	Peripheral function selected by IP7[29:27]
GP3[11]	GP-3-11	Peripheral function selected by IP8[2:0]
GP3[12]	GP-3-12	Peripheral function selected by IP8[5:3]
GP3[13]	GP-3-13	Peripheral function selected by IP8[8:6]
GP3[14]	GP-3-14	Peripheral function selected by IP8[11:9]
GP3[15]	GP-3-15	Peripheral function selected by IP8[14:12]
GP3[16]	GP-3-16	Peripheral function selected by IP8[17:15]
GP3[17]	GP-3-17	Peripheral function selected by IP8[20:18]
GP3[18]	GP-3-18	Peripheral function selected by IP8[23:21]
GP3[19]	GP-3-19	Peripheral function selected by IP8[25:24]
GP3[20]	GP-3-20	Peripheral function selected by IP8[27:26]
GP3[21]	GP-3-21	Peripheral function selected by IP8[30:28]
GP3[22]	GP-3-22	Peripheral function selected by IP9[2:0]
GP3[23]	GP-3-23	Peripheral function selected by IP9[5:3]
GP3[24]	GP-3-24	Peripheral function selected by IP9[6]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP3[25]	GP-3-25	Peripheral function selected by IP9[7]
GP3[26]	GP-3-26	Peripheral function selected by IP9[10:8]
GP3[27]	GP-3-27	Peripheral function selected by IP9[11]
GP3[28]	GP-3-28	Peripheral function selected by IP9[12]
GP3[29]	GP-3-29	Peripheral function selected by IP9[15:13]
GP3[30]	GP-3-30	Peripheral function selected by IP9[16]
GP3[31]	GP-3-31	Peripheral function selected by IP9[18:17]

5.3.6 GPIO/Peripheral Function Select Register 4 (GPSR4)

Function: GPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP4 [31]	GP4 [30]	GP4 [29]	GP4 [28]	GP4 [27]	GP4 [26]	GP4 [25]	GP4 [24]	GP4 [23]	GP4 [22]	GP4 [21]	GP4 [20]	GP4 [19]	GP4 [18]	GP4 [17]	GP4 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP4 [15]	GP4 [14]	GP4 [13]	GP4 [12]	GP4 [11]	GP4 [10]	GP4 [9]	GP4 [8]	GP4 [7]	GP4 [6]	GP4 [5]	GP4 [4]	GP4 [3]	GP4 [2]	GP4 [1]	GP4 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP4[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP4[0]	GP-4-0	VI0_CLK
GP4[1]	GP-4-1	Peripheral function selected by IP9[20:19]
GP4[2]	GP-4-2	Peripheral function selected by IP9[22:21]
GP4[3]	GP-4-3	Peripheral function selected by IP9[24:23]
GP4[4]	GP-4-4	Peripheral function selected by IP9[26:25]
GP4[5]	GP-4-5	VI0_DATA0_VI0_B0
GP4[6]	GP-4-6	VI0_DATA1_VI0_B1
GP4[7]	GP-4-7	VI0_DATA2_VI0_B2
GP4[8]	GP-4-8	Peripheral function selected by IP9[28:27]
GP4[9]	GP-4-9	VI0_DATA4_VI0_B4
GP4[10]	GP-4-10	VI0_DATA5_VI0_B5
GP4[11]	GP-4-11	VI0_DATA6_VI0_B6
GP4[12]	GP-4-12	VI0_DATA7_VI0_B7
GP4[13]	GP-4-13	Peripheral function selected by IP9[31:29]
GP4[14]	GP-4-14	Peripheral function selected by IP10[2:0]
GP4[15]	GP-4-15	Peripheral function selected by IP10[5:3]
GP4[16]	GP-4-16	Peripheral function selected by IP10[8:6]
GP4[17]	GP-4-17	Peripheral function selected by IP10[11:9]
GP4[18]	GP-4-18	Peripheral function selected by IP10[14:12]
GP4[19]	GP-4-19	Peripheral function selected by IP10[16:15]
GP4[20]	GP-4-20	Peripheral function selected by IP10[18:17]
GP4[21]	GP-4-21	Peripheral function selected by IP10[21:19]
GP4[22]	GP-4-22	Peripheral function selected by IP10[24:22]
GP4[23]	GP-4-23	Peripheral function selected by IP10[26:25]
GP4[24]	GP-4-24	Peripheral function selected by IP10[28:27]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP4[25]	GP-4-25	Peripheral function selected by IP10[31:29]
GP4[26]	GP-4-26	Peripheral function selected by IP11[2:0]
GP4[27]	GP-4-27	Peripheral function selected by IP11[5:3]
GP4[28]	GP-4-28	Peripheral function selected by IP11[8:6]
GP4[29]	GP-4-29	Peripheral function selected by IP15[1:0]
GP4[30]	GP-4-30	Peripheral function selected by IP15[3:2]
GP4[31]	GP-4-31	Peripheral function selected by IP15[5:4]

5.3.7 GPIO/Peripheral Function Select Register 5 (GPSR5)

Function: GPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP5 [31]	GP5 [30]	GP5 [29]	GP5 [28]	GP5 [27]	GP5 [26]	GP5 [25]	GP5 [24]	GP5 [23]	GP5 [22]	GP5 [21]	GP5 [20]	GP5 [19]	GP5 [18]	GP5 [17]	GP5 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP5 [15]	GP5 [14]	GP5 [13]	GP5 [12]	GP5 [11]	GP5 [10]	GP5 [9]	GP5 [8]	GP5 [7]	GP5 [6]	GP5 [5]	GP5 [4]	GP5 [3]	GP5 [2]	GP5 [1]	GP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP5[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP5[0]	GP-5-0	Peripheral function selected by IP11[11:9]
GP5[1]	GP-5-1	Peripheral function selected by IP11[14:12]
GP5[2]	GP-5-2	Peripheral function selected by IP11[16:15]
GP5[3]	GP-5-3	Peripheral function selected by IP11[18:17]
GP5[4]	GP-5-4	Peripheral function selected by IP11[19]
GP5[5]	GP-5-5	Peripheral function selected by IP11[20]
GP5[6]	GP-5-6	Peripheral function selected by IP11[21]
GP5[7]	GP-5-7	Peripheral function selected by IP11[22]
GP5[8]	GP-5-8	Peripheral function selected by IP11[23]
GP5[9]	GP-5-9	Peripheral function selected by IP11[24]
GP5[10]	GP-5-10	Peripheral function selected by IP11[25]
GP5[11]	GP-5-11	Peripheral function selected by IP11[26]
GP5[12]	GP-5-12	Peripheral function selected by IP11[27]
GP5[13]	GP-5-13	Peripheral function selected by IP11[29:28]
GP5[14]	GP-5-14	Peripheral function selected by IP11[31:30]
GP5[15]	GP-5-15	Peripheral function selected by IP12[1:0]
GP5[16]	GP-5-16	Peripheral function selected by IP12[3:2]
GP5[17]	GP-5-17	Peripheral function selected by IP12[6:4]
GP5[18]	GP-5-18	Peripheral function selected by IP12[9:7]
GP5[19]	GP-5-19	Peripheral function selected by IP12[12:10]
GP5[20]	GP-5-20	Peripheral function selected by IP12[15:13]
GP5[21]	GP-5-21	Peripheral function selected by IP12[17:16]
GP5[22]	GP-5-22	Peripheral function selected by IP12[19:18]
GP5[23]	GP-5-23	Peripheral function selected by IP12[21:20]
GP5[24]	GP-5-24	Peripheral function selected by IP12[23:22]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP5[25]	GP-5-25	Peripheral function selected by IP12[26:24]
GP5[26]	GP-5-26	Peripheral function selected by IP12[29:27]
GP5[27]	GP-5-27	Peripheral function selected by IP13[2:0]
GP5[28]	GP-5-28	Peripheral function selected by IP13[4:3]
GP5[29]	GP-5-29	Peripheral function selected by IP13[6:5]
GP5[30]	GP-5-30	Peripheral function selected by IP13[9:7]
GP5[31]	GP-5-31	Peripheral function selected by IP3[24:22]

5.3.8 GPIO/Peripheral Function Select Register 6 (GPSR6)

Function: GPSR6 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP6 [31]	GP6 [30]	GP6 [29]	GP6 [28]	GP6 [27]	GP6 [26]	GP6 [25]	GP6 [24]	GP6 [23]	GP6 [22]	GP6 [21]	GP6 [20]	GP6 [19]	GP6 [18]	GP6 [17]	GP6 [16]
Initial value:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP6 [15]	GP6 [14]	GP6 [13]	GP6 [12]	GP6 [11]	GP6 [10]	GP6 [9]	GP6 [8]	GP6 [7]	GP6 [6]	GP6 [5]	GP6 [4]	GP6 [3]	GP6 [2]	GP6 [1]	GP6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP6[31:0]	H'4000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP6[0]	GP-6-0	Peripheral function selected by IP13[10]
GP6[1]	GP-6-1	Peripheral function selected by IP13[11]
GP6[2]	GP-6-2	Peripheral function selected by IP13[12]
GP6[3]	GP-6-3	Peripheral function selected by IP13[13]
GP6[4]	GP-6-4	Peripheral function selected by IP13[14]
GP6[5]	GP-6-5	Peripheral function selected by IP13[15]
GP6[6]	GP-6-6	Peripheral function selected by IP13[18:16]
GP6[7]	GP-6-7	Peripheral function selected by IP13[21:19]
GP6[8]	GP-6-8	SD2_CLK
GP6[9]	GP-6-9	Peripheral function selected by IP13[22]
GP6[10]	GP-6-10	Peripheral function selected by IP13[24:23]
GP6[11]	GP-6-11	Peripheral function selected by IP13[25]
GP6[12]	GP-6-12	Peripheral function selected by IP13[26]
GP6[13]	GP-6-13	Peripheral function selected by IP13[27]
GP6[14]	GP-6-14	Peripheral function selected by IP13[30:28]
GP6[15]	GP-6-15	Peripheral function selected by IP14[1:0]
GP6[16]	GP-6-16	Peripheral function selected by IP14[2]
GP6[17]	GP-6-17	Peripheral function selected by IP14[3]
GP6[18]	GP-6-18	Peripheral function selected by IP14[4]
GP6[19]	GP-6-19	Peripheral function selected by IP14[5]
GP6[20]	GP-6-20	Peripheral function selected by IP14[6]
GP6[21]	GP-6-21	Peripheral function selected by IP14[7]
GP6[22]	GP-6-22	Peripheral function selected by IP14[10:8]
GP6[23]	GP-6-23	Peripheral function selected by IP14[13:11]
GP6[24]	GP-6-24	Peripheral function selected by IP14[16:14]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP6[25]	GP-6-25	Peripheral function selected by IP14[19:17]
GP6[26]	GP-6-26	Peripheral function selected by IP14[22:20]
GP6[27]	GP-6-27	Peripheral function selected by IP14[25:23]
GP6[28]	GP-6-28	Peripheral function selected by IP14[28:26]
GP6[29]	GP-6-29	Peripheral function selected by IP14[31:29]
GP6[30]	GP-6-30	USB1_OVC
GP6[31]	GP-6-31	DU0_DOTCLKIN

5.3.9 GPIO/Peripheral Function Select Register 7 (GPSR7)

Function: GPSR7 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP7 [31]	GP7 [30]	GP7 [29]	GP7 [28]	GP7 [27]	GP7 [26]	GP7 [25]	GP7 [24]	GP7 [23]	GP7 [22]	GP7 [21]	GP7 [20]	GP7 [19]	GP7 [18]	GP7 [17]	GP7 [16]
Initial value:	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP7 [15]	GP7 [14]	GP7 [13]	GP7 [12]	GP7 [11]	GP7 [10]	GP7 [9]	GP7 [8]	GP7 [7]	GP7 [6]	GP7 [5]	GP7 [4]	GP7 [3]	GP7 [2]	GP7 [1]	GP7 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP7[31:0]	H'0380 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP7[0]	GP-7-0	Peripheral function selected by IP15[17:15]
GP7[1]	GP-7-1	Peripheral function selected by IP15[20:18]
GP7[2]	GP-7-2	Peripheral function selected by IP15[23:21]
GP7[3]	GP-7-3	Peripheral function selected by IP15[26:24]
GP7[4]	GP-7-4	Peripheral function selected by IP15[29:27]
GP7[5]	GP-7-5	Peripheral function selected by IP16[2:0]
GP7[6]	GP-7-6	Peripheral function selected by IP16[5:3]
GP7[7]	GP-7-7	Peripheral function selected by IP16[7:6]
GP7[8]	GP-7-8	Peripheral function selected by IP16[9:8]
GP7[9]	GP-7-9	Peripheral function selected by IP16[11:10]
GP7[10]	GP-7-10	Peripheral function selected by IP6[9:8]
GP7[11]	GP-7-11	Peripheral function selected by IP6[11:10]
GP7[12]	GP-7-12	Peripheral function selected by IP6[13:12]
GP7[13]	GP-7-13	Peripheral function selected by IP6[15:14]
GP7[14]	GP-7-14	Peripheral function selected by IP6[18:16]
GP7[15]	GP-7-15	Peripheral function selected by IP6[20:19]
GP7[16]	GP-7-16	Peripheral function selected by IP6[23:21]
GP7[17]	GP-7-17	Peripheral function selected by IP6[26:24]
GP7[18]	GP-7-18	Peripheral function selected by IP6[29:27]
GP7[19]	GP-7-19	Peripheral function selected by IP7[2:0]
GP7[20]	GP-7-20	Peripheral function selected by IP15[8:6]
GP7[21]	GP-7-21	Peripheral function selected by IP15[11:9]
GP7[22]	GP-7-22	Peripheral function selected by IP15[14:12]
GP7[23]	GP-7-23	USB0_PWEN
GP7[24]	GP-7-24	USB0_OVC

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP7[25]	GP-7-25	USB1_PWEN
GP7[26]	GP-7-26	—
GP7[27]	GP-7-27	—
GP7[28]	GP-7-28	—
GP7[29]	GP-7-29	—
GP7[30]	GP-7-30	—
GP7[31]	GP-7-31	—

5.3.10 Peripheral Function Select Register 0 (IPSR0)

Function: IPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP0 [30]	IP0 [29]	IP0 [28]	IP0 [27]	IP0 [26]	IP0 [25]	IP0 [24]	IP0 [23]	IP0 [22]	IP0 [21]	IP0 [20]	IP0 [19]	IP0 [18]	IP0 [17]	IP0 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP0 [15]	IP0 [14]	IP0 [13]	IP0 [12]	IP0 [11]	IP0 [10]	IP0 [9]	IP0 [8]	IP0 [7]	IP0 [6]	IP0 [5]	IP0 [4]	IP0 [3]	IP0 [2]	IP0 [1]	IP0 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP0[0]	D0	—	—	—	—	—	—
IP0[1]	D1	—	—	—	—	—	—
IP0[2]	D2	—	—	—	—	—	—
IP0[3]	D3	—	—	—	—	—	—
IP0[4]	D4	—	—	—	—	—	—
IP0[5]	D5	—	—	—	—	—	—
IP0[6]	D6	—	—	—	—	—	—
IP0[7]	D7	—	—	—	—	—	—
IP0[8]	D8	—	—	—	—	—	—
IP0[9]	D9	—	—	—	—	—	—
IP0[10]	D10	—	—	—	—	—	—
IP0[11]	D11	—	—	—	—	—	—
IP0[12]	D12	—	—	—	—	—	—
IP0[13]	D13	—	—	—	—	—	—
IP0[14]	D14	—	—	—	—	—	—
IP0[15]	D15	—	—	—	—	—	—
IP0[18:16]	A0	ATAWR0#_C	MSIOF0_SCK_B	I2C0_SCL_C	PWM2_B	—	—
IP0[20:19]	A1	MSIOF0_SYNC_B	—	—	—	—	—
IP0[22:21]	A2	MSIOF0_SS1_B	—	—	—	—	—
IP0[24:23]	A3	MSIOF0_SS2_B	—	—	—	—	—
IP0[26:25]	A4	MSIOF0_TXD_B	—	—	—	—	—
IP0[28:27]	A5	MSIOF0_RXD_B	—	—	—	—	—
IP0[30:29]	A6	MSIOF1_SCK	—	—	—	—	—

Legend: — Setting prohibited

5.3.11 Peripheral Function Select Register 1 (IPSR1)

Function: IPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP1 [31]	IP1 [30]	IP1 [29]	IP1 [28]	IP1 [27]	IP1 [26]	IP1 [25]	IP1 [24]	IP1 [23]	IP1 [22]	IP1 [21]	IP1 [20]	IP1 [19]	IP1 [18]	IP1 [17]	IP1 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP1 [15]	IP1 [14]	IP1 [13]	IP1 [12]	IP1 [11]	IP1 [10]	IP1 [9]	IP1 [8]	IP1 [7]	IP1 [6]	IP1 [5]	IP1 [4]	IP1 [3]	IP1 [2]	IP1 [1]	IP1 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP1[1:0]	A7	MSIOF1_SYNC	—	—	—	—	—	—
IP1[3:2]	A8	MSIOF1_SS1	I2C0_SCL	—	—	—	—	—
IP1[5:4]	A9	MSIOF1_SS2	I2C0_SDA	—	—	—	—	—
IP1[7:6]	A10	MSIOF1_TXD	—	MSIOF1_TXD_D	—	—	—	—
IP1[10:8]	A11	MSIOF1_RXD	I2C3_SCL_D	MSIOF1_RXD_D	—	—	—	—
IP1[13:11]	A12	—	I2C3_SDA_D	MSIOF1_SCK_D	—	—	—	—
IP1[16:14]	A13	ATAG0#_C	—	MSIOF1_SS1_D	—	—	—	—
IP1[19:17]	A14	ATADIR0#_C	—	—	MSIOF1_SYNC_D	—	—	—
IP1[22:20]	A15	—	—	—	—	—	—	—
IP1[25:23]	A16	DREQ2_B	—	—	SCIFA1_SCK_B	—	—	—
IP1[28:26]	A17	DACK2_B	—	I2C0_SDA_C	—	—	—	—
IP1[31:29]	A18	DREQ1	SCIFA1_RXD_C	—	SCIFB1_RXD_C	—	—	—

Legend: — Setting prohibited

5.3.12 Peripheral Function Select Register 2 (IPSR2)

Function: IPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP2 [29]	IP2 [28]	IP2 [27]	IP2 [26]	IP2 [25]	IP2 [24]	IP2 [23]	IP2 [22]	IP2 [21]	IP2 [20]	IP2 [19]	IP2 [18]	IP2 [17]	IP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP2 [15]	IP2 [14]	IP2 [13]	IP2 [12]	IP2 [11]	IP2 [10]	IP2 [9]	IP2 [8]	IP2 [7]	IP2 [6]	IP2 [5]	IP2 [4]	IP2 [3]	IP2 [2]	IP2 [1]	IP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP2[2:0]	A19	DACK1	SCIFA1_TXD_C	—	SCIFB1_TXD_C	—	SCIFB1_SCK_B	—	—
IP2[4:3]	A20	SPCLK	—	—	—	—	—	—	—
IP2[6:5]	A21	ATAWR0#_B	MOSI_IO0	—	—	—	—	—	—
IP2[9:7]	A22	MISO_IO1	—	TX0	SCIFA0_TXD	—	—	—	—
IP2[12:10]	A23	IO2	—	RX0	SCIFA0_RXD	—	—	—	—
IP2[15:13]	A24	DREQ2	IO3	TX1	SCIFA1_TXD	—	—	—	—
IP2[18:16]	A25	DACK2	SSL	DREQ1_C	RX1	SCIFA1_RXD	—	—	—
IP2[20:19]	CS0#	ATAG0#_B	I2C1_SCL	—	—	—	—	—	—
IP2[22:21]	CS1#/A26	ATADIR0#_B	I2C1_SDA	—	—	—	—	—	—
IP2[24:23]	EX_CS1#	MSIOF2_SCK	-	—	—	—	—	—	—
IP2[26:25]	EX_CS2#	ATAWR0#	MSIOF2_SYNC	—	—	—	—	—	—
IP2[29:27]	EX_CS3#	ATADIR0#	MSIOF2_TXD	ATAG0#	—	EX_WAIT1	—	—	—

Legend: — Setting prohibited

5.3.13 Peripheral Function Select Register 3 (IPSR3)

Function: IPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP3 [30]	IP3 [29]	IP3 [28]	IP3 [27]	IP3 [26]	IP3 [25]	IP3 [24]	IP3 [23]	IP3 [22]	IP3 [21]	IP3 [20]	IP3 [19]	IP3 [18]	IP3 [17]	IP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP3 [15]	IP3 [14]	IP3 [13]	IP3 [12]	IP3 [11]	IP3 [10]	IP3 [9]	IP3 [8]	IP3 [7]	IP3 [6]	IP3 [5]	IP3 [4]	IP3 [3]	IP3 [2]	IP3 [1]	IP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP3[2:0]	EX_CS4#	ATARD0#	MSIOF2_RXD	—	EX_WAIT2	—	—	—	—
IP3[5:3]	EX_CS5#	ATACS00#	MSIOF2_SS1	HRX1_B	SCIFB1_RXD_B	PWM1	TPU_TO1	—	—
IP3[8:6]	BS#	ATACS10#	MSIOF2_SS2	HTX1_B	SCIFB1_TXD_B	PWM2	TPU_TO2	—	—
IP3[11:9]	RD/WR#	HRX2_B\HRX2_D	—	SCIFB0_RXD_B	DREQ1_D	—	—	—	—
IP3[13:12]	WE0#	HCTS2#_B	SCIFB0_TXD_B	—	—	—	—	—	—
IP3[15:14]	WE1#	ATARD0#_B	HTX2_B	SCIFB0_RTS#_B	—	—	—	—	—
IP3[17:16]	EX_WAIT0	HRTS2#_B	SCIFB0_CTS#_B	—	—	—	—	—	—
IP3[19:18]	DREQ0	PWM3	TPU_TO3	—	—	—	—	—	—
IP3[21:20]	DACK0	DRACK0	—	—	—	—	—	—	—
IP3[24:22]	—	—	HSCK0_C	HSCK2_C	SCIFB0_SCK_B	SCIFB2_SCK_B	DREQ2_C	HTX2_D	-
IP3[27:25]	SSI_SCK0129	HRX0_C	HRX2_C	SCIFB0_RXD_C	SCIFB2_RXD_C	—	—	—	—
IP3[30:28]	SSI_WS0129	HTX0_C	HTX2_C	SCIFB0_TXD_C	SCIFB2_TXD_C	—	—	—	—

Legend: — Setting prohibited

5.3.14 Peripheral Function Select Register 4 (IPSR4)

Function: IPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP4 [30]	IP4 [29]	IP4 [28]	IP4 [27]	IP4 [26]	IP4 [25]	IP4 [24]	IP4 [23]	IP4 [22]	IP4 [21]	IP4 [20]	IP4 [19]	IP4 [18]	IP4 [17]	IP4 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP4 [15]	IP4 [14]	IP4 [13]	IP4 [12]	IP4 [11]	IP4 [10]	IP4 [9]	IP4 [8]	IP4 [7]	IP4 [6]	IP4 [5]	IP4 [4]	IP4 [3]	IP4 [2]	IP4 [1]	IP4 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP4[1:0]	SSI_SDATA0	I2C0_SCL_B	IIC0_SCL_B	MSIOF2_SCK_C	—	—	—	—
IP4[4:2]	SSI_SCK1	I2C0_SDA_B	IIC0_SDA_B	MSIOF2_SYNC_C	—	—	—	—
IP4[7:5]	SSI_WS1	I2C1_SCL_B	IIC1_SCL_B	MSIOF2_TXD_C	—	—	—	—
IP4[9:8]	SSI_SDATA1	I2C1_SDA_B	IIC1_SDA_B	MSIOF2_RXD_C	—	—	—	—
IP4[12:10]	SSI_SCK2	I2C2_SCL	—	—	HSCK1_E	—	—	—
IP4[15:13]	SSI_WS2	I2C2_SDA	—	RX2_E	—	HCTS1#_E	—	—
IP4[18:16]	SSI_SDATA2	—	TX2_E	HRTS1#_E	—	—	—	—
IP4[19]	SSI_SCK34	—	—	—	—	—	—	—
IP4[20]	SSI_WS34	—	—	—	—	—	—	—
IP4[21]	SSI_SDATA3	—	—	—	—	—	—	—
IP4[23:22]	SSI_SCK4	—	—	—	—	—	—	—
IP4[25:24]	SSI_WS4	—	—	—	—	—	—	—
IP4[27:26]	SSI_SDATA4	MSIOF2_SCK_D	—	—	—	—	—	—
IP4[30:28]	SSI_SCK5	MSIOF1_SCK_C	TS_SDATA0	—	MSIOF2_SYNC_D	VI1_R2_B	—	—

Legend: — Setting prohibited

5.3.15 Peripheral Function Select Register 5 (IPSR5)

Function: IPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP5 [31]	IP5 [30]	IP5 [29]	IP5 [28]	IP5 [27]	IP5 [26]	IP5 [25]	IP5 [24]	IP5 [23]	IP5 [22]	IP5 [21]	IP5 [20]	IP5 [19]	IP5 [18]	IP5 [17]	IP5 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP5 [15]	IP5 [14]	IP5 [13]	IP5 [12]	IP5 [11]	IP5 [10]	IP5 [9]	IP5 [8]	IP5 [7]	IP5 [6]	IP5 [5]	IP5 [4]	IP5 [3]	IP5 [2]	IP5 [1]	IP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP5[2:0]	SSI_WS5	MSIOF1_SYNC_C	TS_SCK0	—	MSIOF2_TXD_D	VI1_R3_B	—	—
IP5[5:3]	SSI_SDATA5	MSIOF1_TXD_C	TS_SDEN0	—	MSIOF2_SS1_D	VI1_R4_B	—	—
IP5[8:6]	SSI_SCK6	MSIOF1_RXD_C	TS_SPSYNC0	—	MSIOF2_RXD_D	VI1_R5_B	—	—
IP5[11:9]	SSI_WS6	—	MSIOF2_SS2_D	VI1_R6_B	—	—	—	—
IP5[14:12]	SSI_SDATA6	—	—	VI1_R7_B	—	—	—	—
IP5[16:15]	SSI_SCK78	—	—	—	—	—	—	—
IP5[19:17]	SSI_WS78	TX0_D	—	—	—	—	—	—
IP5[21:20]	SSI_SDATA7	RX0_D	—	—	—	—	—	—
IP5[23:22]	SSI_SDATA8	TX1_D	—	—	—	—	—	—
IP5[25:24]	SSI_SCK9	RX1_D	—	—	—	—	—	—
IP5[28:26]	SSI_WS9	TX3_D	CAN0_TX_D	—	—	—	—	—
IP5[31:29]	SSI_SDATA9	RX3_D	CAN0_RX_D	—	—	—	—	—

Legend: — Setting prohibited

5.3.16 Peripheral Function Select Register 6 (IPSR6)

Function: IPSR6 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP6 [29]	IP6 [28]	IP6 [27]	IP6 [26]	IP6 [25]	IP6 [24]	IP6 [23]	IP6 [22]	IP6 [21]	IP6 [20]	IP6 [19]	IP6 [18]	IP6 [17]	IP6 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP6 [15]	IP6 [14]	IP6 [13]	IP6 [12]	IP6 [11]	IP6 [10]	IP6 [9]	IP6 [8]	IP6 [7]	IP6 [6]	IP6 [5]	IP6 [4]	IP6 [3]	IP6 [2]	IP6 [1]	IP6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP6[2:0]	AUDIO_CLKB	—	MSIOF1_SCK_B	SCIF_CLK	DVC_MUTE	—	—	—
IP6[5:3]	AUDIO_CLKC	SCIFB0_SCK_C	MSIOF1_SYNC_B	RX2	SCIFA2_RXD	—	—	—
IP6[7:6]	AUDIO_CLKOUT	MSIOF1_SS1_B	TX2	SCIFA2_TXD	—	—	—	—
IP6[9:8]	IRQ0	SCIFB1_RXD_D	—	—	—	—	—	—
IP6[11:10]	IRQ1	SCIFB1_SCK_C	—	—	—	—	—	—
IP6[13:12]	IRQ2	SCIFB1_TXD_D	—	—	—	—	—	—
IP6[15:14]	IRQ3	I2C4_SCL_C	MSIOF2_TXD_E	—	—	—	—	—
IP6[18:16]	IRQ4	HRX1_C/HRX1_E	I2C4_SDA_C	MSIOF2_RXD_E	—	—	—	—
IP6[20:19]	IRQ5	HTX1_C/HTX1_E	I2C1_SCL_E	MSIOF2_SCK_E	—	—	—	—
IP6[23:21]	IRQ6	HSCK1_C	MSIOF1_SS2_B	I2C1_SDA_E	MSIOF2_SYNC_E	—	—	—
IP6[26:24]	IRQ7	HCTS1#_C	MSIOF1_TXD_B	—	—	—	—	—
IP6[29:27]	IRQ8	HRTS1#_C	MSIOF1_RXD_B	—	—	—	—	—

Legend: — Setting prohibited

5.3.17 Peripheral Function Select Register 7 (IPSR7)

Function: IPSR7 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP7 [29]	IP7 [28]	IP7 [27]	IP7 [26]	IP7 [25]	IP7 [24]	IP7 [23]	IP7 [22]	IP7 [21]	IP7 [20]	IP7 [19]	IP7 [18]	IP7 [17]	IP7 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP7 [15]	IP7 [14]	IP7 [13]	IP7 [12]	IP7 [11]	IP7 [10]	IP7 [9]	IP7 [8]	IP7 [7]	IP7 [6]	IP7 [5]	IP7 [4]	IP7 [3]	IP7 [2]	IP7 [1]	IP7 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP7[2:0]	IRQ9	DU1_DOTCLKIN_B	CAN_CLK_D	—	SCIF_CLK_B	—	—
IP7[5:3]	DU1_DR0	—	VI1_DATA0_B	TX0_B	SCIFA0_TXD_B	MSIOF2_SCK_B	—
IP7[8:6]	DU1_DR1	—	VI1_DATA1_B	RX0_B	SCIFA0_RXD_B	MSIOF2_SYNC_B	—
IP7[10:9]	DU1_DR2	—	SSI_SCK0129_B	—	—	—	—
IP7[12:11]	DU1_DR3	—	SSI_WS0129_B	—	—	—	—
IP7[14:13]	DU1_DR4	—	SSI_SDATA0_B	—	—	—	—
IP7[16:15]	DU1_DR5	—	SSI_SCK1_B	—	—	—	—
IP7[18:17]	DU1_DR6	—	SSI_WS1_B	—	—	—	—
IP7[20:19]	DU1_DR7	—	SSI_SDATA1_B	—	—	—	—
IP7[23:21]	DU1_DG0	—	VI1_DATA2_B	TX1_B	SCIFA1_TXD_B	MSIOF2_SS1_B	—
IP7[26:24]	DU1_DG1	—	VI1_DATA3_B	RX1_B	SCIFA1_RXD_B	MSIOF2_SS2_B	—
IP7[29:27]	DU1_DG2	—	VI1_DATA4_B	SCIF1_SCK_B	SCIFA1_SCK	SSI_SCK78_B	—

Legend: — Setting prohibited

5.3.18 Peripheral Function Select Register 8 (IPSR8)

Function: IPSR8 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP8 [30]	IP8 [29]	IP8 [28]	IP8 [27]	IP8 [26]	IP8 [25]	IP8 [24]	IP8 [23]	IP8 [22]	IP8 [21]	IP8 [20]	IP8 [19]	IP8 [18]	IP8 [17]	IP8 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP8 [15]	IP8 [14]	IP8 [13]	IP8 [12]	IP8 [11]	IP8 [10]	IP8 [9]	IP8 [8]	IP8 [7]	IP8 [6]	IP8 [5]	IP8 [4]	IP8 [3]	IP8 [2]	IP8 [1]	IP8 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP8[2:0]	DU1_DG3	—	VI1_DATA5_B	—	SSI_WS78_B	—	—
IP8[5:3]	DU1_DG4	—	VI1_DATA6_B	HRX0_B	SCIFB2_RXD_B	SSI_SDATA7_B	—
IP8[8:6]	DU1_DG5	—	VI1_DATA7_B	HCTS0#_B	SCIFB2_TXD_B	SSI_SDATA8_B	—
IP8[11:9]	DU1_DG6	—	HRTS0#_B	SCIFB2_CTS#_B	SSI_SCK9_B	—	—
IP8[14:12]	DU1_DG7	—	HTX0_B	SCIFB2_RTS#_B	SSI_WS9_B	—	—
IP8[17:15]	DU1_DB0	—	VI1_CLK_B	TX2_B	SCIFA2_TXD_B	MSIOF2_TXD_B	—
IP8[20:18]	DU1_DB1	—	VI1_HSYNC#_B	RX2_B	SCIFA2_RXD_B	MSIOF2_RXD_B	—
IP8[23:21]	DU1_DB2	—	VI1_VSYNC#_B	SCIF2_SCK_B	SCIFA2_SCK	SSI_SDATA9_B	—
IP8[25:24]	DU1_DB3	—	VI1_CLKENB_B	—	—	—	—
IP8[27:26]	DU1_DB4	—	VI1_FIELD_B	CAN1_RX	—	—	—
IP8[30:28]	DU1_DB5	—	TX3	SCIFA3_TXD	CAN1_TX	—	—

Legend: — Setting prohibited

5.3.19 Peripheral Function Select Register 9 (IPSR9)

Function: IPSR9 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP9 [31]	IP9 [30]	IP9 [29]	IP9 [28]	IP9 [27]	IP9 [26]	IP9 [25]	IP9 [24]	IP9 [23]	IP9 [22]	IP9 [21]	IP9 [20]	IP9 [19]	IP9 [18]	IP9 [17]	IP9 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP9 [15]	IP9 [14]	IP9 [13]	IP9 [12]	IP9 [11]	IP9 [10]	IP9 [9]	IP9 [8]	IP9 [7]	IP9 [6]	IP9 [5]	IP9 [4]	IP9 [3]	IP9 [2]	IP9 [1]	IP9 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP9[2:0]	DU1_DB6	—	I2C3_SCL_C	RX3	SCIFA3_RXD	—	—	—
IP9[5:3]	DU1_DB7	—	I2C3_SDA_C	SCIF3_SCK	SCIFA3_SCK	—	—	—
IP9[6]	DU1_DOTCLKIN	—	—	—	—	—	—	—
IP9[7]	DU1_DOTCLKOUT0	—	—	—	—	—	—	—
IP9[10:8]	DU1_DOTCLKOUT1	—	CAN0_TX	TX3_B	I2C2_SCL_B	PWM4	—	—
IP9[11]	DU1_EXHSYNC_DU1_HSYNC	—	—	—	—	—	—	—
IP9[12]	DU1_EXVSYNC_DU1_VSYNC	—	—	—	—	—	—	—
IP9[15:13]	DU1_EXODDF_DU1_ODDF_DISP_CDE	—	CAN0_RX	RX3_B	I2C2_SDA_B	—	—	—
IP9[16]	DU1_DISP	—	—	—	—	—	—	—
IP9[18:17]	DU1_CDE	—	PWM4_B	—	—	—	—	—
IP9[20:19]	VI0_CLKENB	TX4	SCIFA4_TXD	TS_SDATA0_D	—	—	—	—
IP9[22:21]	VI0_FIELD	RX4	SCIFA4_RXD	TS_SCK0_D	—	—	—	—
IP9[24:23]	VI0_HSYNC#	TX5	SCIFA5_TXD	TS_SDEN0_D	—	—	—	—
IP9[26:25]	VI0_VSYNC#	RX5	SCIFA5_RXD	TS_SPSYNC0_D	—	—	—	—
IP9[28:27]	VI0_DATA3_VI0_B3	SCIF3_SCK_B	SCIFA3_SCK_B	—	—	—	—	—
IP9[31:29]	VI0_G0	IIC1_SCL	—	I2C4_SCL	HCTS2#	SCIFB2_CTS#	ATAWR1#	—

Legend: — Setting prohibited

5.3.20 Peripheral Function Select Register 10 (IPSR10)

Function: IPSR10 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP10 [31]	IP10 [30]	IP10 [29]	IP10 [28]	IP10 [27]	IP10 [26]	IP10 [25]	IP10 [24]	IP10 [23]	IP10 [22]	IP10 [21]	IP10 [20]	IP10 [19]	IP10 [18]	IP10 [17]	IP10 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP10 [15]	IP10 [14]	IP10 [13]	IP10 [12]	IP10 [11]	IP10 [10]	IP10 [9]	IP10 [8]	IP10 [7]	IP10 [6]	IP10 [5]	IP10 [4]	IP10 [3]	IP10 [2]	IP10 [1]	IP10 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP10[2:0]	VI0_G1	IIC1_SDA	—	I2C4_SDA	HRTS2#	SCIFB2_RTS#	ATADIR1#	—
IP10[5:3]	VI0_G2	VI2_HSYNC#	—	I2C3_SCL_B	HSCK2	SCIFB2_SCK	ATARD1#	—
IP10[8:6]	VI0_G3	VI2_VSYNC#	—	I2C3_SDA_B	HRX2	SCIFB2_RXD	ATACS01#	—
IP10[11:9]	VI0_G4	VI2_CLKENB	—	HTX2	SCIFB2_TXD	SCIFB0_SCK_D	—	—
IP10[14:12]	VI0_G5	VI2_FIELD	—	—	CAN0_TX_E	HTX1_D	SCIFB0_TXD_D	—
IP10[16:15]	VI0_G6	VI2_CLK	—	—	—	—	—	—
IP10[18:17]	VI0_G7	VI2_DATA0	—	—	—	—	—	—
IP10[21:19]	VI0_R0	VI2_DATA1	—	TS_SDATA0_C	ATACS11#	—	—	—
IP10[24:22]	VI0_R1	VI2_DATA2	—	TS_SCK0_C	ATAG1#	—	—	—
IP10[26:25]	VI0_R2	VI2_DATA3	—	TS_SDEN0_C	—	—	—	—
IP10[28:27]	VI0_R3	VI2_DATA4	—	TS_SPSYNC0_C	—	—	—	—
IP10[31:29]	VI0_R4	VI2_DATA5	—	TX0_C	I2C1_SCL_D	—	—	—

Legend: — Setting prohibited

5.3.21 Peripheral Function Select Register 11 (IPSR11)

Function: IPSR11 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP11 [31]	IP11 [30]	IP11 [29]	IP11 [28]	IP11 [27]	IP11 [26]	IP11 [25]	IP11 [24]	IP11 [23]	IP11 [22]	IP11 [21]	IP11 [20]	IP11 [19]	IP11 [18]	IP11 [17]	IP11 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP11 [15]	IP11 [14]	IP11 [13]	IP11 [12]	IP11 [11]	IP11 [10]	IP11 [9]	IP11 [8]	IP11 [7]	IP11 [6]	IP11 [5]	IP11 [4]	IP11 [3]	IP11 [2]	IP11 [1]	IP11 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP11[2:0]	VI0_R5	VI2_DATA6	—	RX0_C	I2C1_SDA_D	—	—	—
IP11[5:3]	VI0_R6	VI2_DATA7	—	TX1_C	I2C4_SCL_B	—	—	—
IP11[8:6]	VI0_R7	—	RX1_C	CAN0_RX_E	I2C4_SDA_B	HRX1_D	SCIFB0_RXD_D	-
IP11[11:9]	VI1_HSYNC#	AVB_RXD0	TS_SDATA0_B	TX4_B	SCIFA4_TXD_B	—	—	—
IP11[14:12]	VI1_VSYNC#	AVB_RXD1	TS_SCK0_B	RX4_B	SCIFA4_RXD_B	—	—	—
IP11[16:15]	VI1_CLKENB	AVB_RXD2	TS_SDEN0_B	—	—	—	—	—
IP11[18:17]	VI1_FIELD	AVB_RXD3	TS_SPSYNC0_B	—	—	—	—	—
IP11[19]	VI1_CLK	AVB_RXD4	—	—	—	—	—	—
IP11[20]	VI1_DATA0	AVB_RXD5	—	—	—	—	—	—
IP11[21]	VI1_DATA1	AVB_RXD6	—	—	—	—	—	—
IP11[22]	VI1_DATA2	AVB_RXD7	—	—	—	—	—	—
IP11[23]	VI1_DATA3	AVB_RX_ER	—	—	—	—	—	—
IP11[24]	VI1_DATA4	AVB_MDIO	—	—	—	—	—	—
IP11[25]	VI1_DATA5	AVB_RX_DV	—	—	—	—	—	—
IP11[26]	VI1_DATA6	AVB_MAGIC	—	—	—	—	—	—
IP11[27]	VI1_DATA7	AVB_MDC	—	—	—	—	—	—
IP11[29:28]	ETH_MDIO	AVB_RX_CLK	I2C2_SCL_C	—	—	—	—	—
IP11[31:30]	ETH_CRS_DV	AVB_LINK	I2C2_SDA_C	—	—	—	—	—

Legend: — Setting prohibited

5.3.22 Peripheral Function Select Register 12 (IPSR12)

Function: IPSR12 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP12 [29]	IP12 [28]	IP12 [27]	IP12 [26]	IP12 [25]	IP12 [24]	IP12 [23]	IP12 [22]	IP12 [21]	IP12 [20]	IP12 [19]	IP12 [18]	IP12 [17]	IP12 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP12 [15]	IP12 [14]	IP12 [13]	IP12 [12]	IP12 [11]	IP12 [10]	IP12 [9]	IP12 [8]	IP12 [7]	IP12 [6]	IP12 [5]	IP12 [4]	IP12 [3]	IP12 [2]	IP12 [1]	IP12 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Others (Set Value = H'5 to H'F)
IP12[1:0]	ETH_RX_ER	AVB_CRS	I2C3_SCL	IIC0_SCL	—	—
IP12[3:2]	ETH_RXD0	AVB_PHY_INT	I2C3_SDA	IIC0_SDA	—	—
IP12[6:4]	ETH_RXD1	AVB_GTXREFCLK	CAN0_TX_C	I2C2_SCL_D	MSIOF1_RXD_E	—
IP12[9:7]	ETH_LINK	AVB_TXD0	CAN0_RX_C	I2C2_SDA_D	MSIOF1_SCK_E	—
IP12[12:10]	ETH_REFCLK	AVB_TXD1	SCIFA3_RXD_B	CAN1_RX_C	MSIOF1_SYNC_E	—
IP12[15:13]	ETH_TXD1	AVB_TXD2	SCIFA3_TXD_B	CAN1_TX_C	MSIOF1_TXD_E	—
IP12[17:16]	ETH_TX_EN	AVB_TXD3	TCLK1_B	CAN_CLK_B	—	—
IP12[19:18]	ETH_MAGIC	AVB_TXD4	—	—	—	—
IP12[21:20]	ETH_TXD0	AVB_TXD5	—	—	—	—
IP12[23:22]	ETH_MDC	AVB_TXD6	—	—	—	—
IP12[26:24]	—	AVB_TXD7	SCIFB2_TXD_D	—	MSIOF0_SYNC_C	—
IP12[29:27]	—	AVB_TX_EN	SCIFB2_RXD_D	—	MSIOF0_SCK_C	—

Legend: — Setting prohibited

5.3.23 Peripheral Function Select Register 13 (IPSR13)

Function: IPSR13 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	IP13 [30]	IP13 [29]	IP13 [28]	IP13 [27]	IP13 [26]	IP13 [25]	IP13 [24]	IP13 [23]	IP13 [22]	IP13 [21]	IP13 [20]	IP13 [19]	IP13 [18]	IP13 [17]	IP13 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP13 [15]	IP13 [14]	IP13 [13]	IP13 [12]	IP13 [11]	IP13 [10]	IP13 [9]	IP13 [8]	IP13 [7]	IP13 [6]	IP13 [5]	IP13 [4]	IP13 [3]	IP13 [2]	IP13 [1]	IP13 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP13[2:0]	—	AVB_TX_ER	SCIFB2_SCK_C	—	MSIOF0_SS1_C	—	—	—	—
IP13[4:3]	—	AVB_TX_CLK	—	MSIOF0_SS2_C	—	—	—	—	—
IP13[6:5]	—	AVB_COL	—	MSIOF0_RXD_C	—	—	—	—	—
IP13[9:7]	—	AVB_GTX_CLK	PWM0_B	—	MSIOF0_TXD_C	—	—	—	—
IP13[10]	SD0_CLK	SPCLK_B	—	—	—	—	—	—	—
IP13[11]	SD0_CMD	MOSI_IO0_B	—	—	—	—	—	—	—
IP13[12]	SD0_DATA0	MISO_IO1_B	—	—	—	—	—	—	—
IP13[13]	SD0_DATA1	IO2_B	—	—	—	—	—	—	—
IP13[14]	SD0_DATA2	IO3_B	—	—	—	—	—	—	—
IP13[15]	SD0_DATA3	SSL_B	—	—	—	—	—	—	—
IP13[18:16]	SD0_CD	MMC_D6_B	—	CAN0_RX_F	SCIFA5_TXD_B	TX3_C			—
IP13[21:19]	SD0_WP	MMC_D7_B	—	CAN0_TX_F	SCIFA5_RXD_B	RX3_C			—
IP13[22]	SD2_CMD	—	—	—	—	—	—	—	—
IP13[24:23]	SD2_DATA0	—	—	—	—	—	—	—	—
IP13[25]	SD2_DATA1	—	—	—	—	—	—	—	—
IP13[26]	SD2_DATA2	—	—	—	—	—	—	—	—
IP13[27]	SD2_DATA3	—	—	—	—	—	—	—	—
IP13[30:28]	SD2_CD	PWM0	TPU_TO0	I2C1_SCL_C		—	—	—	—

Legend: — Setting prohibited

5.3.24 Peripheral Function Select Register 14 (IPSR14)

Function: IPSR14 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP14 [31]	IP14 [30]	IP14 [29]	IP14 [28]	IP14 [27]	IP14 [26]	IP14 [25]	IP14 [24]	IP14 [23]	IP14 [22]	IP14 [21]	IP14 [20]	IP14 [19]	IP14 [18]	IP14 [17]	IP14 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP14 [15]	IP14 [14]	IP14 [13]	IP14 [12]	IP14 [11]	IP14 [10]	IP14 [9]	IP14 [8]	IP14 [7]	IP14 [6]	IP14 [5]	IP14 [4]	IP14 [3]	IP14 [2]	IP14 [1]	IP14 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP14[1:0]	SD2_WP	PWM1_B	I2C1_SDA_C	—	—	—	—	—
IP14[2]	SD3_CLK	MMC_CLK	—	—	—	—	—	—
IP14[3]	SD3_CMD	MMC_CMD	—	—	—	—	—	—
IP14[4]	SD3_DATA0	MMC_D0	—	—	—	—	—	—
IP14[5]	SD3_DATA1	MMC_D1	—	—	—	—	—	—
IP14[6]	SD3_DATA2	MMC_D2	—	—	—	—	—	—
IP14[7]	SD3_DATA3	MMC_D3	—	—	—	—	—	—
IP14[10:8]	SD3_CD	MMC_D4	IIC1_SCL_C	TX5_B	SCIFA5_TXD_C	—	—	—
IP14[13:11]	SD3_WP	MMC_D5	IIC1_SDA_C	RX5_B	SCIFA5_RXD_C	—	—	—
IP14[16:14]	MSIOF0_SCK	RX2_C	—	—	VI1_CLK_C	VI1_G0_B	—	—
IP14[19:17]	MSIOF0_SYNC	TX2_C	—	—	VI1_CLKENB_C	VI1_G1_B	—	—
IP14[22:20]	MSIOF0_TXD	—	—	VI1_FIELD_C	VI1_G2_B	—	—	—
IP14[25:23]	MSIOF0_RXD	—	—	VI1_DATA0_C	VI1_G3_B	—	—	—
IP14[28:26]	MSIOF0_SS1	MMC_D6	—	TX0_E	VI1_HSYNC#_C	IIC0_SCL_C	VI1_G4_B	—
IP14[31:29]	MSIOF0_SS2	MMC_D7	—	RX0_E	VI1_VSYNC#_C	IIC0_SDA_C	VI1_G5_B	—

Legend: — Setting prohibited

5.3.25 Peripheral Function Select Register 15 (IPSR15)

Function: IPSR15 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IP15 [29]	IP15 [28]	IP15 [27]	IP15 [26]	IP15 [25]	IP15 [24]	IP15 [23]	IP15 [22]	IP15 [21]	IP15 [20]	IP15 [19]	IP15 [18]	IP15 [17]	IP15 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP15 [15]	IP15 [14]	IP15 [13]	IP15 [12]	IP15 [11]	IP15 [10]	IP15 [9]	IP15 [8]	IP15 [7]	IP15 [6]	IP15 [5]	IP15 [4]	IP15 [3]	IP15 [2]	IP15 [1]	IP15 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP15[1:0]	—	—	CAN1_TX_D	—	—	—	—	—
IP15[3:2]	—	—	CAN_CLK_C	—	—	—	—	—
IP15[5:4]	—	—	CAN1_RX_D	—	—	—	—	—
IP15[8:6]	—	DU1_DOTCLKIN_C	AUDIO_CLKB_B	PWM5_B	SCIFA3_TXD_C	—	—	—
IP15[11:9]	—	TX4_C	SCIFA4_TXD_C	PWM5	VI1_G6_B	SCIFA3_RXD_C	—	—
IP15[14:12]	—	RX4_C	SCIFA4_RXD_C	PWM6	VI1_G7_B	SCIFA3_SCK_C	—	—
IP15[17:15]	HCTS0#	SCIFB0_CTS#	—	—	TCLK1	VI1_DATA1_C	—	—
IP15[20:18]	HRTS0#	SCIFB0_RTS#	—	—	VI1_DATA2_C	—	—	—
IP15[23:21]	HSCK0	SCIFB0_SCK	—	—	CAN_CLK	TCLK2	VI1_DATA3_C	—
IP15[26:24]	HRX0	SCIFB0_RXD	—	—	CAN0_RX_B	VI1_DATA4_C	—	—
IP15[29:27]	HTX0	SCIFB0_TXD	—	—	CAN0_TX_B	VI1_DATA5_C	—	—

Legend: — Setting prohibited

5.3.26 Peripheral Function Select Register 16 (IPSR16)

Function: IPSR16 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	IP16 [11]	IP16 [10]	IP16 [9]	IP16 [8]	IP16 [7]	IP16 [6]	IP16 [5]	IP16 [4]	IP16 [3]	IP16 [2]	IP16 [1]	IP16 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Others (Set Value = H'5 to H'F)
IP16[2:0]	HRX1	SCIFB1_RXD	VI1_R0_B	—	VI1_DATA6_C	—
IP16[5:3]	HTX1	SCIFB1_TXD	VI1_R1_B	—	VI1_DATA7_C	—
IP16[7:6]	HSCK1	SCIFB1_SCK	—	—	—	—
IP16[9:8]	HCTS1#	SCIFB1_CTS#	—	CAN1_TX_B	—	—
IP16[11:10]	HRTS1#	SCIFB1_RTS#	—	CAN1_RX_B	—	—

Legend: — Setting prohibited

Table 5.2 shows the correspondence between the function signals and the bit settings in the GPIO/peripheral function select registers and peripheral function selecting registers.

Table 5.2 Correspondence between Function Signals and Register Bit Settings

GPIO	Peripheral-Module-(GP-Set-Value-=-1)								GPIO/ Peripheral -Function- Selecting- Bit	Peripheral- Function- Selecting- Bit
	Function-Selected-by-IP-Bits									
(GP-Set-Value-=-0)	Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)		
GP-0-0	D0	—	—	—	—	—	—	—	GP0[0]	IP0[0]
GP-0-1	D1	—	—	—	—	—	—	—	GP0[1]	IP0[1]
GP-0-2	D2	—	—	—	—	—	—	—	GP0[2]	IP0[2]
GP-0-3	D3	—	—	—	—	—	—	—	GP0[3]	IP0[3]
GP-0-4	D4	—	—	—	—	—	—	—	GP0[4]	IP0[4]
GP-0-5	D5	—	—	—	—	—	—	—	GP0[5]	IP0[5]
GP-0-6	D6	—	—	—	—	—	—	—	GP0[6]	IP0[6]
GP-0-7	D7	—	—	—	—	—	—	—	GP0[7]	IP0[7]
GP-0-8	D8	—	—	—	—	—	—	—	GP0[8]	IP0[8]
GP-0-9	D9	—	—	—	—	—	—	—	GP0[9]	IP0[9]
GP-0-10	D10	—	—	—	—	—	—	—	GP0[10]	IP0[10]
GP-0-11	D11	—	—	—	—	—	—	—	GP0[11]	IP0[11]
GP-0-12	D12	—	—	—	—	—	—	—	GP0[12]	IP0[12]
GP-0-13	D13	—	—	—	—	—	—	—	GP0[13]	IP0[13]
GP-0-14	D14	—	—	—	—	—	—	—	GP0[14]	IP0[14]
GP-0-15	D15	—	—	—	—	—	—	—	GP0[15]	IP0[15]
GP-0-16	A0	ATAWR0#_C	MSIOF0_SCK_B	I2C0_SCL_C	PWM2_B	—	—	—	GP0[16]	IP0[18:16]
GP-0-17	A1	MSIOF0_SYNC_B	—	—	—	—	—	—	GP0[17]	IP0[20:19]
GP-0-18	A2	MSIOF0_SS1_B	—	—	—	—	—	—	GP0[18]	IP0[22:21]
GP-0-19	A3	MSIOF0_SS2_B	—	—	—	—	—	—	GP0[19]	IP0[24:23]
GP-0-20	A4	MSIOF0_TXD_B	—	—	—	—	—	—	GP0[20]	IP0[26:25]
GP-0-21	A5	MSIOF0_RXD_B	—	—	—	—	—	—	GP0[21]	IP0[28:27]
GP-0-22	A6	MSIOF1_SCK	—	—	—	—	—	—	GP0[22]	IP0[30:29]
GP-0-23	A7	MSIOF1_SYNC	—	—	—	—	—	—	GP0[23]	IP1[1:0]
GP-0-24	A8	MSIOF1_SS1	I2C0_SCL	—	—	—	—	—	GP0[24]	IP1[3:2]
GP-0-25	A9	MSIOF1_SS2	I2C0_SDA	—	—	—	—	—	GP0[25]	IP1[5:4]
GP-0-26	A10	MSIOF1_TXD	—	MSIOF1_TXD_D	—	—	—	—	GP0[26]	IP1[7:6]
GP-0-27	A11	MSIOF1_RXD	I2C3_SCL_D	MSIOF1_RXD_D	—	—	—	—	GP0[27]	IP1[10:8]
GP-0-28	A12	—	I2C3_SDA_D	MSIOF1_SCK_D	—	—	—	—	GP0[28]	IP1[13:11]
GP-0-29	A13	ATAG0#_C	—	MSIOF1_SS1_D	—	—	—	—	GP0[29]	IP1[16:14]
GP-0-30	A14	ATADIR0#_C	—	—	MSIOF1_SYNC_D	—	—	—	GP0[30]	IP1[19:17]
GP-0-31	A15	—	—	—	—	—	—	—	GP0[31]	IP1[22:20]
GP-1-0	A16	DREQ2_B	—	—	SCIFA1_SCK_B	—	—	—	GP1[0]	IP1[25:23]
GP-1-1	A17	DACK2_B	—	I2C0_SDA_C	—	—	—	—	GP1[1]	IP1[28:26]
GP-1-2	A18	DREQ1	SCIFA1_RXD_C	—	SCIFB1_RXD_C	—	—	—	GP1[2]	IP1[31:29]
GP-1-3	A19	DACK1	SCIFA1_TXD_C	—	SCIFB1_TXD_C	—	SCIFB1_SCK_B	—	GP1[3]	IP2[2:0]
GP-1-4	A20	SPCLK	—	—	—	—	—	—	GP1[4]	IP2[4:3]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP-1-5	A21	ATAWR0#_B	MOSI_IO0	—	—	—	—	—	GP1[5]	IP2[6:5]
GP-1-6	A22	MISO_IO1	—	TX0	SCIFA0_TXD	—	—	—	GP1[6]	IP2[9:7]
GP-1-7	A23	IO2	—	RX0	SCIFA0_RXD	—	—	—	GP1[7]	IP2[12:10]
GP-1-8	A24	DREQ2	IO3	TX1	SCIFA1_TXD	—	—	—	GP1[8]	IP2[15:13]
GP-1-9	A25	DACK2	SSL	DREQ1_C	RX1	SCIFA1_RXD	—	—	GP1[9]	IP2[18:16]
GP-1-10	CS0#	ATAG0#_B	I2C1_SCL	—	—	—	—	—	GP1[10]	IP2[20:19]
GP-1-11	CS1#/A26	ATADIR0#_B	I2C1_SDA	—	—	—	—	—	GP1[11]	IP2[22:21]
GP-1-12	EX_CS0#	—	—	—	—	—	—	—	GP1[12]	—
GP-1-13	EX_CS1#	MSIOF2_SCK	—	—	—	—	—	—	GP1[13]	IP2[24:23]
GP-1-14	EX_CS2#	ATAWR0#	MSIOF2_SYNC	—	—	—	—	—	GP1[14]	IP2[26:25]
GP-1-15	EX_CS3#	ATADIR0#	MSIOF2_TXD	ATAG0#	—	EX_WAIT1	—	—	GP1[15]	IP2[29:27]
GP-1-16	EX_CS4#	ATARD0#	MSIOF2_RXD	—	EX_WAIT2	—	—	—	GP1[16]	IP3[2:0]
GP-1-17	EX_CS5#	ATACS00#	MSIOF2_SS1	HRX1_B	SCIFB1_RXD_B	PWM1	TPU_TO1	—	GP1[17]	IP3[5:3]
GP-1-18	BS#	ATACS10#	MSIOF2_SS2	HTX1_B	SCIFB1_TXD_B	PWM2	TPU_TO2	—	GP1[18]	IP3[8:6]
GP-1-19	RD#	—	—	—	—	—	—	—	GP1[19]	—
GP-1-20	RD/WR#	HRX2_B\HRX2_D	—	SCIFB0_RXD_B	DREQ1_D	—	—	—	GP1[20]	IP3[11:9]
GP-1-21	WE0#	HCTS2#_B	SCIFB0_TXD_B	—	—	—	—	—	GP1[21]	IP3[13:12]
GP-1-22	WE1#	ATARD0#_B	HTX2_B	SCIFB0_RTS#_B	—	—	—	—	GP1[22]	IP3[15:14]
GP-1-23	EX_WAIT0	HRTS2#_B	SCIFB0_CTS#_B	—	—	—	—	—	GP1[23]	IP3[17:16]
GP-1-24	DREQ0	PWM3	TPU_TO3	—	—	—	—	—	GP1[24]	IP3[19:18]
GP-1-25	DACK0	DRACK0	—	—	—	—	—	—	GP1[25]	IP3[21:20]
GP-2-0	SSI_SCK0129	HRX0_C	HRX2_C	SCIFB0_RXD_C	SCIFB2_RXD_C	—	—	—	GP2[0]	IP3[27:25]
GP-2-1	SSI_WS0129	HTX0_C	HTX2_C	SCIFB0_TXD_C	SCIFB2_TXD_C	—	—	—	GP2[1]	IP3[30:28]
GP-2-2	SSI_SDATA0	I2C0_SCL_B	IIC0_SCL_B	MSIOF2_SCK_C	—	—	—	—	GP2[2]	IP4[1:0]
GP-2-3	SSI_SCK1	I2C0_SDA_B	IIC0_SDA_B	MSIOF2_SYNC_C	—	—	—	—	GP2[3]	IP4[4:2]
GP-2-4	SSI_WS1	I2C1_SCL_B	IIC1_SCL_B	MSIOF2_TXD_C	—	—	—	—	GP2[4]	IP4[7:5]
GP-2-5	SSI_SDATA1	I2C1_SDA_B	IIC1_SDA_B	MSIOF2_RXD_C	—	—	—	—	GP2[5]	IP4[9:8]
GP-2-6	SSI_SCK2	I2C2_SCL	—	—	HSCK1_E	—	—	—	GP2[6]	IP4[12:10]
GP-2-7	SSI_WS2	I2C2_SDA	—	RX2_E	—	HCTS1#_E	—	—	GP2[7]	IP4[15:13]
GP-2-8	SSI_SDATA2	—	TX2_E	HRTS1#_E	—	—	—	—	GP2[8]	IP4[18:16]
GP-2-9	SSI_SCK34	—	—	—	—	—	—	—	GP2[9]	IP4[19]
GP-2-10	SSI_WS34	—	—	—	—	—	—	—	GP2[10]	IP4[20]
GP-2-11	SSI_SDATA3	—	—	—	—	—	—	—	GP2[11]	IP4[21]
GP-2-12	SSI_SCK4	—	—	—	—	—	—	—	GP2[12]	IP4[23:22]
GP-2-13	SSI_WS4	—	—	—	—	—	—	—	GP2[13]	IP4[25:24]
GP-2-14	SSI_SDATA4	MSIOF2_SCK_D	—	—	—	—	—	—	GP2[14]	IP4[27:26]
GP-2-15	SSI_SCK5	MSIOF1_SCK_C	TS_SDATA0	—	MSIOF2_SYNC_D	VI1_R2_B	—	—	GP2[15]	IP4[30:28]
GP-2-16	SSI_WS5	MSIOF1_SYNC_C	TS_SCK0	—	MSIOF2_TXD_D	VI1_R3_B	—	—	GP2[16]	IP5[2:0]
GP-2-17	SSI_SDATA5	MSIOF1_TXD_C	TS_SDEN0	—	MSIOF2_SS1_D	VI1_R4_B	—	—	GP2[17]	IP5[5:3]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP-2-18	SSI_SCK6	MSIOF1_RXD_C	TS_SPSYNC0	—	MSIOF2_RXD_D	VI1_R5_B	—	—	GP2[18]	IP5[8:6]
GP-2-19	SSI_WS6	—	MSIOF2_SS2_D	VI1_R6_B	—	—	—	—	GP2[19]	IP5[11:9]
GP-2-20	SSI_SDATA6	—	—	VI1_R7_B	—	—	—	—	GP2[20]	IP5[14:12]
GP-2-21	SSI_SCK78	—	—	—	—	—	—	—	GP2[21]	IP5[16:15]
GP-2-22	SSI_WS78	TX0_D	—	—	—	—	—	—	GP2[22]	IP5[19:17]
GP-2-23	SSI_SDATA7	RX0_D	—	—	—	—	—	—	GP2[23]	IP5[21:20]
GP-2-24	SSI_SDATA8	TX1_D	—	—	—	—	—	—	GP2[24]	IP5[23:22]
GP-2-25	SSI_SCK9	RX1_D	—	—	—	—	—	—	GP2[25]	IP5[25:24]
GP-2-26	SSI_WS9	TX3_D	CAN0_TX_D	—	—	—	—	—	GP2[26]	IP5[28:26]
GP-2-27	SSI_SDATA9	RX3_D	CAN0_RX_D	—	—	—	—	—	GP2[27]	IP5[31:29]
GP-2-28	AUDIO_CLKA	—	—	—	—	—	—	—	GP2[28]	-
GP-2-29	AUDIO_CLKB	—	MSIOF1_SCK_B	SCIF_CLK	—	—	—	—	GP2[29]	IP6[2:0]
GP-2-30	AUDIO_CLKC	SCIFB0_SCK_C	MSIOF1_SYNC_B	RX2	SCIFA2_RXD	—	—	—	GP2[30]	IP6[5:3]
GP-2-31	AUDIO_CLKOUT	MSIOF1_SS1_B	TX2	SCIFA2_TXD	—	—	—	—	GP2[31]	IP6[7:6]
GP-3-0	DU1_DR0	—	VI1_DATA0_B	TX0_B	SCIFA0_TXD_B	MSIOF2_SCK_B	—	—	GP3[0]	IP7[5:3]
GP-3-1	DU1_DR1	—	VI1_DATA1_B	RX0_B	SCIFA0_RXD_B	MSIOF2_SYNC_B	—	—	GP3[1]	IP7[8:6]
GP-3-2	DU1_DR2	—	SSI_SCK0129_B	—	—	—	—	—	GP3[2]	IP7[10:9]
GP-3-3	DU1_DR3	—	SSI_WS0129_B	—	—	—	—	—	GP3[3]	IP7[12:11]
GP-3-4	DU1_DR4	—	SSI_SDATA0_B	—	—	—	—	—	GP3[4]	IP7[14:13]
GP-3-5	DU1_DR5	—	SSI_SCK1_B	—	—	—	—	—	GP3[5]	IP7[16:15]
GP-3-6	DU1_DR6	—	SSI_WS1_B	—	—	—	—	—	GP3[6]	IP7[18:17]
GP-3-7	DU1_DR7	—	SSI_SDATA1_B	—	—	—	—	—	GP3[7]	IP7[20:19]
GP-3-8	DU1_DG0	—	VI1_DATA2_B	TX1_B	SCIFA1_TXD_B	MSIOF2_SS1_B	—	—	GP3[8]	IP7[23:21]
GP-3-9	DU1_DG1	—	VI1_DATA3_B	RX1_B	SCIFA1_RXD_B	MSIOF2_SS2_B	—	—	GP3[9]	IP7[26:24]
GP-3-10	DU1_DG2	—	VI1_DATA4_B	SCIF1_SCK_B	SCIFA1_SCK	SSI_SCK78_B	—	—	GP3[10]	IP7[29:27]
GP-3-11	DU1_DG3	—	VI1_DATA5_B	—	SSI_WS78_B	—	—	—	GP3[11]	IP8[2:0]
GP-3-12	DU1_DG4	—	VI1_DATA6_B	HRX0_B	SCIFB2_RXD_B	SSI_SDATA7_B	—	—	GP3[12]	IP8[5:3]
GP-3-13	DU1_DG5	—	VI1_DATA7_B	HCTS0#_B	SCIFB2_TXD_B	SSI_SDATA8_B	—	—	GP3[13]	IP8[8:6]
GP-3-14	DU1_DG6	—	HRTS0#_B	SCIFB2_CTS#_B	SSI_SCK9_B	—	—	—	GP3[14]	IP8[11:9]
GP-3-15	DU1_DG7	—	HTX0_B	SCIFB2_RTS#_B	SSI_WS9_B	—	—	—	GP3[15]	IP8[14:12]
GP-3-16	DU1_DB0	—	VI1_CLK_B	TX2_B	SCIFA2_TXD_B	MSIOF2_TXD_B	—	—	GP3[16]	IP8[17:15]
GP-3-17	DU1_DB1	—	VI1_HSYNC#_B	RX2_B	SCIFA2_RXD_B	MSIOF2_RXD_B	—	—	GP3[17]	IP8[20:18]
GP-3-18	DU1_DB2	—	VI1_VSYNC#_B	SCIF2_SCK_B	SCIFA2_SCK	SSI_SDATA9_B	—	—	GP3[18]	IP8[23:21]
GP-3-19	DU1_DB3	—	VI1_CLKENB_B	—	—	—	—	—	GP3[19]	IP8[25:24]
GP-3-20	DU1_DB4	—	VI1_FIELD_B	CAN1_RX	—	—	—	—	GP3[20]	IP8[27:26]
GP-3-21	DU1_DB5	—	TX3	SCIFA3_TXD	CAN1_TX	—	—	—	GP3[21]	IP8[30:28]
GP-3-22	DU1_DB6	—	I2C3_SCL_C	RX3	SCIFA3_RXD	—	—	—	GP3[22]	IP9[2:0]
GP-3-23	DU1_DB7	—	I2C3_SDA_C	SCIF3_SCK	SCIFA3_SCK	—	—	—	GP3[23]	IP9[5:3]
GP-3-24	DU1_DOTCLKIN	—	—	—	—	—	—	—	GP3[24]	IP9[6]
GP-3-25	DU1_DOTCLKOUT0	—	—	—	—	—	—	—	GP3[25]	IP9[7]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP-3-26	DU1_DOTCLKOUT1	—	CAN0_TX	TX3_B	I2C2_SCL_B	PWM4	—	—	GP3[26]	IP9[10:8]
GP-3-27	DU1_EXHSYNC_DU1_HSYNC	—	—	—	—	—	—	—	GP3[27]	IP9[11]
GP-3-28	DU1_EXVSYNC_DU1_VSYNC	—	—	—	—	—	—	—	GP3[28]	IP9[12]
GP-3-29	DU1_EXODDF_DU1_ODDF_DISP_CDE	—	CAN0_RX	RX3_B	I2C2_SDA_B	—	—	—	GP3[29]	IP9[15:13]
GP-3-30	DU1_DISP	—	—	—	—	—	—	—	GP3[30]	IP9[16]
GP-3-31	DU1_CDE	—	PWM4_B	—	—	—	—	—	GP3[31]	IP9[18:17]
GP-4-0	VI0_CLK	—	—	—	—	—	—	—	GP4[0]	—
GP-4-1	VI0_CLKENB	TX4	SCIFA4_TXD	TS_SDATA0_D	—	—	—	—	GP4[1]	IP9[20:19]
GP-4-2	VI0_FIELD	RX4	SCIFA4_RXD	TS_SCK0_D	—	—	—	—	GP4[2]	IP9[22:21]
GP-4-3	VI0_HSYNC#	TX5	SCIFA5_TXD	TS_SDEN0_D	—	—	—	—	GP4[3]	IP9[24:23]
GP-4-4	VI0_VSYNC#	RX5	SCIFA5_RXD	TS_SPSYNC0_D	—	—	—	—	GP4[4]	IP9[26:25]
GP-4-5	VI0_DATA0_VI0_B0	—	—	—	—	—	—	—	GP4[5]	—
GP-4-6	VI0_DATA1_VI0_B1	—	—	—	—	—	—	—	GP4[6]	—
GP-4-7	VI0_DATA2_VI0_B2	—	—	—	—	—	—	—	GP4[7]	—
GP-4-8	VI0_DATA3_VI0_B3	SCIF3_SCK_B	SCIFA3_SCK_B	—	—	—	—	—	GP4[8]	IP9[28:27]
GP-4-9	VI0_DATA4_VI0_B4	—	—	—	—	—	—	—	GP4[9]	—
GP-4-10	VI0_DATA5_VI0_B5	—	—	—	—	—	—	—	GP4[10]	—
GP-4-11	VI0_DATA6_VI0_B6	—	—	—	—	—	—	—	GP4[11]	—
GP-4-12	VI0_DATA7_VI0_B7	—	—	—	—	—	—	—	GP4[12]	—
GP-4-13	VI0_G0	IIC1_SCL	—	I2C4_SCL	HCTS2#	SCIFB2_CTS#	ATAWR1#	—	GP4[13]	IP9[31:29]
GP-4-14	VI0_G1	IIC1_SDA	—	I2C4_SDA	HRTS2#	SCIFB2_RTS#	ATADIR1#	—	GP4[14]	IP10[2:0]
GP-4-15	VI0_G2	VI2_HSYNC#	—	I2C3_SCL_B	HSCK2	SCIFB2_SCK	ATARD1#	—	GP4[15]	IP10[5:3]
GP-4-16	VI0_G3	VI2_VSYNC#	—	I2C3_SDA_B	HRX2	SCIFB2_RXD	ATACS01#	—	GP4[16]	IP10[8:6]
GP-4-17	VI0_G4	VI2_CLKENB	—	HTX2	SCIFB2_TXD	SCIFB0_SCK_D	—	—	GP4[17]	IP10[11:9]
GP-4-18	VI0_G5	VI2_FIELD	—	—	CAN0_TX_E	HTX1_D	SCIFB0_TXD_D	—	GP4[18]	IP10[14:12]
GP-4-19	VI0_G6	VI2_CLK	—	—	—	—	—	—	GP4[19]	IP10[16:15]
GP-4-20	VI0_G7	VI2_DATA0	—	—	—	—	—	—	GP4[20]	IP10[18:17]
GP-4-21	VI0_R0	VI2_DATA1	—	TS_SDATA0_C	ATACS11#	—	—	—	GP4[21]	IP10[21:19]
GP-4-22	VI0_R1	VI2_DATA2	—	TS_SCK0_C	ATAG1#	—	—	—	GP4[22]	IP10[24:22]
GP-4-23	VI0_R2	VI2_DATA3	—	TS_SDEN0_C	—	—	—	—	GP4[23]	IP10[26:25]
GP-4-24	VI0_R3	VI2_DATA4	—	TS_SPSYNC0_C	—	—	—	—	GP4[24]	IP10[28:27]
GP-4-25	VI0_R4	VI2_DATA5	—	TX0_C	I2C1_SCL_D	—	—	—	GP4[25]	IP10[31:29]
GP-4-26	VI0_R5	VI2_DATA6	—	RX0_C	I2C1_SDA_D	—	—	—	GP4[26]	IP11[2:0]
GP-4-27	VI0_R6	VI2_DATA7	—	TX1_C	I2C4_SCL_B	—	—	—	GP4[27]	IP11[5:3]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function- Selecting- Bit	Peripheral- Function- Selecting- Bit
GP-4-28	VI0_R7	—	RX1_C	CAN0_RX_E	I2C4_SDA_B	HRX1_D	SCIFB0_RXD_D	—	GP4[28]	IP11[8:6]
GP-4-29	—	—	CAN1_TX_D	—	—	—	—	—	GP4[29]	IP15[1:0]
GP-4-30	—	—	CAN_CLK_C	—	—	—	—	—	GP4[30]	IP15[3:2]
GP-4-31	—	—	CAN1_RX_D	—	—	—	—	—	GP4[31]	IP15[5:4]
GP-5-0	VI1_HSYNC#	AVB_RXD0	TS_SDATA0_B	TX4_B	SCIFA4_TXD_B	—	—	—	GP5[0]	IP11[11:9]
GP-5-1	VI1_VSYNC#	AVB_RXD1	TS_SCK0_B	RX4_B	SCIFA4_RXD_B	—	—	—	GP5[1]	IP11[14:12]
GP-5-2	VI1_CLKENB	AVB_RXD2	TS_SDEN0_B	—	—	—	—	—	GP5[2]	IP11[16:15]
GP-5-3	VI1_FIELD	AVB_RXD3	TS_SPSYNC0_B	—	—	—	—	—	GP5[3]	IP11[18:17]
GP-5-4	VI1_CLK	AVB_RXD4	—	—	—	—	—	—	GP5[4]	IP11[19]
GP-5-5	VI1_DATA0	AVB_RXD5	—	—	—	—	—	—	GP5[5]	IP11[20]
GP-5-6	VI1_DATA1	AVB_RXD6	—	—	—	—	—	—	GP5[6]	IP11[21]
GP-5-7	VI1_DATA2	AVB_RXD7	—	—	—	—	—	—	GP5[7]	IP11[22]
GP-5-8	VI1_DATA3	AVB_RX_ER	—	—	—	—	—	—	GP5[8]	IP11[23]
GP-5-9	VI1_DATA4	AVB_MDIO	—	—	—	—	—	—	GP5[9]	IP11[24]
GP-5-10	VI1_DATA5	AVB_RX_DV	—	—	—	—	—	—	GP5[10]	IP11[25]
GP-5-11	VI1_DATA6	AVB_MAGIC	—	—	—	—	—	—	GP5[11]	IP11[26]
GP-5-12	VI1_DATA7	AVB_MDC	—	—	—	—	—	—	GP5[12]	IP11[27]
GP-5-13	ETH_MDIO	AVB_RX_CLK	I2C2_SCL_C	—	—	—	—	—	GP5[13]	IP11[29:28]
GP-5-14	ETH_CRS_DV	AVB_LINK	I2C2_SDA_C	—	—	—	—	—	GP5[14]	IP11[31:30]
GP-5-15	ETH_RX_ER	AVB_CRS	I2C3_SCL	IIC0_SCL	—	—	—	—	GP5[15]	IP12[1:0]
GP-5-16	ETH_RXD0	AVB_PHY_INT	I2C3_SDA	IIC0_SDA	—	—	—	—	GP5[16]	IP12[3:2]
GP-5-17	ETH_RXD1	AVB_GTXREFCLK	CAN0_TX_C	I2C2_SCL_D	MSIOF1_RXD_E	—	—	—	GP5[17]	IP12[6:4]
GP-5-18	ETH_LINK	AVB_TXD0	CAN0_RX_C	I2C2_SDA_D	MSIOF1_SCK_E	—	—	—	GP5[18]	IP12[9:7]
GP-5-19	ETH_REFCLK	AVB_TXD1	SCIFA3_RXD_B	CAN1_RX_C	MSIOF1_SYNC_E	—	—	—	GP5[19]	IP12[12:10]
GP-5-20	ETH_TXD1	AVB_TXD2	SCIFA3_TXD_B	CAN1_TX_C	MSIOF1_TXD_E	—	—	—	GP5[20]	IP12[15:13]
GP-5-21	ETH_TX_EN	AVB_TXD3	TCLK1_B	CAN_CLK_B	—	—	—	—	GP5[21]	IP12[17:16]
GP-5-22	ETH_MAGIC	AVB_TXD4	—	—	—	—	—	—	GP5[22]	IP12[19:18]
GP-5-23	ETH_TXD0	AVB_TXD5	—	—	—	—	—	—	GP5[23]	IP12[21:20]
GP-5-24	ETH_MDC	AVB_TXD6	—	—	—	—	—	—	GP5[24]	IP12[23:22]
GP-5-25	—	AVB_TXD7	SCIFB2_TXD_D	—	MSIOF0_SYNC_C	—	—	—	GP5[25]	IP12[26:24]
GP-5-26	—	AVB_TX_EN	SCIFB2_RXD_D	—	MSIOF0_SCK_C	—	—	—	GP5[26]	IP12[29:27]
GP-5-27	—	AVB_TX_ER	SCIFB2_SCK_C	—	MSIOF0_SS1_C	—	—	—	GP5[27]	IP13[2:0]
GP-5-28	—	AVB_TX_CLK	—	MSIOF0_SS2_C	—	—	—	—	GP5[28]	IP13[4:3]
GP-5-29	—	AVB_COL	—	MSIOF0_RXD_C	—	—	—	—	GP5[29]	IP13[6:5]
GP-5-30	—	AVB_GTX_CLK	PWM0_B	—	MSIOF0_TXD_C	—	—	—	GP5[30]	IP13[9:7]
GP-5-31	—	—	HSCK0_C	HSCK2_C	SCIFB0_SCK_B	SCIFB2_SCK_B	DREQ2_C	HTX2_D	GP5[31]	IP3[24:22]
GP-6-0	SD0_CLK	SPCLK_B	—	—	—	—	—	—	GP6[0]	IP13[10]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP-6-1	SD0_CMD	MOSI_IO0_B	—	—	—	—	—	—	GP6[1]	IP13[11]
GP-6-2	SD0_DATA0	MISO_IO1_B	—	—	—	—	—	—	GP6[2]	IP13[12]
GP-6-3	SD0_DATA1	IO2_B	—	—	—	—	—	—	GP6[3]	IP13[13]
GP-6-4	SD0_DATA2	IO3_B	—	—	—	—	—	—	GP6[4]	IP13[14]
GP-6-5	SD0_DATA3	SSL_B	—	—	—	—	—	—	GP6[5]	IP13[15]
GP-6-6	SD0_CD	MMC_D6_B	—	CAN0_RX_F	SCIFA5_TXD_B	TX3_C	—	—	GP6[6]	IP13[18:16]
GP-6-7	SD0_WP	MMC_D7_B	—	CAN0_TX_F	SCIFA5_RXD_B	RX3_C	—	—	GP6[7]	IP13[21:19]
GP-6-8	SD2_CLK	—	—	—	—	—	—	—	GP6[8]	-
GP-6-9	SD2_CMD	—	—	—	—	—	—	—	GP6[9]	IP13[22]
GP-6-10	SD2_DATA0	—	—	—	—	—	—	—	GP6[10]	IP13[24:23]
GP-6-11	SD2_DATA1	—	—	—	—	—	—	—	GP6[11]	IP13[25]
GP-6-12	SD2_DATA2	—	—	—	—	—	—	—	GP6[12]	IP13[26]
GP-6-13	SD2_DATA3	—	—	—	—	—	—	—	GP6[13]	IP13[27]
GP-6-14	SD2_CD	PWM0	TPU_TO0	I2C1_SCL_C	—	—	—	—	GP6[14]	IP13[30:28]
GP-6-15	SD2_WP	PWM1_B	I2C1_SDA_C	—	—	—	—	—	GP6[15]	IP14[1:0]
GP-6-16	SD3_CLK	MMC_CLK	—	—	—	—	—	—	GP6[16]	IP14[2]
GP-6-17	SD3_CMD	MMC_CMD	—	—	—	—	—	—	GP6[17]	IP14[3]
GP-6-18	SD3_DATA0	MMC_D0	—	—	—	—	—	—	GP6[18]	IP14[4]
GP-6-19	SD3_DATA1	MMC_D1	—	—	—	—	—	—	GP6[19]	IP14[5]
GP-6-20	SD3_DATA2	MMC_D2	—	—	—	—	—	—	GP6[20]	IP14[6]
GP-6-21	SD3_DATA3	MMC_D3	—	—	—	—	—	—	GP6[21]	IP14[7]
GP-6-22	SD3_CD	MMC_D4	IIC1_SCL_C	TX5_B	SCIFA5_TXD_C	—	—	—	GP6[22]	IP14[10:8]
GP-6-23	SD3_WP	MMC_D5	IIC1_SDA_C	RX5_B	SCIFA5_RXD_C	—	—	—	GP6[23]	IP14[13:11]
GP-6-24	MSIOF0_SCK	RX2_C	—	—	VI1_CLK_C	VI1_G0_B	—	—	GP6[24]	IP14[16:14]
GP-6-25	MSIOF0_SYNC	TX2_C	—	—	VI1_CLKENB_C	VI1_G1_B	—	—	GP6[25]	IP14[19:17]
GP-6-26	MSIOF0_TXD	—	—	VI1_FIELD_C	VI1_G2_B	—	—	—	GP6[26]	IP14[22:20]
GP-6-27	MSIOF0_RXD	—	—	VI1_DATA0_C	VI1_G3_B	—	—	—	GP6[27]	IP14[25:23]
GP-6-28	MSIOF0_SS1	MMC_D6	—	TX0_E	VI1_HSYNC#_C	IIC0_SCL_C	VI1_G4_B	—	GP6[28]	IP14[28:26]
GP-6-29	MSIOF0_SS2	MMC_D7	—	RX0_E	VI1_VSYNC#_C	IIC0_SDA_C	VI1_G5_B	—	GP6[29]	IP14[31:29]
GP-6-30	USB1_OVC	—	—	—	—	—	—	—	GP6[30]	—
GP-6-31	DU0_DOTCLKIN	—	—	—	—	—	—	—	GP6[31]	—
GP-7-0	HCTS0#	SCIFB0_CTS#	—	—	TCLK1	VI1_DATA1_C	—	—	GP7[0]	IP15[17:15]
GP-7-1	HRTS0#	SCIFB0_RTS#	—	—	VI1_DATA2_C	—	—	—	GP7[1]	IP15[20:18]
GP-7-2	HSCK0	SCIFB0_SCK	—	—	CAN_CLK	TCLK2	VI1_DATA3_C	—	GP7[2]	IP15[23:21]
GP-7-3	HRX0	SCIFB0_RXD	—	—	CAN0_RX_B	VI1_DATA4_C	—	—	GP7[3]	IP15[26:24]
GP-7-4	HTX0	SCIFB0_TXD	—	—	CAN0_TX_B	VI1_DATA5_C	—	—	GP7[4]	IP15[29:27]
GP-7-5	HRX1	SCIFB1_RXD	VI1_R0_B	—	VI1_DATA6_C	—	—	—	GP7[5]	IP16[2:0]
GP-7-6	HTX1	SCIFB1_TXD	VI1_R1_B	—	VI1_DATA7_C	—	—	—	GP7[6]	IP16[5:3]
GP-7-7	HSCK1	SCIFB1_SCK	—	—	—	—	—	—	GP7[7]	IP16[7:6]
GP-7-8	HCTS1#	SCIFB1_CTS#	—	CAN1_TX_B	—	—	—	—	GP7[8]	IP16[9:8]
GP-7-9	HRTS1#	SCIFB1_RTS#	—	CAN1_RX_B	—	—	—	—	GP7[9]	IP16[11:10]
GP-7-10	IRQ0	SCIFB1_RXD_D	—	—	—	—	—	—	GP7[10]	IP6[9:8]
GP-7-11	IRQ1	SCIFB1_SCK_C	—	—	—	—	—	—	GP7[11]	IP6[11:10]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP-7-12	IRQ2	SCIFB1_TXD_D	—	—	—	—	—	—	GP7[12]	IP6[13:12]
GP-7-13	IRQ3	I2C4_SCL_C	MSIOF2_TXD_E	—	—	—	—	—	GP7[13]	IP6[15:14]
GP-7-14	IRQ4	HRX1_C\HRX1_E	I2C4_SDA_C	MSIOF2_RXD_E	—	—	—	—	GP7[14]	IP6[18:16]
GP-7-15	IRQ5	HTX1_C\HTX1_E	I2C1_SCL_E	MSIOF2_SCK_E	—	—	—	—	GP7[15]	IP6[20:19]
GP-7-16	IRQ6	HSCK1_C	MSIOF1_SS2_B	I2C1_SDA_E	MSIOF2_SYNC_E	—	—	—	GP7[16]	IP6[23:21]
GP-7-17	IRQ7	HCTS1#_C	MSIOF1_TXD_B	—	—	—	—	—	GP7[17]	IP6[26:24]
GP-7-18	IRQ8	HRTS1#_C	MSIOF1_RXD_B	—	—	—	—	—	GP7[18]	IP6[29:27]
GP-7-19	IRQ9	DU1_DOTCLKIN_B	CAN_CLK_D	—	SCIF_CLK_B	—	—	—	GP7[19]	IP7[2:0]
GP-7-20	—	DU1_DOTCLKIN_C	AUDIO_CLKB_B	PWM5_B	SCIFA3_TXD_C	—	—	—	GP7[20]	IP15[8:6]
GP-7-21	—	TX4_C	SCIFA4_TXD_C	PWM5	VI1_G6_B	SCIFA3_RXD_C	—	—	GP7[21]	IP15[11:9]
GP-7-22	—	RX4_C	SCIFA4_RXD_C	PWM6	VI1_G7_B	SCIFA3_SCK_C	—	—	GP7[22]	IP15[14:12]
GP-7-23	USB0_PWEN	—	—	—	—	—	—	—	GP7[23]	—
GP-7-24	USB0_OVC	—	—	—	—	—	—	—	GP7[24]	—
GP-7-25	USB1_PWEN	—	—	—	—	—	—	—	GP7[25]	—

Legend: — Setting prohibited

5.3.27 Module Select Register (MOD_SEL)

Function: MOD_SEL selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SCIF, HSCIF, SSI, QSPI, VI , TMU, LBSC, TSIF and MSIOF are assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups. When ssi7 and ssi8 (in MOD_SEL2 register) are to be used simultaneously, the values of sel_ssi7 and sel_ssi8 must be the same so that the selected pins belong to the same group. If this is not the case, correct operation is not guaranteed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	sel_ scif1_1	sel_ scif1_0	sel_ scifb_1	sel_ scifb_0	sel_ scifb2_1	sel_ scifb2_0	sel_ scifb1_2	sel_ scifb1_1	sel_ scifb1_0	sel_ scifa1_1	sel_ scifa1_0	sel_ ssi9	sel_ scfa	sel_qsp	sel_ ssi7_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ hscif1_2	sel_ hscif1_1	sel_ hscif1_0	—	—	sel_ vi1_1	sel_ vi1_0	—	—	sel_ tmu1	sel_ lbs_1	sel_ lbs_0	sel_ tsif0_1	sel_ tsif0_0	sel_ sof0_1	sel_ sof0_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 1 * (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_scif1 [1:0]	RX1 of the A25 pin TX1 of the A24 pin	—	RX1_B of the DU1_DG1 pin TX1_B of the DU1_DG0 pin	RX1_C of the VI0_R7 pin TX1_C of the VI0_R6 pin	RX1_D of the SSI_SCK9 pin TX1_D of the SSI_SDATA8 pin	—
sel_scifb [1:0]	SCIFB0_CTS# of the HCTS0# pin SCIFB0_RTS# of the HRTS0# pin SCIFB0_RXD of the HRX0 pin SCIFB0_SCK of the HSCK0 pin SCIFB0_TXD of the HTX0 pin	—	SCIFB0_CTS#_B of the EX_WAIT0 pin SCIFB0_RTS#_B of the WE1# pin SCIFB0_RXD_B of the RD_WR# pin SCIFB0_SCK_B of the SPEEDIN pin SCIFB0_TXD_B of the WE0# pin	SCIFB0_RXD_C of the SSI_SCK0129 pin SCIFB0_SCK_C of the AUDIO_CLKC pin SCIFB0_TXD_C of the SSI_WS0129 pin	SCIFB0_RXD_D of the VI0_R7 pin SCIFB0_SCK_D of the VI0_G4 pin SCIFB0_TXD_D of the VI0_G5 pin	—
sel_scifb2 [1:0]	SCIFB2_CTS# of the VI0_G0 pin SCIFB2_RTS# of the VI0_G1 pin SCIFB2_RXD of the VI0_G3 pin SCIFB2_SCK of the VI0_G2 pin SCIFB2_TXD of the VI0_G4 pin	—	SCIFB2_CTS#_B of the DU1_DG6 pin SCIFB2_RTS#_B of the DU1_DG7 pin SCIFB2_RXD_B of the DU1_DG4 pin SCIFB2_SCK_B of the SPEEDIN pin SCIFB2_TXD_B of the DU1_DG5 pin	SCIFB2_RXD_C of the SSI_SCK0129 pin SCIFB2_SCK_C of the STP_ISD_0 pin SCIFB2_TXD_C of the SSI_WS0129 pin	SCIFB2_RXD_D of the STP_ISCLK_0 pin SCIFB2_TXD_D of the STP_IVCXO27_0 pin	—
sel_scifb1 [2:0]	SCIFB1_RXD of the HRX1 pin SCIFB1_SCK of the HSCK1 pin SCIFB1_TXD of the HTX1 pin	SCIFB1_SCK_B of the A19 pin SCIFB1_RXD of the HRX1 pin SCIFB1_TXD of the HTX1 pin	SCIFB1_RXD_B of the EX_CS5# pin SCIFB1_SCK_B of the A19 pin SCIFB1_TXD_B of the BS# pin	SCIFB1_RXD_C of the A18 pin SCIFB1_SCK_C of the IRQ1 pin SCIFB1_TXD_C of the A19 pin	SCIFB1_RXD_D of the IRQ0 pin SCIFB1_TXD_D of the IRQ2 pin	—

Bit Name	Function 1 (Set Value = H'0)	Function 1 * (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_scifa1 [1:0]	SCIFA1_RXD of the A25 pin SCIFA1_SCK of the DU1_DG2 pin SCIFA1_TXD of the A24 pin	—	SCIFA1_RXD_B of the DU1_DG1 pin SCIFA1_SCK_B of the A16 pin SCIFA1_TXD_B of the DU1_DG0 pin	SCIFA1_RXD_C of the A18 pin SCIFA1_TXD_C of the A19 pin	—	—
sel_ssi9	SSI_SCK9 of the SSI_SCK9 pin SSI_SDATA9 of the SSI_SDATA9 pin SSI_WS9 of the SSI_WS9 pin	—	SSI_SCK9_B of the DU1_DG6 pin SSI_SDATA9_B of the DU1_DB2 pin SSI_WS9_B of the DU1_DG7 pin	—	—	—
sel_scfa	SCIFA0_RXD of the A23 pin SCIFA0_TXD of the A22 pin	—	SCIFA0_RXD_B of the DU1_DR1 pin SCIFA0_TXD_B of the DU1_DR0 pin	—	—	—
sel_qsp	IO2 of the A23 pin IO3 of the A24 pin MISO_IO1 of the A22 pin MOSI_IO0 of the A21 pin SPCLK of the A20 pin SSL of the A25 pin	—	IO2_B of the SD0_DATA1 pin IO3_B of the SD0_DATA2 pin MISO_IO1_B of the SD0_DATA0 pin MOSI_IO0_B of the SD0_CMD pin SPCLK_B of the SD0_CLK pin SSL_B of the SD0_DATA3 pin	—	—	—
sel_ssi7	SSI_SCK78 of the SSI_SCK78 pin SSI_SDATA7 of the SSI_SDATA7 pin SSI_WS78 of the SSI_WS78 pin	—	SSI_SCK78_B of the DU1_DG2 pin SSI_SDATA7_B of the DU1_DG4 pin SSI_WS78_B of the DU1_DG3 pin	—	—	—
sel_hscif1 [2:0]	HCTS1# of the HCTS1# pin HRTS1# of the HRTS1# pin HRX1 of the HRX1 pin HSCK1 of the HSCK1 pin HTX1 of the HTX1 pin	—	HRX1_B of the EX_CS5# pin HTX1_B of the BS# pin	HCTS1#_C of the IRQ7 pin HRTS1#_C of the IRQ8 pin HRX1_C of the IRQ4 pin HSCK1_C of the IRQ6 pin HTX1_C of the IRQ5 pin	HRX1_D of the VI0_R7 pin HTX1_D of the VI0_G5 pin	HCTS1#_E of the SSI_WS2 pin HRTS1#_E of the SSI_SDATA2 pin HRX1_E of the IRQ4 pin HSCK1_E of the SSI_SCK2 pin HTX1_E of the IRQ5 pin
sel_vi1[1:0]	VI1_CLKENB of the VI1_CLKENB pin VI1_CLK of the VI1_CLK pin VI1_DATA0 of the VI1_DATA0 pin VI1_DATA1 of the VI1_DATA1 pin VI1_DATA2 of the VI1_DATA2 pin VI1_DATA3 of the VI1_DATA3 pin VI1_DATA4 of the VI1_DATA4 pin VI1_DATA5 of the VI1_DATA5 pin VI1_DATA6 of the VI1_DATA6 pin VI1_DATA7 of the VI1_DATA7 pin VI1_FIELD of the VI1_FIELD pin VI1_HSYNC# of the VI1_HSYNC# pin VI1_VSYNC# of the VI1_VSYNC# pin	—	VI1_CLK_B of the DU1_DB0 pin VI1_CLKENB_B of the DU1_DB3 pin VI1_DATA0_B of the DU1_DR0 pin VI1_DATA1_B of the DU1_DR1 pin VI1_DATA2_B of the DU1_DG0 pin VI1_DATA3_B of the DU1_DG1 pin VI1_DATA4_B of the DU1_DG2 pin VI1_DATA5_B of the DU1_DG3 pin VI1_DATA6_B of the DU1_DG4 pin VI1_DATA7_B of the DU1_DG5 pin VI1_FIELD_B of the DU1_DB4 pin VI1_HSYNC#_B of the DU1_DB1 pin VI1_VSYNC#_B of the DU1_DB2 pin	VI1_CLK_C of the MSIOF0_SCK pin VI1_CLKENB_C of the MSIOF0_SYNC pin VI1_DATA0_C of the MSIOF0_RXD pin VI1_DATA1_C of the HCTS0# pin VI1_DATA2_C of the HRTS0# pin VI1_DATA3_C of the HSCK0 pin VI1_DATA4_C of the HRX0 pin VI1_DATA5_C of the HTX0 pin VI1_DATA6_C of the HRX1 pin VI1_DATA7_C of the HTX1 pin VI1_FIELD_C of the MSIOF0_TXD pin VI1_HSYNC#_C of the MSIOF0_SS1 pin VI1_VSYNC#_C of the MSIOF0_SS2 pin	—	—
sel_tmu1	TCLK1 of the HCTS0# pin	—	TCLK1_B of the ETH_TX_EN pin	—	—	—

Bit Name	Function 1 (Set Value = H'0)	Function 1 * (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_lbs[1:0]	ATADIR0# of the EX_CS3# pin ATAG0# of the EX_CS3# pin ATARD0# of the EX_CS4# pin ATAWR0# of the EX_CS2# pin DACK2 of the A25 pin DREQ1 of the A18 pin DREQ2 of the A24 pin	—	ATADIR0#_B of the CS1#/A26 pin ATAG0#_B of the CS0# pin ATARD0#_B of the WE1# pin ATAWR0#_B of the A21 pin DACK2_B of the A17 pin DREQ1_D of the RD_WR# pin DREQ2_B of the A16 pin	ATADIR0#_C of the A14 pin ATAG0#_C of the A13 pin ATAWR0#_C of the A0 pin DREQ1_C of the A25 pin DREQ2_C of the SPEEDIN pin	DREQ1_D of the RD_WR# pin DREQ2 of the A24 pin	—
sel_tsif0 [1:0]	TS_SCK0 of the SSI_WS5 pin TS_SDATA0 of the SSI_SCK5 pin TS_SDEN0 of the SSI_SDATA5 pin TS_SPSYNC0 of the SSI_SCK6 pin	—	TS_SCK0_B of the VI1_VSYNC# pin TS_SDATA0_B of the VI1_HSYNC# pin TS_SDEN0_B of the VI1_CLKENB pin TS_SPSYNC0_B of the VI1_FIELD pin	TS_SCK0_C of the VI0_R1 pin TS_SDATA0_C of the VI0_R0 pin TS_SDEN0_C of the VI0_R2 pin TS_SPSYNC0_C of the VI0_R3 pin	TS_SCK0_D of the VI0_FIELD pin TS_SDATA0_D of the VI0_CLKENB pin TS_SDEN0_D of the VI0_HSYNC# pin TS_SPSYNC0_D of the VI0_VSYNC# pin	—
sel_sof0 [1:0]	MSIOF0_RXD of the MSIOF0_RXD pin MSIOF0_SCK of the MSIOF0_SCK pin MSIOF0_SS1 of the MSIOF0_SS1 pin MSIOF0_SS2 of the MSIOF0_SS2 pin MSIOF0_SYNC of the MSIOF0_SYNC pin MSIOF0_TXD of the MSIOF0_TXD pin	—	MSIOF0_RXD_B of the A5 pin MSIOF0_SCK_B of the A0 pin MSIOF0_SS1_B of the A2 pin MSIOF0_SS2_B of the A3 pin MSIOF0_SYNC_B of the A1 pin MSIOF0_TXD_B of the A4 pin	MSIOF0_RXD_C of the STP_ISSYNC_0 pin MSIOF0_SCK_C of the STP_ISCLK_0 pin MSIOF0_SS1_C of the STP_ISD_0 pin MSIOF0_SS2_C of the STP_ISEN_0 pin MSIOF0_SYNC_C of the STP_IVCXO27_0 pin MSIOF0_TXD_C of the STP_OPWM_0 pin	—	—

Legend: – Setting prohibited

Note: * Using SCIFB1_SCK_B is regardless of value of the bit sel_scifb1[2:0].

5.3.28 Module Select Register 2 (MOD_SEL2)

Function: MOD_SEL2 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SCIF, RCAN, ADG and SSI is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. When ssi8 and ssi7 (in MOD_SEL register) are to be used simultaneously, the values of sel_ssi8 and sel_ssi7 must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_ scif0_2	sel_ scif0_1	sel_ scif0_0	—	sel_scif	sel_ can0_2	sel_ can0_1	sel_ can0_0	sel_ can1_1	sel_ can1_0	—	sel_ scifa2_0	sel_ scif4_1	sel_ scif4_0	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ adg_0	—	—	—	sel_ scifa5_1	sel_ scifa5_0	—	—	—	sel_ scifa4_1	sel_ scifa4_0	sel_ scifa3_1	sel_ scifa3_0	—	—	sel_ ssi8_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)
sel_scif0[2:0]	RX0 of the A23 pin TX0 of the A22 pin	RX0_B of the DU1_DR1 pin TX0_B of the DU1_DR0 pin	RX0_C of the VI0_R5 pin TX0_C of the VI0_R4 pin	RX0_D of the SSI_SDATA7 pin TX0_D of the SSI_WS78 pin	RX0_E of the MSIOF0_SS2 pin TX0_E of the MSIOF0_SS1 pin	—
sel_scif	SCIF_CLK of the AUDIO_CLKB pin	SCIF_CLK_B of the IRQ9 pin	—	—	—	—
sel_can0[2:0]	CAN0_RX of the DU1_EXODDF_ DU1_ODDF_DISP_CDE pin CAN0_TX of the DU1_DOTCLKOUT1 pin	CAN0_RX_B of the HRX0 pin CAN0_TX_B of the HTX0 pin	CAN0_RX_C of the ETH_LINK pin CAN0_TX_C of the ETH_RXD1 pin	CAN0_RX_D of the SSI_SDATA9 pin CAN0_TX_D of the SSI_WS9 pin	CAN0_RX_E of the VI0_R7 pin CAN0_TX_E of the VI0_G5 pin	CAN0_RX_F of the SD0_CD pin CAN0_TX_F of the SD0_WP pin
sel_can1[1:0]	CAN1_RX of the DU1_DB4 pin CAN1_TX of the DU1_DB5 pin	CAN1_RX_B of the HRTS1# pin CAN1_TX_B of the HCTS1# pin	CAN1_RX_C of the ETH_REFCLK pin CAN1_TX_C of the ETH_TXD1 pin	CAN1_RX_D of the SIM0_D pin CAN1_TX_D of the SIM0_RST pin	—	—
sel_scifa2	SCIFA2_RXD of the AUDIO_CLKC pin SCIFA2_TXD of the AUDIO_CLKOUT pin	SCIFA2_SCK of the DU1_DB2 pin * SCIFA2_RXD_B of the DU1_DB1 pin SCIFA2_TXD_B of the DU1_DB0 pin	—	—	—	—
sel_scif4[1:0]	RX4 of the VI0_FIELD pin TX4 of the VI0_CLKENB pin	RX4_B of the VI1_VSYNC# pin TX4_B of the VI1_HSYNC# pin	RX4_C of the GPS_MAG pin TX4_C of the GPS_SIGN pin	—	—	—
sel_adg	AUDIO_CLKB of the AUDIO_CLKB pin	AUDIO_CLKB_B of the GPS_CLK pin	—	—	—	—

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)
sel_scifa5 [1:0]	SCIFA5_RXD of the VI0_VSYNC# pin SCIFA5_TXD of the VI0_HSYNC# pin	SCIFA5_RXD_B of the SD0_WP pin SCIFA5_TXD_B of the SD0_CD pin	SCIFA5_RXD_C of the SD3_WP pin SCIFA5_TXD_C of the SD3_CD pin	—	—	—
sel_scifa4 [1:0]	SCIFA4_RXD of the VI0_FIELD pin SCIFA4_TXD of the VI0_CLKENB pin	SCIFA4_RXD_B of the VI1_VSYNC# pin SCIFA4_TXD_B of the VI1_HSYNC# pin	SCIFA4_RXD_C of the GPS_MAG pin SCIFA4_TXD_C of the GPS_SIGN pin	—	—	—
sel_scifa3 [1:0]	SCIFA3_RXD of the DU1_DB6 pin SCIFA3_SCK of the DU1_DB7 pin SCIFA3_TXD of the DU1_DB5 pin	SCIFA3_RXD_B of the ETH_REFCLK pin SCIFA3_SCK_B of the VI0_DATA3_VI0_B3 pin SCIFA3_TXD_B of the ETH_TXD1 pin	SCIFA3_RXD_C of the GPS_SIGN pin SCIFA3_SCK_C of the GPS_MAG pin SCIFA3_TXD_C of the GPS_CLK pin	—	—	—
sel_ssi8	SSI_SDATA8 of the SSI_SDATA8 pin	SSI_SDATA8_B of the DU1_DG5 pin	—	—	—	—

Legend: – Setting prohibited

Note: * Using SCIFA2_SCK is regardless of value of the bit sel_scifa2.

5.3.29 Module Select Register 3 (MOD_SEL3)

Function: MOD_SEL3 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SCIF, RCAN, I2C, IIC and MMC is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. When ssi8 (in MOD_SEL2 register) and ssi7 (in MOD_SEL register) are to be used simultaneously, the values of sel_ssi8 and sel_ssi7 must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_ hscif2_1	sel_ hscif2_0	sel_can clk_1	sel_can clk_0	sel_ iic1_1	sel_ iic1_0	sel_ iic0_1	sel_ iic0_0	sel_ i2c4_1	sel_ i2c4_0	sel_ i2c3_1	sel_ i2c3_0	sel_ scif3_1	sel_ scif3_0	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ mmc	sel_ scif5	—	—	sel_ i2c2_1	sel_ i2c2_0	sel_ i2c1_2	sel_ i2c1_1	sel_ i2c1_0	sel_ i2c0_1	sel_ i2c0_0	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_hscif2[1:0]	HCTS2# of the VI0_G0 pin HRTS2# of the VI0_G1 pin HRX2 of the VI0_G3 pin HSCK2 of the VI0_G2 pin HTX2 of the VI0_G4 pin	HCTS2#_B of the WE0# pin HRTS2#_B of the EX_WAIT0 pin HRX2_B of the RD_WR# pin HTX2_B of the WE1# pin	HRX2_C of the SSI_SCK0129 pin HSCK2_C of the SPEEDIN pin HTX2_C of the SSI_WS0129 pin	HTX2_D of the SPEEDIN pin HRX2_D of the RD_WR# pin	—
sel_canclk[1:0]	CAN_CLK of the HSCK0 pin	CAN_CLK_B of the ETH_TX_EN pin	CAN_CLK_C of the SIM0_CLK pin	CAN_CLK_D of the IRQ9 pin	—
sel_iic1[1:0] (iic8)	IIC1_SCL of the VI0_G0 pin IIC1_SDA of the VI0_G1 pin	IIC1_SCL_B of the SSI_WS1 pin IIC1_SDA_B of the SSI_SDATA1 pin	IIC1_SCL_C of the SD3_CD pin IIC1_SDA_C of the SD3_WP pin	—	—
sel_iic0[1:0] (iic7)	IIC0_SCL of the ETH_RX_ER pin IIC0_SDA of the ETH_RXD0 pin	IIC0_SCL_B of the SSI_SDATA0 pin IIC0_SDA_B of the SSI_SCK1 pin	IIC0_SCL_C of the MSIOF0_SS1 pin IIC0_SDA_C of the MSIOF0_SS2 pin	—	—
sel_i2c4[1:0]	I2C4_SCL of the VI0_G0 pin I2C4_SDA of the VI0_G1 pin	I2C4_SCL_B of the VI0_R6 pin I2C4_SDA_B of the VI0_R7 pin	I2C4_SCL_C of the IRQ3 pin I2C4_SDA_C of the IRQ4 pin	—	—
sel_i2c3[1:0]	I2C3_SCL of the ETH_RX_ER pin I2C3_SDA of the ETH_RXD0 pin	I2C3_SCL_B of the VI0_G2 pin I2C3_SDA_B of the VI0_G3 pin	I2C3_SCL_C of the DU1_DB6 pin I2C3_SDA_C of the DU1_DB7 pin	I2C3_SCL_D of the A11 pin I2C3_SDA_D of the A12 pin	—
sel_scif3[1:0]	RX3 of the DU1_DB6 pin SCIF3_SCK of the DU1_DB7 pin TX3 of the DU1_DB5 pin	RX3_B of the DU1_EXODDF_ DU1_ODDF_DISP_CDE pin SCIF3_SCK_B of the VI0_DATA3_VI0_B3 pin TX3_B of the DU1_DOTCLKOUT1 pin	RX3_C of the SD0_WP pin TX3_C of the SD0_CD pin	RX3_D of the SSI_SDATA9 pin TX3_D of the SSI_WS9 pin	—
sel_mmc	MMC_D6 of the MSIOF0_SS1 pin MMC_D7 of the MSIOF0_SS2 pin	MMC_D6_B of the SD0_CD pin MMC_D7_B of the SD0_WP pin	—	—	—

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_scif5	RX5 of the VI0_VSYNC# pin TX5 of the VI0_HSYNC# pin	RX5_B of the SD3_WP pin TX5_B of the SD3_CD pin	—	—	—
sel_i2c2[1:0]	I2C2_SCL of the SSI_SCK2 pin I2C2_SDA of the SSI_WS2 pin	I2C2_SCL_B of the DU1_DOTCLKOUT1 pin I2C2_SDA_B of the DU1_EXODDF_ DU1_ODDF_DISP_CDE pin	I2C2_SCL_C of the ETH_MDIO pin I2C2_SDA_C of the ETH_CRS_DV pin	I2C2_SCL_D of the ETH_RXD1 pin I2C2_SDA_D of the ETH_LINK pin	—
sel_i2c1[2:0]	I2C1_SCL of the CS0# pin I2C1_SDA of the CS1#/A26 pin	I2C1_SCL_B of the SSI_WS1 pin I2C1_SDA_B of the SSI_SDATA1 pin	I2C1_SCL_C of the SD2_CD pin I2C1_SDA_C of the SD2_WP pin	I2C1_SCL_D of the VI0_R4 pin I2C1_SDA_D of the VI0_R5 pin	I2C1_SCL_E of the IRQ5 pin I2C1_SDA_E of the IRQ6 pin
sel_i2c0[1:0]	I2C0_SCL of the A8 pin I2C0_SDA of the A9 pin	I2C0_SCL_B of the SSI_SDATA0 pin I2C0_SDA_B of the SSI_SCK1 pin	I2C0_SCL_C of the A0 pin I2C0_SDA_C of the A17 pin	—	—

Legend: – Setting prohibited

5.3.30 Module Select Register 4 (MOD_SEL4)

Function: MOD_SEL4 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the MSIOF, HSCIF, DU, and SSI is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_sof1_2	sel_sof1_1	sel_sof1_0	sel_hscif0_	sel_hscif0_	sel_dis_1	sel_dis_0	—	—	—	—	sel_scif2_2	sel_scif2_1	sel_scif2_0	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	sel_sof2_2	sel_sof2_1	sel_sof2_0	—	sel_ssi1	sel_ssi0	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_sof1[2:0]	MSIOF1_RXD of the A11 pin MSIOF1_SCK of the A6 pin MSIOF1_SS1 of the A8 pin MSIOF1_SS2 of the A9 pin MSIOF1_SYNC of the A7 pin MSIOF1_TXD of the A10 pin	MSIOF1_RXD_B of the IRQ8 pin MSIOF1_SCK_B of the AUDIO_CLKB pin MSIOF1_SS1_B of the AUDIO_CLKOUT pin MSIOF1_SS2_B of the IRQ6 pin MSIOF1_SYNC_B of the AUDIO_CLKC pin MSIOF1_TXD_B of the IRQ7 pin	MSIOF1_RXD_C of the SSI_SCK6 pin MSIOF1_SCK_C of the SSI_SCK5 pin MSIOF1_SYNC_C of the SSI_WS5 pin MSIOF1_TXD_C of the SSI_SDATA5 pin	MSIOF1_RXD_D of the A11 pin MSIOF1_SCK_D of the A12 pin MSIOF1_SS1_D of the A13 pin MSIOF1_SYNC_D of the A14 pin MSIOF1_TXD_D of the A10 pin	MSIOF1_RXD_E of the ETH_RXD1 pin MSIOF1_SCK_E of the ETH_LINK pin MSIOF1_SYNC_E of the ETH_REFCLK pin MSIOF1_TXD_E of the ETH_TXD1 pin
sel_hscif0[1:0]	HCTS0# of the HCTS0# pin HRTS0# of the HRTS0# pin HRX0 of the HRX0 pin HSCK0 of the HSCK0 pin HTX0 of the HTX0 pin	HCTS0#_B of the DU1_DG5 pin HRTS0#_B of the DU1_DG6 pin HRX0_B of the DU1_DG4 pin HTX0_B of the DU1_DG7 pin	HRX0_C of the SSI_SCK0129 pin HTX0_C of the SSI_WS0129 pin HSCK0_C of the SPEEDIN pin	—	—
sel_dis[1:0]	DU1_DOTCLKIN of the DU1_DOTCLKIN pin	DU1_DOTCLKIN_B of the IRQ9 pin	DU1_DOTCLKIN_C of the GPS_CLK pin	—	—
sel_scif2[2:0]	RX2 of the AUDIO_CLKC pin TX2 of the AUDIO_CLKOUT pin	RX2_B of the DU1_DB1 pin TX2_B of the DU1_DB0 pin	RX2_C of the MSIOF0_SCK pin TX2_C of the MSIOF0_SYNC pin	—	RX2_E of the SSI_WS2 pin TX2_E of the SSI_SDATA2 pin
sel_sof2[2:0]	MSIOF2_RXD of the EX_CS4# pin MSIOF2_SCK of the EX_CS1# pin MSIOF2_SS1 of the EX_CS5# pin MSIOF2_SS2 of the BS# pin MSIOF2_SYNC of the EX_CS2# pin MSIOF2_TXD of the EX_CS3# pin	MSIOF2_RXD_B of the DU1_DB1 pin MSIOF2_SCK_B of the DU1_DR0 pin MSIOF2_SS1_B of the DU1_DG0 pin MSIOF2_SS2_B of the DU1_DG1 pin MSIOF2_SYNC_B of the DU1_DR1 pin MSIOF2_TXD_B of the DU1_DB0 pin	MSIOF2_RXD_C of the SSI_SDATA1 pin MSIOF2_SCK_C of the SSI_SDATA0 pin MSIOF2_SYNC_C of the SSI_SCK1 pin MSIOF2_TXD_C of the SSI_WS1 pin	MSIOF2_RXD_D of the SSI_SCK6 pin MSIOF2_SCK_D of the SSI_SDATA4 pin MSIOF2_SS1_D of the SSI_SDATA5 pin MSIOF2_SS2_D of the SSI_WS6 pin MSIOF2_SYNC_D of the SSI_SCK5 pin MSIOF2_TXD_D of the SSI_WS5 pin	MSIOF2_RXD_E of the IRQ4 pin MSIOF2_SCK_E of the IRQ5 pin MSIOF2_SYNC_E of the IRQ6 pin MSIOF2_TXD_E of the IRQ3 pin
sel_ssi1	SSI_SCK1 of the SSI_SCK1 pin SSI_SDATA1 of the SSI_SDATA1 pin SSI_WS1 of the SSI_WS1 pin	SSI_SCK1_B of the DU1_DR5 pin SSI_SDATA1_B of the DU1_DR7 pin SSI_WS1_B of the DU1_DR6 pin	—	—	—

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_ssi0	SSI_SCK0129 of the SSI_SCK0129 pin SSI_SDATA0 of the SSI_SDATA0 pin SSI_WS0129 of the SSI_WS0129 pin	SSI_SCK0129_B of the DU1_DR2 pin SSI_SDATA0_B of the DU1_DR4 pin SSI_WS0129_B of the DU1_DR3 pin	—	—	—

Legend: – Setting prohibited

5.3.31 LSI Pin Pull-Up Control Register 0 (PUPR0)

Function: PUPR0 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR0 [31]	PUPR0 [30]	PUPR0 [29]	PUPR0 [28]	PUPR0 [27]	PUPR0 [26]	PUPR0 [25]	PUPR0 [24]	PUPR0 [23]	PUPR0 [22]	PUPR0 [21]	PUPR0 [20]	PUPR0 [19]	PUPR0 [18]	PUPR0 [17]	PUPR0 [16]
Initial value:	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR0 [15]	PUPR0 [14]	PUPR0 [13]	PUPR0 [12]	PUPR0 [11]	PUPR0 [10]	PUPR0 [9]	PUPR0 [8]	PUPR0 [7]	PUPR0 [6]	PUPR0 [5]	PUPR0 [4]	PUPR0 [3]	PUPR0 [2]	PUPR0 [1]	PUPR0 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR0[31:0]	H'D87F FFFF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR0[31]	A9 pin is pulled up
PUPR0[30]	A8 pin is pulled up
PUPR0[29]	A7 pin is pulled up
PUPR0[28]	A6 pin is pulled up
PUPR0[27]	A5 pin is pulled up
PUPR0[26]	A4 pin is pulled up
PUPR0[25]	A3 pin is pulled up
PUPR0[24]	A2 pin is pulled up
PUPR0[23]	A1 pin is pulled up
PUPR0[22]	A0 pin is pulled up
PUPR0[21]	D15 pin is pulled up
PUPR0[20]	D14 pin is pulled up
PUPR0[19]	D13 pin is pulled up
PUPR0[18]	D12 pin is pulled up
PUPR0[17]	D11 pin is pulled up
PUPR0[16]	D10 pin is pulled up
PUPR0[15]	D9 pin is pulled up
PUPR0[14]	D8 pin is pulled up
PUPR0[13]	D7 pin is pulled up
PUPR0[12]	D6 pin is pulled up
PUPR0[11]	D5 pin is pulled up
PUPR0[10]	D4 pin is pulled up
PUPR0[9]	D3 pin is pulled up
PUPR0[8]	D2 pin is pulled up
PUPR0[7]	D1 pin is pulled up

Bit Name	Set Value = 1
PUPR0[6]	D0 pin is pulled up
PUPR0[5]	DU0_DOTCLKIN pin is pulled up
PUPR0[4]	A24 pin is pulled up
PUPR0[3]	A23 pin is pulled up
PUPR0[2]	A22 pin is pulled up
PUPR0[1]	A21 pin is pulled up
PUPR0[0]	A20 pin is pulled up

5.3.32 LSI Pin Pull-Up Control Register 1 (PUPR1)

Function: PUPR1 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR1 [31]	PUPR1 [30]	PUPR1 [29]	PUPR1 [28]	PUPR1 [27]	PUPR1 [26]	PUPR1 [25]	PUPR1 [24]	PUPR1 [23]	PUPR1 [22]	PUPR1 [21]	PUPR1 [20]	PUPR1 [19]	PUPR1 [18]	PUPR1 [17]	PUPR1 [16]
Initial value:	1	1	1	0	1	1	0	0	1	0	0	0	1	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR1 [15]	PUPR1 [14]	PUPR1 [13]	PUPR1 [12]	PUPR1 [11]	PUPR1 [10]	PUPR1 [9]	PUPR1 [8]	PUPR1 [7]	PUPR1 [6]	PUPR1 [5]	PUPR1 [4]	PUPR1 [3]	PUPR1 [2]	PUPR1 [1]	PUPR1 [0]
Initial value:	0	1	1	1	1	1	0	1	1	1	0	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR1[31:0]	H'EC8B 7DC6	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR1[31]	SSI_WS0129 pin is pulled up
PUPR1[30]	SSI_SCK0129 pin is pulled up
PUPR1[29]	SPEEDIN pin is pulled up
PUPR1[28]	DACK0 pin is pulled up
PUPR1[27]	DREQ0 pin is pulled up
PUPR1[26]	EX_WAIT0 pin is pulled up
PUPR1[25]	WE1# pin is pulled up
PUPR1[24]	WE0# pin is pulled up
PUPR1[23]	RD/WR# pin is pulled up
PUPR1[22]	RD# pin is pulled up
PUPR1[21]	BS# pin is pulled up
PUPR1[20]	EX_CS5# pin is pulled up
PUPR1[19]	EX_CS4# pin is pulled up
PUPR1[18]	EX_CS3# pin is pulled up
PUPR1[17]	EX_CS2# pin is pulled up
PUPR1[16]	EX_CS1# pin is pulled up
PUPR1[15]	EX_CS0# pin is pulled up
PUPR1[14]	CS1#/A26 pin is pulled up
PUPR1[13]	TDI pin is pulled up
PUPR1[12]	TMS pin is pulled up
PUPR1[11]	TCK pin is pulled up
PUPR1[10]	TRST# pin is pulled up
PUPR1[9]	A19 pin is pulled up
PUPR1[8]	A18 pin is pulled up
PUPR1[7]	A17 pin is pulled up

Bit Name	Set Value = 1
PUPR1[6]	A16 pin is pulled up
PUPR1[5]	A15 pin is pulled up
PUPR1[4]	A14 pin is pulled up
PUPR1[3]	A13 pin is pulled up
PUPR1[2]	A12 pin is pulled up
PUPR1[1]	A11 pin is pulled up
PUPR1[0]	A10 pin is pulled up

5.3.33 LSI Pin Pull-Up Control Register 2 (PUPR2)

Function: PUPR2 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR2 [31]	PUPR2 [30]	PUPR2 [29]	PUPR2 [28]	PUPR2 [27]	PUPR2 [26]	PUPR2 [25]	PUPR2 [24]	PUPR2 [23]	PUPR2 [22]	PUPR2 [21]	PUPR2 [20]	PUPR2 [19]	PUPR2 [18]	PUPR2 [17]	PUPR2 [16]
Initial value:	1	1	0	1	1	1	1	0	0	1	1	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR2 [15]	PUPR2 [14]	PUPR2 [13]	PUPR2 [12]	PUPR2 [11]	PUPR2 [10]	PUPR2 [9]	PUPR2 [8]	PUPR2 [7]	PUPR2 [6]	PUPR2 [5]	PUPR2 [4]	PUPR2 [3]	PUPR2 [2]	PUPR2 [1]	PUPR2 [0]
Initial value:	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR2[31:0]	H'DE61 F3FF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR2[31]	IRQ1 pin is pulled up
PUPR2[30]	IRQ0 pin is pulled up
PUPR2[29]	AUDIO_CLKOUT pin is pulled up
PUPR2[28]	AUDIO_CLKC pin is pulled up
PUPR2[27]	AUDIO_CLKB pin is pulled up
PUPR2[26]	AUDIO_CLKA pin is pulled up
PUPR2[25]	SSI_SDATA9 pin is pulled up
PUPR2[24]	SSI_WS9 pin is pulled up
PUPR2[23]	SSI_SCK9 pin is pulled up
PUPR2[22]	SSI_SDATA8 pin is pulled up
PUPR2[21]	SSI_SDATA7 pin is pulled up
PUPR2[20]	SSI_WS78 pin is pulled up
PUPR2[19]	SSI_SCK78 pin is pulled up
PUPR2[18]	SSI_SDATA6 pin is pulled up
PUPR2[17]	SSI_WS6 pin is pulled up
PUPR2[16]	SSI_SCK6 pin is pulled up
PUPR2[15]	SSI_SDATA5 pin is pulled up
PUPR2[14]	SSI_WS5 pin is pulled up
PUPR2[13]	SSI_SCK5 pin is pulled up
PUPR2[12]	SSI_SDATA4 pin is pulled up
PUPR2[11]	SSI_WS4 pin is pulled up
PUPR2[10]	SSI_SCK4 pin is pulled up
PUPR2[9]	SSI_SDATA3 pin is pulled up
PUPR2[8]	SSI_WS34 pin is pulled up
PUPR2[7]	SSI_SCK34 pin is pulled up

Bit Name	Set Value = 1
PUPR2[6]	SSI_SDATA2 pin is pulled up
PUPR2[5]	SSI_WS2 pin is pulled up
PUPR2[4]	SSI_SCK2 pin is pulled up
PUPR2[3]	SSI_SDATA1 pin is pulled up
PUPR2[2]	SSI_WS1 pin is pulled up
PUPR2[1]	SSI_SCK1 pin is pulled up
PUPR2[0]	SSI_SDATA0 pin is pulled up

5.3.34 LSI Pin Pull-Up Control Register 3 (PUPR3)

Function: PUPR3 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR3 [31]	PUPR3 [30]	PUPR3 [29]	PUPR3 [28]	PUPR3 [27]	PUPR3 [26]	PUPR3 [25]	PUPR3 [24]	PUPR3 [23]	PUPR3 [22]	PUPR3 [21]	PUPR3 [20]	PUPR3 [19]	PUPR3 [18]	PUPR3 [17]	PUPR3 [16]
Initial value:	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR3 [15]	PUPR3 [14]	PUPR3 [13]	PUPR3 [12]	PUPR3 [11]	PUPR3 [10]	PUPR3 [9]	PUPR3 [8]	PUPR3 [7]	PUPR3 [6]	PUPR3 [5]	PUPR3 [4]	PUPR3 [3]	PUPR3 [2]	PUPR3 [1]	PUPR3 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR3[31:0]	H'DFFF FFFF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR3[31]	DU1_DB7
PUPR3[30]	DU1_DB6
PUPR3[29]	DU1_DB5
PUPR3[28]	DU1_DB4 pin is pulled up
PUPR3[27]	DU1_DB3 pin is pulled up
PUPR3[26]	DU1_DB2 pin is pulled up
PUPR3[25]	DU1_DB1 pin is pulled up
PUPR3[24]	DU1_DB0 pin is pulled up
PUPR3[23]	DU1_DG7 pin is pulled up
PUPR3[22]	DU1_DG6 pin is pulled up
PUPR3[21]	DU1_DG5 pin is pulled up
PUPR3[20]	DU1_DG4 pin is pulled up
PUPR3[19]	DU1_DG3 pin is pulled up
PUPR3[18]	DU1_DG2 pin is pulled up
PUPR3[17]	DU1_DG1 pin is pulled up
PUPR3[16]	DU1_DG0 pin is pulled up
PUPR3[15]	DU1_DR7 pin is pulled up
PUPR3[14]	DU1_DR6 pin is pulled up
PUPR3[13]	DU1_DR5 pin is pulled up
PUPR3[12]	DU1_DR4 pin is pulled up
PUPR3[11]	DU1_DR3 pin is pulled up
PUPR3[10]	DU1_DR2 pin is pulled up
PUPR3[9]	DU1_DR1 pin is pulled up
PUPR3[8]	DU1_DR0 pin is pulled up
PUPR3[7]	IRQ9 pin is pulled up

Bit Name	Set Value = 1
PUPR3[6]	IRQ8 pin is pulled up
PUPR3[5]	IRQ7 pin is pulled up
PUPR3[4]	IRQ6 pin is pulled up
PUPR3[3]	IRQ5 pin is pulled up
PUPR3[2]	IRQ4 pin is pulled up
PUPR3[1]	IRQ3 pin is pulled up
PUPR3[0]	IRQ2 pin is pulled up

5.3.35 LSI Pin Pull-Up Control Register 4 (PUPR4)

Function: PUPR4 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR4 [31]	PUPR4 [30]	PUPR4 [29]	PUPR4 [28]	PUPR4 [27]	PUPR4 [26]	PUPR4 [25]	PUPR4 [24]	PUPR4 [23]	PUPR4 [22]	PUPR4 [21]	PUPR4 [20]	PUPR4 [19]	PUPR4 [18]	PUPR4 [17]	PUPR4 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR4 [15]	PUPR4 [14]	PUPR4 [13]	PUPR4 [12]	PUPR4 [11]	PUPR4 [10]	PUPR4 [9]	PUPR4 [8]	PUPR4 [7]	PUPR4 [6]	PUPR4 [5]	PUPR4 [4]	PUPR4 [3]	PUPR4 [2]	PUPR4 [1]	PUPR4 [0]
Initial value:	1	1	1	1	1	1	1	1	0	0	1	0	0	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR4[31:0]	H'FFFF FF27	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR4[31]	VI0_R2 pin is pulled up
PUPR4[30]	VI0_R1 pin is pulled up
PUPR4[29]	VI0_R0 pin is pulled up
PUPR4[28]	VI0_G7 pin is pulled up
PUPR4[27]	VI0_G6 pin is pulled up
PUPR4[26]	VI0_G5 pin is pulled up
PUPR4[25]	VI0_G4 pin is pulled up
PUPR4[24]	VI0_G3 pin is pulled up
PUPR4[23]	VI0_G2 pin is pulled up
PUPR4[22]	VI0_G1 pin is pulled up
PUPR4[21]	VI0_G0 pin is pulled up
PUPR4[20]	VI0_DATA7_VI0_B7 pin is pulled up
PUPR4[19]	VI0_DATA6_VI0_B6 pin is pulled up
PUPR4[18]	VI0_DATA5_VI0_B5 pin is pulled up
PUPR4[17]	VI0_DATA4_VI0_B4 pin is pulled up
PUPR4[16]	VI0_DATA3_VI0_B3 pin is pulled up
PUPR4[15]	VI0_DATA2_VI0_B2 pin is pulled up
PUPR4[14]	VI0_DATA1_VI0_B1 pin is pulled up
PUPR4[13]	VI0_DATA0_VI0_B0 pin is pulled up
PUPR4[12]	VI0_VSYNC# pin is pulled up
PUPR4[11]	VI0_HSYNC# pin is pulled up
PUPR4[10]	VI0_FIELD pin is pulled up
PUPR4[9]	VI0_CLKENB pin is pulled up
PUPR4[8]	VI0_CLK pin is pulled up
PUPR4[7]	DU1_CDE pin is pulled up

Bit Name	Set Value = 1
PUPR4[6]	DU1_DISP pin is pulled up
PUPR4[5]	DU1_EXODDF_DU1_ODDF_DISP_CDE pin is pulled up
PUPR4[4]	DU1_EXVSYNC_DU1_VSYNC pin is pulled up
PUPR4[3]	DU1_EXHSYNC_DU1_HSYNC pin is pulled up
PUPR4[2]	DU1_DOTCLKOUT1 pin is pulled up
PUPR4[1]	DU1_DOTCLKOUT0 pin is pulled up
PUPR4[0]	DU1_DOTCLKIN pin is pulled up

5.3.36 LSI Pin Pull-Up Control Register 5 (PUPR5)

Function: PUPR5 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR5 [31]	PUPR5 [30]	PUPR5 [29]	PUPR5 [28]	PUPR5 [27]	PUPR5 [26]	PUPR5 [25]	PUPR5 [24]	PUPR5 [23]	PUPR5 [22]	PUPR5 [21]	PUPR5 [20]	PUPR5 [19]	PUPR5 [18]	PUPR5 [17]	PUPR5 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR5 [15]	PUPR5 [14]	PUPR5 [13]	PUPR5 [12]	PUPR5 [11]	PUPR5 [10]	PUPR5 [9]	PUPR5 [8]	PUPR5 [7]	PUPR5 [6]	PUPR5 [5]	PUPR5 [4]	PUPR5 [3]	PUPR5 [2]	PUPR5 [1]	PUPR5 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR5[31:0]	H'FFFF FFE1	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR5[31]	STP_ISCLK_0 pin is pulled up
PUPR5[30]	STP_IVCXO27_0 pin is pulled up
PUPR5[29]	ETH_MDC pin is pulled up
PUPR5[28]	ETH_TXD0 pin is pulled up
PUPR5[27]	ETH_MAGIC pin is pulled up
PUPR5[26]	ETH_TX_EN pin is pulled up
PUPR5[25]	ETH_TXD1 pin is pulled up
PUPR5[24]	ETH_REFCLK pin is pulled up
PUPR5[23]	ETH_LINK pin is pulled up
PUPR5[22]	ETH_RXD1 pin is pulled up
PUPR5[21]	ETH_RXD0 pin is pulled up
PUPR5[20]	ETH_RX_ER pin is pulled up
PUPR5[19]	ETH_CRS_DV pin is pulled up
PUPR5[18]	ETH_MDIO pin is pulled up
PUPR5[17]	VI1_DATA7 pin is pulled up
PUPR5[16]	VI1_DATA6 pin is pulled up
PUPR5[15]	VI1_DATA5 pin is pulled up
PUPR5[14]	VI1_DATA4 pin is pulled up
PUPR5[13]	VI1_DATA3 pin is pulled up
PUPR5[12]	VI1_DATA2 pin is pulled up
PUPR5[11]	VI1_DATA1 pin is pulled up
PUPR5[10]	VI1_DATA0 pin is pulled up
PUPR5[9]	VI1_CLK pin is pulled up
PUPR5[8]	VI1_FIELD pin is pulled up
PUPR5[7]	VI1_CLKENB pin is pulled up

Bit Name	Set Value = 1
PUPR5[6]	VI1_VSYNC# pin is pulled up
PUPR5[5]	VI1_HSYNC# pin is pulled up
PUPR5[4]	VI0_R7 pin is pulled up
PUPR5[3]	VI0_R6 pin is pulled up
PUPR5[2]	VI0_R5 pin is pulled up
PUPR5[1]	VI0_R4 pin is pulled up
PUPR5[0]	VI0_R3 pin is pulled up

5.3.37 LSI Pin Pull-Up Control Register 6 (PUPR6)

Function: PUPR6 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR6 [31]	PUPR6 [30]	PUPR6 [29]	PUPR6 [28]	PUPR6 [27]	PUPR6 [26]	PUPR6 [25]	PUPR6 [24]	PUPR6 [23]	PUPR6 [22]	PUPR6 [21]	PUPR6 [20]	PUPR6 [19]	PUPR6 [18]	PUPR6 [17]	PUPR6 [16]
Initial value:	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR6 [15]	PUPR6 [14]	PUPR6 [13]	PUPR6 [12]	PUPR6 [11]	PUPR6 [10]	PUPR6 [9]	PUPR6 [8]	PUPR6 [7]	PUPR6 [6]	PUPR6 [5]	PUPR6 [4]	PUPR6 [3]	PUPR6 [2]	PUPR6 [1]	PUPR6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR6[31:0]	H'F000 000F	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR6[31]	MSIOF0_RXD pin is pulled up
PUPR6[30]	MSIOF0_TXD pin is pulled up
PUPR6[29]	MSIOF0_SYNC pin is pulled up
PUPR6[28]	MSIOF0_SCK pin is pulled up
PUPR6[27]	SD3_WP pin is pulled up
PUPR6[26]	SD3_CD pin is pulled up
PUPR6[25]	SD3_DATA3 pin is pulled up
PUPR6[24]	SD3_DATA2 pin is pulled up
PUPR6[23]	SD3_DATA1 pin is pulled up
PUPR6[22]	SD3_DATA0 pin is pulled up
PUPR6[21]	SD3_CMD pin is pulled up
PUPR6[20]	SD3_CLK pin is pulled up
PUPR6[19]	SD2_WP pin is pulled up
PUPR6[18]	SD2_CD pin is pulled up
PUPR6[17]	SD2_DATA3 pin is pulled up
PUPR6[16]	SD2_DATA2 pin is pulled up
PUPR6[15]	SD2_DATA1 pin is pulled up
PUPR6[14]	SD2_DATA0 pin is pulled up
PUPR6[13]	SD2_CMD pin is pulled up
PUPR6[12]	SD2_CLK pin is pulled up
PUPR6[11]	SD0_WP pin is pulled up
PUPR6[10]	SD0_CD pin is pulled up
PUPR6[9]	SD0_DATA3 pin is pulled up
PUPR6[8]	SD0_DATA2 pin is pulled up
PUPR6[7]	SD0_DATA1 pin is pulled up

Bit Name	Set Value = 1
PUPR6[6]	SD0_DATA0 pin is pulled up
PUPR6[5]	SD0_CMD pin is pulled up
PUPR6[4]	SD0_CLK pin is pulled up
PUPR6[3]	STP_OPWM_0 pin is pulled up
PUPR6[2]	STP_ISSYNC_0 pin is pulled up
PUPR6[1]	STP_ISEN_0 pin is pulled up
PUPR6[0]	STP_ISD_0 pin is pulled up

5.3.38 LSI Pin Pull-Up Control Register 7 (PUPR7)

Function: PUPR7 performs on/off control of the pull-up/down* resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR7 [31]	PUPR7 [30]	PUPR7 [29]	PUPR7 [28]	PUPR7 [27]	PUPR7 [26]	PUPR7 [25]	PUPR7 [24]	PUPR7 [23]	PUPR7 [22]	PUPR7 [21]	PUPR7 [20]	PUPR7 [19]*	PUPR7 [18]	PUPR7 [17]	PUPR7 [16]
Initial value:	0	0	0	0	0	0	0	1	0	1	0	1	1	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR7 [15]	PUPR7 [14]	PUPR7 [13]	PUPR7 [12]	PUPR7 [11]	PUPR7 [10]	PUPR7 [9]	PUPR7 [8]	PUPR7 [7]	PUPR7 [6]	PUPR7 [5]	PUPR7 [4]	PUPR7 [3]	PUPR7 [2]	PUPR7 [1]	PUPR7 [0]
Initial value:	0	0	0	0	1	1	1	1	1	1	1	1	0	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR7[31:0]*	H'015C 0FF3	R/W	Performs individual on/off control of the pull-up/down* resistor provided in each signal pin of the LSI. 0: Pull-up/down function is disabled. 1: Pull-up/down function is enabled.

Note: * Only PUPR7[19] ACK pin is available for pull-down function.

Bit Name	Set Value = 1
PUPR7[31]	—
PUPR7[30]	—
PUPR7[29]	—
PUPR7[28]	—
PUPR7[27]	—
PUPR7[26]	AVS2 pin is pulled up
PUPR7[25]	AVS1 pin is pulled up
PUPR7[24]	USB1_OVC pin is pulled up
PUPR7[23]	USB1_PWEN pin is pulled up
PUPR7[22]	USB0_OVC pin is pulled up
PUPR7[21]	USB0_PWEN pin is pulled up
PUPR7[20]	CS0# pin is pulled up
PUPR7[19]	ACK is pulled down
PUPR7[18]	A25 pin is pulled up
PUPR7[17]	—
PUPR7[16]	—
PUPR7[15]	—
PUPR7[14]	HTX1 pin is pulled up
PUPR7[13]	HRX1 pin is pulled up
PUPR7[12]	HTX0 pin is pulled up
PUPR7[11]	HRX0 pin is pulled up
PUPR7[10]	HSCK0 pin is pulled up
PUPR7[9]	HRTS0# pin is pulled up
PUPR7[8]	HCTS0# pin is pulled up

Bit Name	Set Value = 1
PUPR7[7]	GPS_MAG pin is pulled up
PUPR7[6]	GPS_SIGN pin is pulled up
PUPR7[5]	GPS_CLK pin is pulled up
PUPR7[4]	SIM0_D pin is pulled up
PUPR7[3]	SIM0_CLK pin is pulled up
PUPR7[2]	SIM0_RST pin is pulled up
PUPR7[1]	MSIOF0_SS2 pin is pulled up
PUPR7[0]	MSIOF0_SS1 pin is pulled up

5.3.39 SD Control Register 0 (IOCTRL0)

Function: IOCTRL0 controls the driving abilities of pins in use for the SD0 interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	drv2_stpopwm	drv1_stpopwm	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	drv2_sd0wp	drv1_sd0wp	drv2_sd0cd	drv1_sd0cd	drv2_sd0clk	drv1_sd0clk	drv2_sd0cmd	drv1_sd0cmd	drv2_sd0d3	drv1_sd0d3	drv2_sd0d2	drv1_sd0d2	drv2_sd0d1	drv1_sd0d1	drv2_sd0d0	drv1_sd0d0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	drv2_stpopwm	1	R/W	STP_OPWM_0 Setting.
30	drv1_stpopwm	0	R/W	The value of these bits must be 10.
29 to 16	—	All 0	R/W	—
15	drv2_sd0wp	1	R/W	SD0_WP Setting.
14	drv1_sd0wp	1	R/W	The value of these bits must be 11.
13	drv2_sd0cd	1	R/W	SD0_CD Setting.
12	drv1_sd0cd	1	R/W	The value of these bits must be 11.
11	drv2_sd0clk	1	R/W	SD0_CLK Setting.
10	drv1_sd0clk	1	R/W	The value of these bits must be 11.
9	drv2_sd0cmd	1	R/W	SD0_CMD Setting.
8	drv1_sd0cmd	1	R/W	The value of these bits must be 11.
7	drv2_sd0d3	1	R/W	SD0_DATA3 Setting.
6	drv1_sd0d3	1	R/W	The value of these bits must be 11.
5	drv2_sd0d2	1	R/W	SD0_DATA2 Setting.
4	drv1_sd0d2	1	R/W	The value of these bits must be 11.
3	drv2_sd0d1	1	R/W	SD0_DATA1 Setting.
2	drv1_sd0d1	1	R/W	The value of these bits must be 11.
1	drv2_sd0d0	1	R/W	SD0_DATA0 Setting.
0	drv1_sd0d0	1	R/W	The value of these bits must be 11.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.40 SD Control Register 1 (IOCTRL1)

Function: IOCTRL1 controls the driving abilities of pins in use for the SD2 and SD3 interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	drv2_sd2wp	drv1_sd2wp	drv2_sd2cd	drv1_sd2cd	drv2_sd2clk	drv1_sd2clk	drv2_sd2cmd	drv1_sd2cmd	drv2_sd2d3	drv1_sd2d3	drv2_sd2d2	drv1_sd2d2	drv2_sd2d1	drv1_sd2d1	drv2_sd2d0	drv1_sd2d0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	drv2_sd3wp	drv1_sd3wp	drv2_sd3cd	drv1_sd3cd	drv2_sd3clk	drv1_sd3clk	drv2_sd3cmd	drv1_sd3cmd	drv2_sd3d3	drv1_sd3d3	drv2_sd3d2	drv1_sd3d2	drv2_sd3d1	drv1_sd3d1	drv2_sd3d0	drv1_sd3d0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	drv2_sd2wp	1	R/W	SD2_WP Setting.
30	drv1_sd2wp	1	R/W	The value of these bits must be 11.
29	drv2_sd2cd	1	R/W	SD2_CD Setting.
28	drv1_sd2cd	1	R/W	The value of these bits must be 11.
27	drv2_sd2clk	1	R/W	SD2_CLK Setting.
26	drv1_sd2clk	1	R/W	The value of these bits must be 11.
25	drv2_sd2cmd	1	R/W	SD2_CMD Setting.
24	drv1_sd2cmd	1	R/W	The value of these bits must be 11.
23	drv2_sd2d3	1	R/W	SD2_DATA3 Setting.
22	drv1_sd2d3	1	R/W	The value of these bits must be 11.
21	drv2_sd2d2	1	R/W	SD2_DATA2 Setting.
20	drv1_sd2d2	1	R/W	The value of these bits must be 11.
19	drv2_sd2d1	1	R/W	SD2_DATA1 Setting.
18	drv1_sd2d1	1	R/W	The value of these bits must be 11.
17	drv2_sd2d0	1	R/W	SD2_DATA0 Setting.
16	drv1_sd2d0	1	R/W	The value of these bits must be 11.
15	drv2_sd3wp	1	R/W	SD3_WP Setting.
14	drv1_sd3wp	1	R/W	The value of these bits must be 11.
13	drv2_sd3cd	1	R/W	SD3_CD Setting.
12	drv1_sd3cd	1	R/W	The value of these bits must be 11.
11	drv2_sd3clk	1	R/W	SD3_CLK Setting.
10	drv1_sd3clk	1	R/W	The value of these bits must be 11.
9	drv2_sd3cmd	1	R/W	SD3_CMD Setting.
8	drv1_sd3cmd	1	R/W	The value of these bits must be 11.
7	drv2_sd3d3	1	R/W	SD3_DATA3 Setting.
6	drv1_sd3d3	1	R/W	The value of these bits must be 11.
5	drv2_sd3d2	1	R/W	SD3_DATA2 Setting.
4	drv1_sd3d2	1	R/W	The value of these bits must be 11.
3	drv2_sd3d1	1	R/W	SD3_DATA1 Setting.
2	drv1_sd3d1	1	R/W	The value of these bits must be 11.

Bit	Bit Name	Initial Value	R/W	Description
1	drv2_sd3d0	1	R/W	SD3_DATA0 Setting.
0	drv1_sd3d0	1	R/W	The value of these bits must be 11.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.41 TDSEL Control Register 4 (IOCTRL4)

Function: IOCTRL4 controls the delay of returned clock of in pins of IRQ, DU and Ethernet interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	irq5_tdsel1	irq5_tdsel0	du1dr0_tdsel1	du1dr0_tdsel0	—	—	—	—	—	—	ethlink_tdsel1	ethlink_tdsel0	stpisclk_tdsel1	stpisclk_tdsel0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R/W	—
13	irq5_tdsel1	0	R/W	IRQ5 Setting:
12	irq5_tdsel0	0	R/W	The value of these bits must be 00.
11	du1dr0_tdsel1	0	R/W	DU1_DR0 Setting:
10	du1dr0_tdsel0	0	R/W	The value of these bits must be 00.
9 to 4	—	All 0	R/W	—
3	ethlink_tdsel1	0	R/W	ETH_LINK Setting:
2	ethlink_tdsel0	0	R/W	The value of these bits must be 00.
1	stpisclk_tdsel1	0	R/W	STP_ISCLK_0 Setting:
0	stpisclk_tdsel0	0	R/W	The value of these bits must be 00.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.42 TDSEL Control Register 5 (IOCTRL5)

Function: IOCTRL5 controls the delay of returned clock in pins of SDHI, LBSC, SSI and ADG interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	audio_tdsel1	audio_tdsel0	ssisck5_tdsel1	ssisck5_tdsel0	ssisdat4_tdsel1	ssisdat4_tdsel0	ssisdat0_tdsel1	ssisdat0_tdsel0	excs1_tdsel1	excs1_tdsel0	sd0tdsel1	sd0tdsel0	sd2tdsel1	sd2tdsel0	sd3tdsel1	sd3tdsel0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	a0_tdsel1	a0_tdsel0	—	—	a12_tdsel1	a12_tdsel0	—	—	—	—	—	—	—	—	a6_tdsel1	a6_tdsel0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	audio_tdsel1	0	R/W	AUDIO_CLKB Setting:
30	audio_tdsel0	0	R/W	The setting value of these bits must be 00.
29	ssisck5_tdsel1	0	R/W	SSI_SCK5 Setting:
28	ssisck5_tdsel0	0	R/W	The setting value of these bits must be 00.
27	ssisdat4_tdsel1	0	R/W	SSI_SDATA4 Setting:
26	ssisdat4_tdsel0	0	R/W	The setting value of these bits must be 00.
25	ssisdat0_tdsel1	0	R/W	SSI_SDATA0 Setting:
24	ssisdat0_tdsel0	0	R/W	The setting value of these bits must be 00.
23	excs1_tdsel1	0	R/W	EX_CS1# Setting:
22	excs1_tdsel0	0	R/W	The setting value of these bits must be 00.
21	sd0tdsel1	0	R/W	SD0_CLK Setting 2:
20	sd0tdsel0	0	R/W	The setting value of these bits must be 00.
19	sd2tdsel1	0	R/W	SD2_CLK Setting 2:
18	sd2tdsel0	0	R/W	The setting value of these bits must be 00.
17	sd3tdsel1	0	R/W	SD3_CLK Setting 2:
16	sd3tdsel0	0	R/W	The setting value of these bits must be 00.
15	a0_tdsel1	0	R/W	A0 Setting:
14	a0_tdsel0	0	R/W	The setting value of these bits must be 00.
13, 12	—	All 0	R/W	—
11	a12_tdsel1	0	R/W	A12 Setting:
10	a12_tdsel0	0	R/W	The setting value of these bits must be 00.
9 to 2	—	All 0	R/W	—
1	a6_tdsel1	0	R/W	A6 Setting:
0	a6_tdsel0	0	R/W	The setting value of these bits must be 00.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.43 SD Control Register 6 (IOCTRL6)

Function: IOCTRL6 controls the IO voltage of pins in use for the SD interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	poc_sd 0clk	poc_sd 0cmd	poc_sd 0dat0	poc_sd 0dat1	poc_sd 0dat2	poc_sd 0dat3	poc_sd 0cd	poc_sd 0wp	poc_sd 2clk	poc_sd 2cmd	poc_sd 2dat0	poc_sd 2dat1	poc_sd 2dat2	poc_sd 2dat3	poc_sd 2cd	poc_sd 2wp
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	poc_sd 3clk	poc_sd 3cmd	poc_sd 3dat0	poc_sd 3dat1	poc_sd 3dat2	poc_sd 3dat3	poc_sd 3cd	poc_sd 3wp	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	poc_sd0clk	1	R/W	Selecting IO voltage for the pin SD0_CLK 0: 1.8 V 1: 3.3 V
30	poc_sd0cmd	1	R/W	Selecting IO voltage for the pin SD0_CMD 0: 1.8 V 1: 3.3 V
29	poc_sd0dat0	1	R/W	Selecting IO voltage for the pin SD0_DATA0 0: 1.8 V 1: 3.3 V
28	poc_sd0dat1	1	R/W	Selecting IO voltage for the pin SD0_DATA1 0: 1.8 V 1: 3.3 V
27	poc_sd0dat2	1	R/W	Selecting IO voltage for the pin SD0_ DATA2 0: 1.8 V 1: 3.3 V
26	poc_sd0dat3	1	R/W	Selecting IO voltage for the pin SD0_ DATA3 0: 1.8 V 1: 3.3 V
25	poc_sd0cd	1	R/W	Selecting IO voltage for the pin SD0_CD 0: 1.8 V 1: 3.3 V
24	poc_sd0wp	1	R/W	Selecting IO voltage for the pin SD0_WP 0: 1.8 V 1: 3.3 V
23	poc_sd2clk	1	R/W	Selecting IO voltage for the pin SD2_CLK 0: 1.8 V 1: 3.3 V
22	poc_sd2cmd	1	R/W	Selecting IO voltage for the pin SD2_CMD 0: 1.8 V 1: 3.3 V
21	poc_sd2dat0	1	R/W	Selecting IO voltage for the pin SD2_DATA0 0: 1.8 V 1: 3.3 V

Bit	Bit Name	Initial Value	R/W	Description
20	poc_sd2dat1	1	R/W	Selecting IO voltage for the pin SD2_DATA1 0: 1.8 V 1: 3.3 V
19	poc_sd2dat2	1	R/W	Selecting IO voltage for the pin SD2_DATA2 0: 1.8 V 1: 3.3 V
18	poc_sd2dat3	1	R/W	Selecting IO voltage for the pin SD2_DATA3 0: 1.8 V 1: 3.3 V
17	poc_sd2cd	1	R/W	Selecting IO voltage for the pin SD2_CD 0: 1.8 V 1: 3.3 V
16	poc_sd2wp	1	R/W	Selecting IO voltage for the pin SD2_WP 0: 1.8 V 1: 3.3 V
15	poc_sd3clk	1	R/W	Selecting IO voltage for the pin SD3_CLK 0: 1.8 V 1: 3.3 V
14	poc_sd3cmd	1	R/W	Selecting IO voltage for the pin SD3_CMD 0: 1.8 V 1: 3.3 V
13	poc_sd3dat0	1	R/W	Selecting IO voltage for the pin SD3_DATA0 0: 1.8 V 1: 3.3 V
12	poc_sd3dat1	1	R/W	Selecting IO voltage for the pin SD3_DATA1 0: 1.8 V 1: 3.3 V
11	poc_sd3dat2	1	R/W	Selecting IO voltage for the pin SD3_DATA2 0: 1.8 V 1: 3.3 V
10	poc_sd3dat3	1	R/W	Selecting IO voltage for the pin SD3_DATA3 0: 1.8 V 1: 3.3 V
9	poc_sd3cd	1	R/W	Selecting IO voltage for the pin SD3_CD 0: 1.8 V 1: 3.3 V
8	poc_sd3wp	1	R/W	Selecting IO voltage for the pin SD3_WP 0: 1.8 V 1: 3.3 V
7 to 0	—	All 0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.44 IIC3 (DVFS) and TDBG IO Cell Control Register (IOCTRL7)

Function: IOCTRL controls the driving abilities of pins in use for the IIC and IIC3 (DVFS) interfaces. This register is internal use and reserved; the value of this register should not be changed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

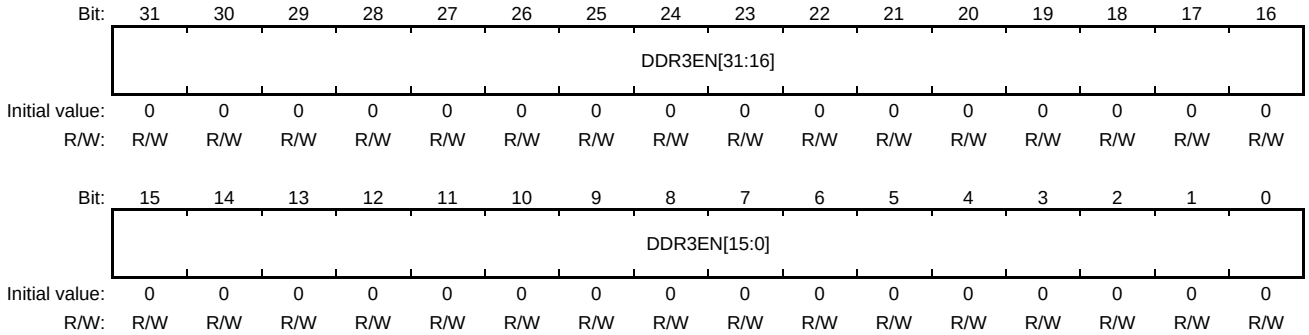
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	gpreg_msel03_p	—	—	—	—	conta_IIC3(DVFS)	contb_IIC3(DVFS)	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R/W	—
12	gpreg_msel03_p	0	R/W	Debug monitor function: 0: Use DU pins for debug monitor function. 1: Use SDHI pins for debug monitor function.
11 to 8	—	All 0	R/W	—
7	conta_IIC3(DVFS)	0	R/W	The setting value of these bits must be 00.
6	contb_IIC3(DVFS)	0	R/W	
5 to 0	—	All 0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.45 DDR3 General Port IO Enable Register (DDR3GPEN)

Function: DDR3GPEN is used to write values to enable DDR3 general port function.

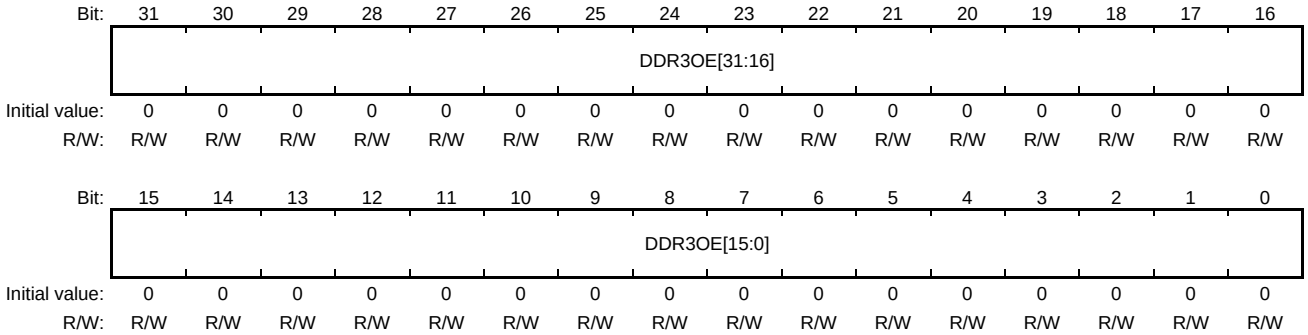


Bit	Bit Name	Initial Value	R/W	Description
31, 30	DDR3EN[31:30]	00	R/W	—
29 to 1	DDR3EN[29:1]	0	R/W	For enabling DDR3 general port function bit 29 to 1: 0: Disabled. 1: Enabled.
0	DDR3EN[0]	0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.46 DDR3 General Port Output Enable Register (DDR3GPOE)

Function: DDR3GPOE is use to enable output of DDR3 general port function.



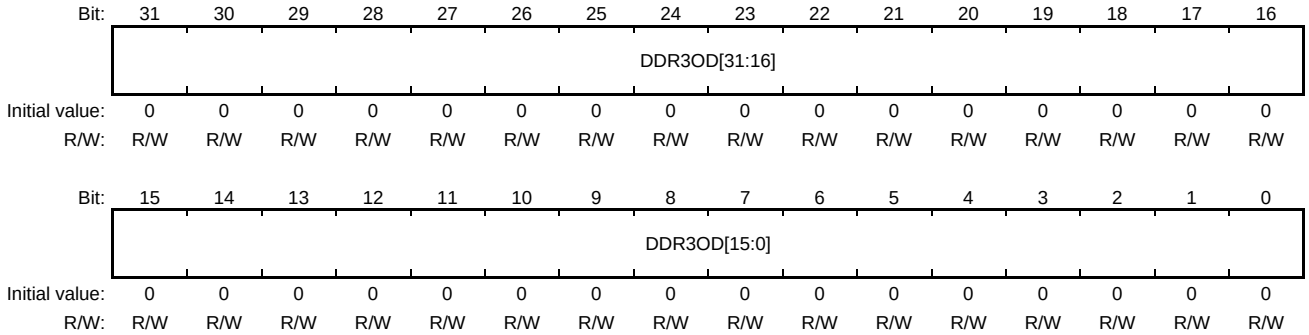
Bit	Bit Name	Initial Value	R/W	Description
31	DDR3OE[31]	0	R/W	—
30	DDR3OE[30]	0	R/W	—
29	DDR3OE[29]	0	R/W	Enabling output of DDR3 general port function bit 29 0: Disabled. 1: Enabled.
28	DDR3OE[28]	0	R/W	—
27	DDR3OE[27]	0	R/W	—
26	DDR3OE[26]	0	R/W	Enabling output of DDR3 general port function bit 26 0: Disabled. 1: Enabled.
25	DDR3OE[25]	0	R/W	—
24	DDR3OE[24]	0	R/W	Enabling output of DDR3 general port function bit 24 0: Disabled. 1: Enabled.
23	DDR3OE[23]	0	R/W	—
22	DDR3OE[22]	0	R/W	—
21	DDR3OE[21]	0	R/W	Enabling output of DDR3 general port function bit 21 0: Disabled. 1: Enabled.
20	DDR3OE[20]	0	R/W	Enabling output of DDR3 general port function bit 20 0: Disabled. 1: Enabled.
19	DDR3OE[19]	0	R/W	Enabling output of DDR3 general port function bit 19 0: Disabled. 1: Enabled.
18	DDR3OE[18]	0	R/W	—
17	DDR3OE[17]	0	R/W	Enabling output of DDR3 general port function bit 17 0: Disabled. 1: Enabled.

Bit	Bit Name	Initial Value	R/W	Description
16	DDR3OE[16]	0	R/W	Enabling output of DDR3 general port function bit 16 0: Disabled. 1: Enabled.
15	DDR3OE[15]	0	R/W	Enabling output of DDR3 general port function bit 15 0: Disabled. 1: Enabled.
14	DDR3OE[14]	0	R/W	—
13	DDR3OE[13]	0	R/W	—
12	DDR3OE[12]	0	R/W	Enabling output of DDR3 general port function bit 12 0: Disabled. 1: Enabled.
11	DDR3OE[11]	0	R/W	Enabling output of DDR3 general port function bit 11 0: Disabled. 1: Enabled.
10	DDR3OE[10]	0	R/W	—
9	DDR3OE[9]	0	R/W	Enabling output of DDR3 general port function bit 9 0: Disabled. 1: Enabled.
8	DDR3OE[8]	0	R/W	—
7	DDR3OE[7]	0	R/W	Enabling output of DDR3 general port function bit 7 0: Disabled. 1: Enabled.
6	DDR3OE[6]	0	R/W	—
5	DDR3OE[5]	0	R/W	—
4	DDR3OE[4]	0	R/W	—
3	DDR3OE[3]	0	R/W	Enabling output of DDR3 general port function bit 3 0: Disabled. 1: Enabled.
2	DDR3OE[2]	0	R/W	Enabling output of DDR3 general port function bit 2 0: Disabled. 1: Enabled.
1	DDR3OE[1]	0	R/W	Enabling output of DDR3 general port function bit 1 0: Disabled. 1: Enabled.
0	DDR3OE[0]	0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.47 DDR3 General Port Output Data Register (DDR3GPOD)

Function: DDR3GPOD is use to write data to DDR3 general port.



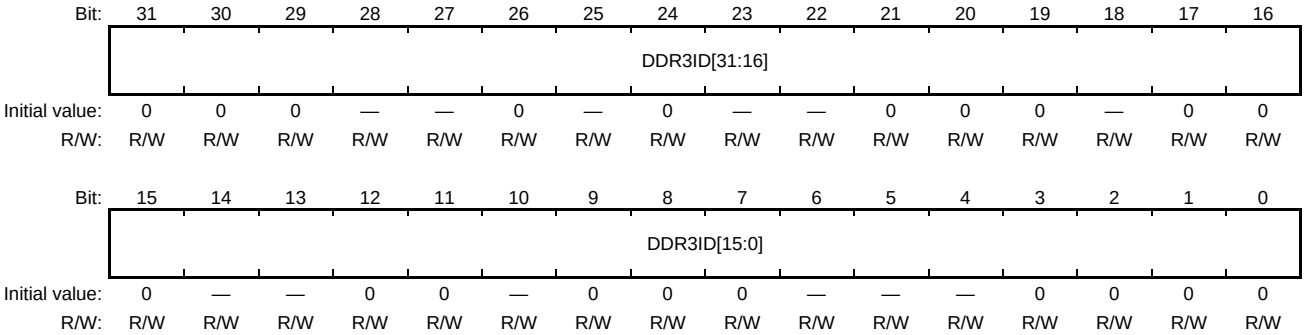
Bit	Bit Name	Initial Value	R/W	Description
31	DDR3OD[31]	0	R/W	—
30	DDR3OD[30]	0	R/W	—
29	DDR3OD[29]	0	R/W	For writing values to DDR3 general port bit 29
28	DDR3OD[28]	0	R/W	—
27	DDR3OD[27]	0	R/W	—
26	DDR3OD[26]	0	R/W	For writing values to DDR3 general port bit 26
25	DDR3OD[25]	0	R/W	—
24	DDR3OD[24]	0	R/W	For writing values to DDR3 general port bit 24
23	DDR3OD[23]	0	R/W	—
22	DDR3OD[22]	0	R/W	—
21	DDR3OD[21]	0	R/W	For writing values to DDR3 general port bit 21
20	DDR3OD[20]	0	R/W	For writing values to DDR3 general port bit 20
19	DDR3OD[19]	0	R/W	For writing values to DDR3 general port bit 19
18	DDR3OD[18]	0	R/W	—
17	DDR3OD[17]	0	R/W	For writing values to DDR3 general port bit 17
16	DDR3OD[16]	0	R/W	For writing values to DDR3 general port bit 16
15	DDR3OD[15]	0	R/W	For writing values to DDR3 general port bit 15
14	DDR3OD[14]	0	R/W	—
13	DDR3OD[13]	0	R/W	—
12	DDR3OD[12]	0	R/W	For writing values to DDR3 general port bit 12
11	DDR3OD[11]	0	R/W	For writing values to DDR3 general port bit 11
10	DDR3OD[10]	0	R/W	—
9	DDR3OD[9]	0	R/W	For writing values to DDR3 general port bit 9
8	DDR3OD[8]	0	R/W	—
7	DDR3OD[7]	0	R/W	For writing values to DDR3 general port bit 7
6	DDR3OD[6]	0	R/W	—
5	DDR3OD[5]	0	R/W	—
4	DDR3OD[4]	0	R/W	—
3	DDR3OD[3]	0	R/W	For writing values to DDR3 general port bit 3
2	DDR3OD[2]	0	R/W	For writing values to DDR3 general port bit 2

Bit	Bit Name	Initial Value	R/W	Description
1	DDR3OD[1]	0	R/W	For writing values to DDR3 general port bit 1
0	DDR3OD[0]	0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.48 DDR3 General Port Input Data Register (DDR3GPID)

Function: DDR3GPID is use to read input data from DDR3 general port.



Bit	Bit Name	Initial Value	R/W	Description
31	DDR3ID[31]	0	R	—
30	DDR3ID[30]	0	R	—
29	DDR3ID[29]	0	R	—
28	DDR3ID[28]	—	R	Indicating values from DDR3 general port bit 28
27	DDR3ID[27]	—	R	Indicating values from DDR3 general port bit 27
26	DDR3ID[26]	0	R	—
25	DDR3ID[25]	—	R	Indicating values from DDR3 general port bit 25
24	DDR3ID[24]	0	R	—
23	DDR3ID[23]	—	R	Indicating values from DDR3 general port bit 23
22	DDR3ID[22]	—	R	Indicating values from DDR3 general port bit 22
21	DDR3ID[21]	0	R	—
20	DDR3ID[20]	0	R	—
19	DDR3ID[19]	0	R	—
18	DDR3ID[18]	—	R	Indicating values from DDR3 general port bit 18
17	DDR3ID[17]	0	R	—
16	DDR3ID[16]	0	R	—
15	DDR3ID[15]	0	R	—
14	DDR3ID[14]	—	R	Indicating values from DDR3 general port bit 14
13	DDR3ID[13]	—	R	Indicating values from DDR3 general port bit 13
12	DDR3ID[12]	0	R	—
11	DDR3ID[11]	0	R	—
10	DDR3ID[10]	—	R	Indicating values from DDR3 general port bit 10
9	DDR3ID[9]	0	R	—
8	DDR3ID[8]	—	R	Indicating values from DDR3 general port bit 8
7	DDR3ID[7]	0	R	—
6	DDR3ID[6]	—	R	Indicating values from DDR3 general port bit 6
5	DDR3ID[5]	—	R	Indicating values from DDR3 general port bit 5
4	DDR3ID[4]	—	R	Indicating values from DDR3 general port bit 4
3	DDR3ID[3]	0	R	—
2	DDR3ID[2]	0	R	—
1	DDR3ID[1]	0	R	—

Bit	Bit Name	Initial Value	R/W	Description
0	DDR3ID[0]	0	R	—

5.4 Operation

5.4.1 Function Setting for Multiplexed Pins

Setting the LSI multiplexed pin setting mask register (PMMR) is necessary before setting each of the GPIO/peripheral function select registers 0 to 7 (GPSR0 to GPSR7) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16). Specifically, the inverse of the value to be set in the select register must be written to the LSI multiplexed pin setting mask register. Otherwise, the GPIO/peripheral function select registers 0 to 7 (GPSR0 to GPSR7) and peripheral function select registers 0 to 16 (IPSR0 to IPSR16) cannot be set. IPSR0 to IPSR16, MOD_SEL and MOD_SEL2 to MOD_SEL4 registers shall be set before setting GPSR0 to GPSR7 registers in case that they need to be configured. MOD_SEL and MOD_SEL2 to MOD_SEL4 registers can be set either earlier or later than setting IPSR0 to IPSR16 registers.

Note: When GPIO is selected by GPSRn for an LSI pin and one of the below pin functions is selected by IPSRn, make sure to disable data reception of SCIFA3/4/5.

LSI Pin	Pin Function
DU1_DB6	SCIFA3_RXD
ETH_REFCLK	SCIFA3_RXD_B
GPS_MAG	SCIFA4_RXD_C
GPS_SIGN	SCIFA3_RXD_C
SD0_WP	SCIFA5_RXD_B
SD3_WP	SCIFA5_RXD_C
VI0_FIELD	SCIFA4_RXD
VI0_VSYNC#	SCIFA5_RXD
VI1_VSYNC#	SCIFA4_RXD_B

(1) Procedure for changing pin function from GPIO to peripheral function

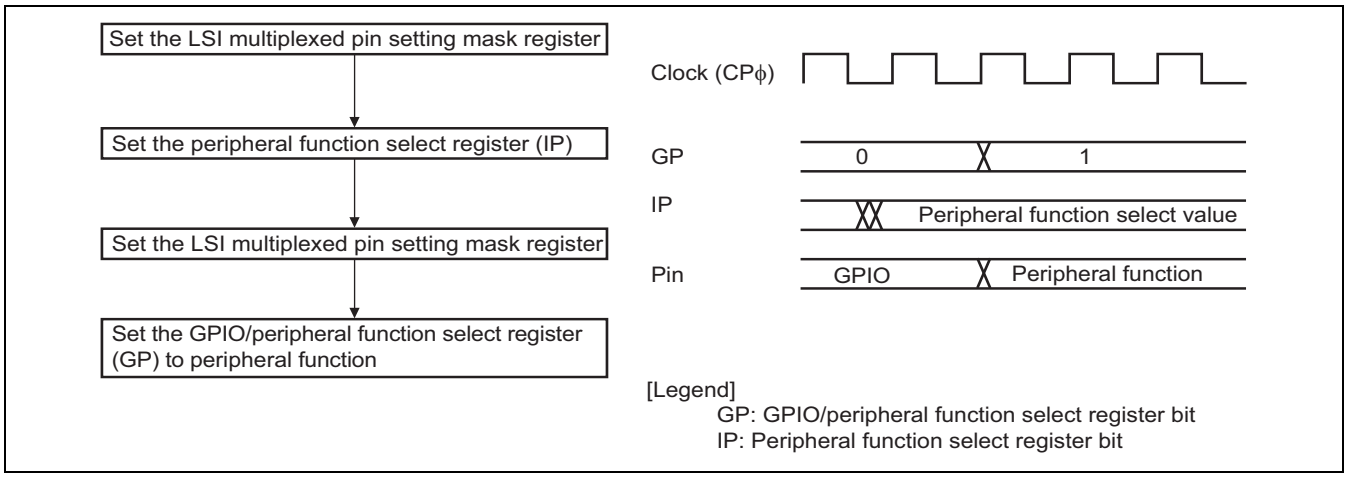


Figure 5.1 Procedure for Changing Pin Function from GPIO to Peripheral Function

(2) Procedure for changing pin function from peripheral function to GPIO

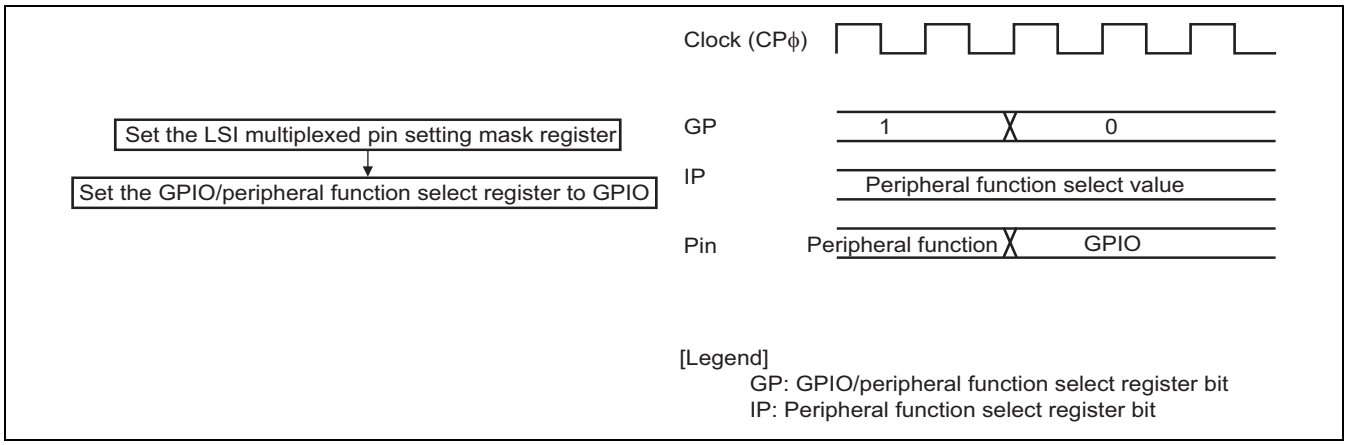


Figure 5.2 Procedure for Changing Pin Function from Peripheral function to GPIO

When changing pin function from peripheral function to GPIO of LSI pin in the below list, make sure to disable the data reception of corresponding SCIFAn channel before performing the sequence in the Figure 5.2.

LSI Pin	Pin Function
DU1_DB6	SCIFA3_RXD
ETH_REFCLK	SCIFA3_RXD_B
GPS_MAG	SCIFA4_RXD_C
GPS_SIGN	SCIFA3_RXD_C
SD0_WP	SCIFA5_RXD_B
SD3_WP	SCIFA5_RXD_C
VI0_FIELD	SCIFA4_RXD_
VI0_VSYNC#	SCIFA5_RXD
VI1_VSYNC#	SCIFA4_RXD_B

(3) Procedure 1 for changing pin function from one peripheral function to another peripheral function

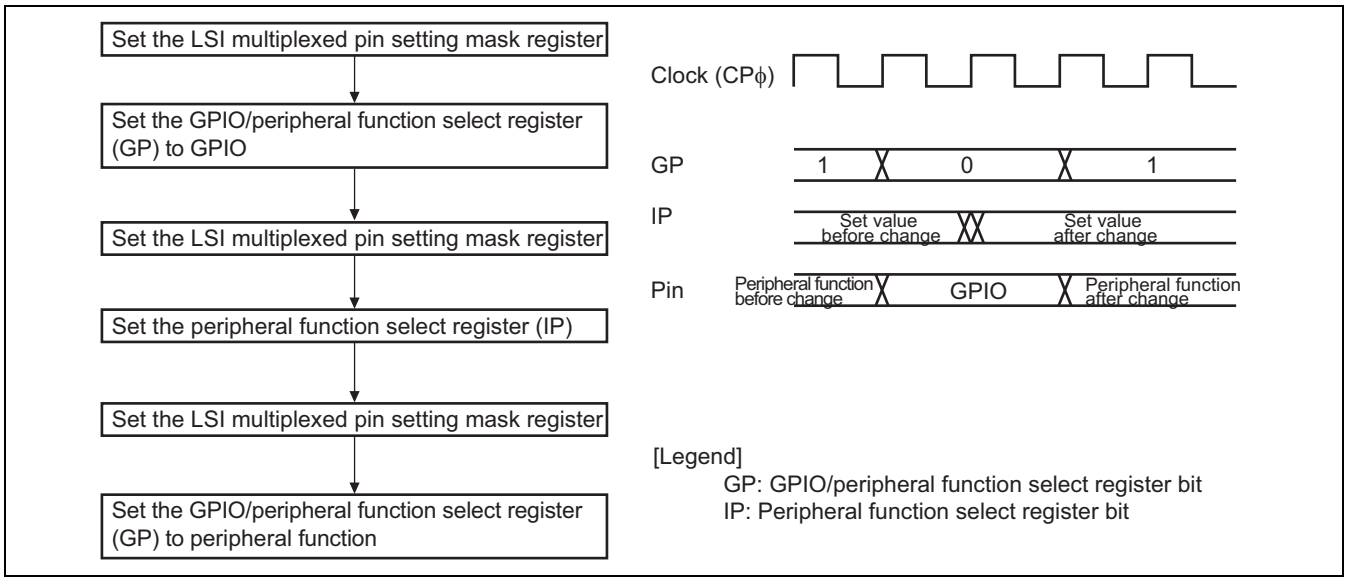


Figure 5.3 Procedure for Changing Pin Function from One Peripheral Function to Another Peripheral Function (with GPIO Setting)

In case that one of the pin function in the following list is selected, make sure to disable the data reception of corresponding SCIFAn channel before performing the sequence in the Figure 5.3.

LSI Pin	Pin Function
DU1_DB6	SCIFA3_RXD
ETH_REFCLK	SCIFA3_RXD_B
GPS_MAG	SCIFA4_RXD_C
GPS_SIGN	SCIFA3_RXD_C
SD0_WP	SCIFA5_RXD_B
SD3_WP	SCIFA5_RXD_C
VI0_FIELD	SCIFA4_RXD
VI0_VSYNC#	SCIFA5_RXD
VI1_VSYNC#	SCIFA4_RXD_B

5.4.2 Setting Pull-Up/Down Resistors

The LSI pin pull-up/down control registers 0 to 7 (PUPR0 to PUPR7) are used to switch the pull-up/down resistors on and off.

Main Revisions and Additions in this Edition

Minor revisions such as corrections of errors in spelling and modifications of wording are not included in the revision history.

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	Page	Contents	Summary
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