Mask Set Errata for Mask 0N36F

Introduction

This report applies to mask 0N36F for these products:

- S08PA4

Errata ID	Errata Title
5264	DBG: Comparator C with TAG type can not generate breakpoint when setting breakpoint at the address other than instruction opcode address
5265	DBG: DGB can not store data into FIFO when writing data to RAM and/or flash space at Event B only trigger mode or A then event only B trigger mode
5266	DBG: source address of BSR instruction stored in FIFO instead of the destination address
6251	NVM: flash commands might not run due to an unexpected protection violation
6245	NVM: flash protection issue affecting program flash command
5288	ICS: ICS_S[LOCK] flag not set after wakeup from stop mode when BDM mode is enabled
4592	PMC: Unstable to wake up MCU from stop3 mode with LVD disabled when the MCU power supply VDD is in the low range
4567	PMC: higher stop3 IDD after power on reset
7331	IO: High current drive pins not in high-Z state during power up
7040	SOC: Slow VDD ramp-up might cause unstable startup on some devices during power up at cold temperatures
6657	ADC: ADC FIFO not working when the bus clock is slower than ADC clock divided by 2

e5264: DBG: Comparator C with TAG type can not generate breakpoint when setting breakpoint at the address other than instruction opcode address

Errata type: Errata

Description: When setting breakpoint at the address other than instruction opcode address, the comparator C with TAG type can not generate breakpoint. This issue does not affect code execution.

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Workaround: If such tag breakpoint at the address other than instruction opcode address is required, use comparator A and/or B tag breakpoint.

e5265: DBG: DGB can not store data into FIFO when writing data to RAM and/or flash space at Event B only trigger mode or A then event only B trigger mode

Errata type: Errata

Description: When Event B only trigger mode or A then event only B trigger mode is used, the DGB can not store data into FIFO when writing data to RAM and/or flash memory space (i.e.,DBG_CBH,DBG_CBL point to RAM or Flash address). But when the compare bits in DBG_CBH,DBG_CBL point to register, it works well.

Workaround: No workaround

e5266: DBG: source address of BSR instruction stored in FIFO instead of the destination address

Errata type: Errata

Description: In COF storing mode, the address stored in FIFO for a BSR instruction is the source address instead of the destination address.

Workaround: No workaround.

e6251: FTMRH P-Flash commands might not run due to an unexpected Protection violation

Errata type: Errata

Description: For the P-Flash sizes of 4K, 8K or 16K, in the protection scenario 1, if bits FPHS[1:0] are set to '11' the user might expect that it would behave the same as scenario 7 (P-Flash fully unprotected). However, in such a configuration in scenario 1 the commands that affect the whole P-Flash array (ERSBLK, ERSALL, UNSECU) will not execute and flag PVIOL will set indicating a protection violation.

For the greater P-Flash sizes (64K or 32K) this configuration does not result in the P-Flash fully unprotected, so this errata does not apply for those sizes. In this case these commands would run only if P-Flash protection is configured to scenario 7 (fully unprotected).

Workaround: In order to launch the commands that affect the whole P-Flash array protection must be set according to scenario 7 (P-Flash fully unprotected).

e6245: FTMRH P-Flash protection issue affecting command PGM

Errata type: Errata

Description: There is a problem affecting command PGM in a scenario where the P-Flash is partially protected.

When command PGM is used to program 8-bytes, starting from the address that corresponds to the last 4-bytes in the P-Flash unprotected region (therefore crossing the boundary into the protected region), the PGM command will program the full set of 8 bytes: 4 bytes in the unprotected region and the next 4 bytes in the protected region, what results in an undetected protection violation.

Workaround: The application should launch command PGM to program 4-bytes or 8-bytes to correctly match the limits of the P-Flash unprotected region, not forcing the transition from the unprotected to the protected region as explained above.

e5288: ICS: ICS_S[LOCK] flag not set after wakeup from stop mode when BDM mode is enabled

Errata type: Errata

Description: ICS_S[LOCK] flag can not be set after wakeup from stop mode when BDM mode is enabled. This can be observed during code debugging with CodeWarrior when the debugger wakes up MCU via BDM. It does not affect code standalone execution.

Workaround: Perform two writes after wakeup from stop mode before checking LOCK flag:

1) write a different trim value than the manufacture default trim value to ICS_C3. The recommended value is default trim value + 1 or -1.

2) write the manufacture default trim value to ICS_C3.

e4592: PMC: Unstable to wake up MCU from stop3 mode with LVD disabled when the MCU power supply VDD is in the low range

Errata type: Errata

Description: The PMC does not provide enough current while waking up MCU from stop3 mode if the MCU power supply VDD is in the low range. If LVD enabled with LVDRE bit set and LVDSE bit clear, the LVD reset may occur with high MCU power supply VDD. The observed VDD can be as high as 4V when LVD reset on wakeup happens.

Workaround: The low power stop3 mode can only be used at VDD from 5V down to the high LVD trip (VLVDH) safely (4.2V to 5.5V). The low power stop3 mode cannot be used from 2.7V to 4.2V. High power stop3 mode (both LVDE bit and LVDSE bit set) can still be used for lower voltage applications.

It'll be fixed in future silicon revision.

e4567: PMC: higher stop3 IDD after power on reset

Errata type: Errata

Description: Abnormal high stop current is observed at cold temperature after power-on reset. It will take 1-2 seconds for stop current to drop to normal value (~3uA typical) from 100+uA at room temperature, 20 seconds at -20°C, up to a few minutes at -40°C. It will not be observed at hot temperature.

This issue does not affect applications which do not require stop3 mode. It'll be fixed in future silicon revision.

Workaround: It'll be fixed in future silicon revision.

e7331: IO: High current drive pins not in high-Z state during power up

Errata type: Errata

Description: The high current drive pins on the chip are unexpectedly driven low for a short period during power up. All other I/O pins are high impedance. The issue happens only before VDD reaches the power-on reset voltage. After power up the normal I/O functions on the high current drive pins are not impacted.

Workaround: Use one or more combination of the following methods to avoid possible issues:

- Use high current drive pins as current source for LED connection, but keep total IDD < 120mA (refer to device data sheet for IDD)
- Configure the corresponding Flextimer channel output polarity as active high which are muxed with high current drive pins
- Use high current drive pins with NPN transistor (active high) to drive relays
- Keep VDD ramp-up time greater than or equal to 1KV/s and less than or equal to 10KVs to disable LED and/or driver action during power up

e7040: SOC: Slow VDD ramp-up might cause unstable startup on some devices during power up at cold temperatures

Errata type: Errata

Description: Some devices may not start up when both conditions are met: cold temperature (between -40°C and about -20°C) and slow VDD ramp up time (less than or equal to 900 V/s). The unstable startup is occasional and recoverable after an uncertain period of time.

Workaround: In order to avoid such startup issue either of these conditions shall be met:

- Temperature above -20°C;
- VDD ramp up time >=1K V/s and <= 10K V/s

This erratum will be fixed in the next revision.

e6657: ADC: ADC FIFO not working when the bus clock is slower than ADC clock divided by 2

Errata type: Errata

Description: When the ADC FIFO mode is enabled, the FIFO can not get correct result if the bus clock is slower than ADC conversion clock divided by 2.

Workaround: Configure the bus clock to be faster than the ADC conversion clock (ADCK) divided by 2 if the ADC FIFO is used.

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