

CD4023BC Buffered Triple 3-Input NAND Gate

General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS} .

Features

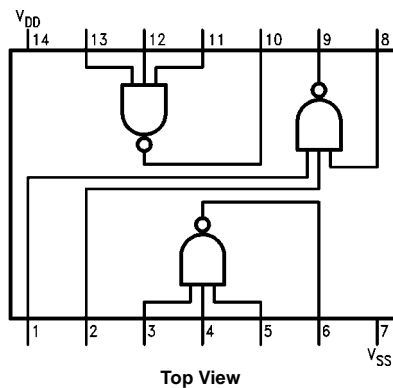
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: $0.45 V_{DD}$ (typ)
- Low power TTL compatibility:
fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage $1 \mu\text{A}$ at 15V over full temperature range

Ordering Code:

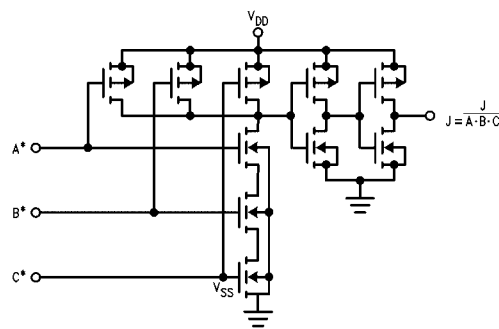
| Order Number | Package Number | Package Description |
|-----------------------|----------------|--|
| CD4023BCM (Note 1) | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4023BCSJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| CD4023BCN | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Note 1: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Block Diagram



$\frac{1}{3}$ Device Shown

*All Inputs Protected by Standard CMOS Input Protection Circuit.

Absolute Maximum Ratings (Note 2)

(Note 3)

| | |
|--------------------------------|--------------------------------------|
| DC Supply Voltage (V_{DD}) | -0.5 V_{DC} to +18 V_{DC} |
| Input Voltage (V_{IN}) | -0.5 V_{DC} to $V_{DD}+0.5 V_{DC}$ |
| Storage Temp. Range (T_S) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions

| | |
|---------------------------------------|-------------------------------|
| DC Supply Voltage (V_{DD}) | 5 V_{DC} to 15 V_{DC} |
| Input Voltage (V_{IN}) | 0 V_{DC} to $V_{DD} V_{DC}$ |
| Operating Temperature Range (T_A) | -55°C to +125°C |

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 3: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | -55°C | | +25°C | | | +125°C | | Units |
|----------|---------------------------------------|------------------------------|-------|------|-------|------------|------|--------|------|---------|
| | | | Min | Typ | Min | Typ | Max | Min | Max | |
| I_{DD} | Quiescent Device Current | $V_{DD} = 5V$ | | 0.25 | | 0.004 | 0.25 | | 7.5 | μA |
| | | $V_{DD} = 10V$ | | 0.5 | | 0.005 | 0.5 | | 15 | |
| | | $V_{DD} = 15V$ | | 1.0 | | 0.006 | 1.0 | | 30 | |
| V_{OL} | LOW Level Output Voltage | $V_{DD} = 5V$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD} = 10V$ | | 0.05 | | 0 | 0.05 | | 0.05 | |
| | | $V_{DD} = 15V$ | | 0.05 | | 0 | 0.05 | | 0.05 | |
| V_{OH} | HIGH Level Output Voltage | $V_{DD} = 5V$ | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | $V_{DD} = 10V$ | 9.95 | | 9.95 | 10 | | 9.95 | | |
| | | $V_{DD} = 15V$ | 14.95 | | 14.95 | 15 | | 14.95 | | |
| V_{IL} | LOW Level Input Voltage | $V_{DD}=5V, V_O=4.5V$ | | 1.5 | | 2 | 1.5 | | 1.5 | V |
| | | $V_{DD}=10V, V_O=9.0V$ | | 3.0 | | 4 | 3.0 | | 3.0 | |
| | | $V_{DD}=15V, V_O=13.5V$ | | 4.0 | | 6 | 4.0 | | 4.0 | |
| V_{IH} | HIGH Level Input Voltage | $V_{DD}=5V, V_O=0.5V$ | 3.5 | | 3.5 | 3 | | 3.5 | | V |
| | | $V_{DD}=10V, V_O=1.0V$ | 7.0 | | 7.0 | 6 | | 7.0 | | |
| | | $V_{DD}=15V, V_O=1.5V$ | 11.0 | | 11.0 | 9 | | 11.0 | | |
| I_{OL} | LOW Level Output Current (Note 5) | $V_{DD}=5V, V_O = 0.4V$ | 0.64 | | 0.51 | 0.88 | | 0.36 | | mA |
| | | $V_{DD} = 10V, V_O = 0.5V$ | 1.6 | | 1.3 | 2.2 | | 0.90 | | |
| | | $V_{DD} = 15V, V_O = 1.5V$ | 4.2 | | 3.4 | 8 | | 2.4 | | |
| I_{OH} | HIGH Level Output Current (Note 5) | $V_{DD} = 5V, V_O = 4.6V$ | -0.64 | | -0.51 | -0.88 | | -0.36 | | mA |
| | | $V_{DD} = 10V, V_O = 9.5V$ | -1.6 | | -1.3 | -2.2 | | -0.90 | | |
| | | $V_{DD} = 15V, V_O = 13.5V$ | -4.2 | | -3.4 | -8 | | -2.4 | | |
| I_{IN} | Input Current | $V_{DD} = 15V, V_{IN} = 0V$ | | -0.1 | | -10^{-5} | -0.1 | | -1.0 | μA |
| | | $V_{DD} = 15V, V_{IN} = 15V$ | | 0.1 | | 10^{-5} | 0.1 | | 1.0 | |

Note 4: $V_{SS} = 0V$ unless otherwise specified.

Note 5: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 6) $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------|--------------------------------------|-----------------------|-----|-----|-----|-------|
| t_{PHL} | Propagation Delay, HIGH-to-LOW Level | $V_{DD} = 5\text{V}$ | | 130 | 250 | ns |
| | | $V_{DD} = 10\text{V}$ | | 60 | 100 | |
| | | $V_{DD} = 15\text{V}$ | | 40 | 70 | |
| t_{PLH} | Propagation Delay, LOW-to-HIGH Level | $V_{DD} = 5\text{V}$ | | 110 | 250 | ns |
| | | $V_{DD} = 10\text{V}$ | | 50 | 100 | |
| | | $V_{DD} = 15\text{V}$ | | 35 | 70 | |
| t_{THL} t_{TLH} | Transition Time | $V_{DD} = 5\text{V}$ | | 90 | 200 | ns |
| | | $V_{DD} = 10\text{V}$ | | 50 | 100 | |
| | | $V_{DD} = 15\text{V}$ | | 40 | 80 | |
| C_{IN} | Average Input Capacitance | Any Input | | 5 | 7.5 | pF |
| C_{PD} | Power Dissipation Capacity (Note 7) | Any Gate | | 17 | | pF |

Note 6: AC Parameters are guaranteed by DC correlated testing.**Note 7:** C_{PD} determines the no load AC power consumption of any CMOS device.

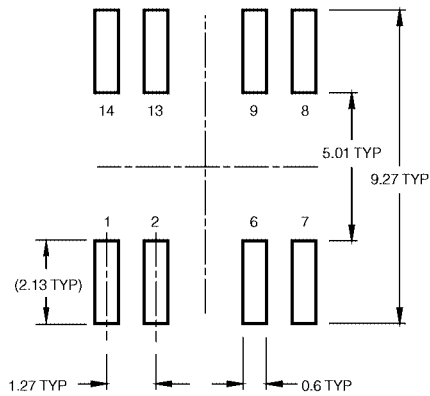
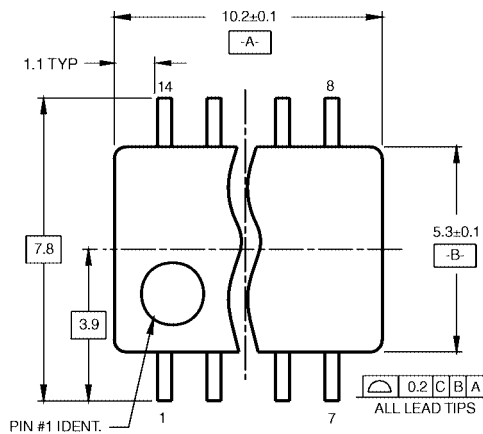
For complete explanation, see Family Characteristics Application Note AN-90.

Physical Dimensions inches (millimeters) unless otherwise noted

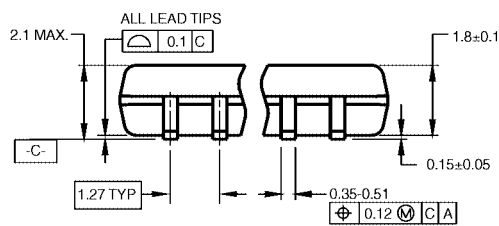


**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

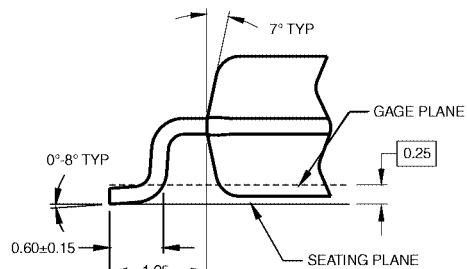
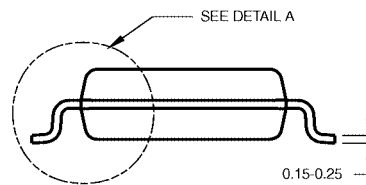
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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