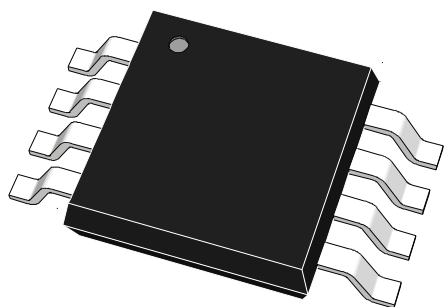


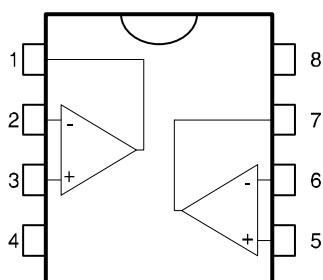
Low-power, dual-voltage comparator

Datasheet - production data



S
MiniSO8
(plastic micropackage)

Pin connections (top view)



- 1 - Output 1
- 2 - Inverting input 1
- 3 - Non-inverting input 1
- 4 - V_{CC}^-
- 5 - Non-inverting input 2
- 6 - Inverting input 2
- 7 - Output 2
- 8 - V_{CC}^+

Features

- Wide, single supply voltage range or dual supplies, 2 V to 36 V or ± 1 V to ± 18 V
- Very low supply current (0.4 mA) independent of supply voltage (1 mW/comparator at 5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ± 5 nA typ.
- Input common-mode voltage range includes negative rail
- Low output saturation voltage: 250 mV typ. ($I_o = 4$ mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs
- ESD internal protection: 2 kV
- Wide operating temperature range: -40 to 150 °C

Description

This device consists of two independent low-power voltage comparators designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

The input common-mode voltage range includes negative rail even though operated from a single power supply voltage.

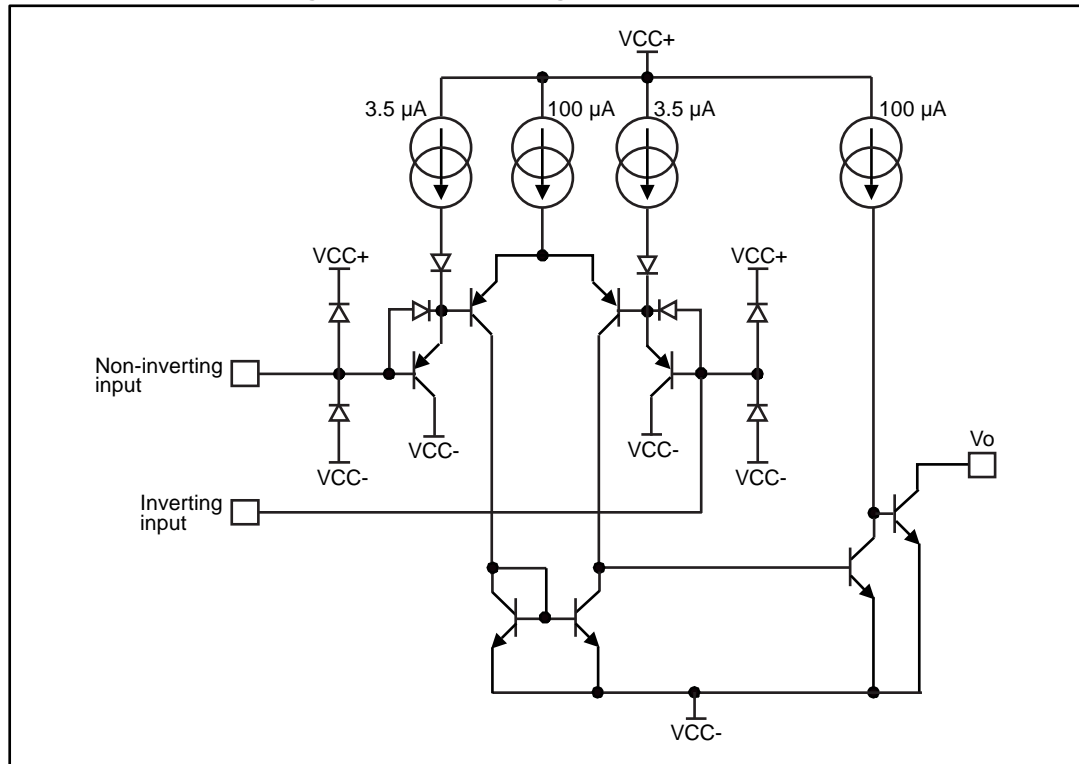
All pins are protected against electrostatic discharge up to 2 kV. Consequently, the input voltages must not exceed the V_{CC}^+ or V_{CC}^- magnitudes.

Contents

1	Schematic diagram.....	3
2	Absolute maximum ratings and operating conditions	4
3	Electrical characteristics	5
4	Typical application schematics	7
5	Package information	10
	5.1 MiniSO8 package information	11
6	Ordering information.....	12
7	Revision history	13

1 Schematic diagram

Figure 1: Schematic diagram (1/2 LM2903WH)



2 Absolute maximum ratings and operating conditions

Table 1: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	±18 or 36	V
V _{id}	Differential input voltage	(V _{CC} ⁻) - 0.3 to (V _{CC} ⁺) + 0.3	
V _{in}	Input voltage		
V _{out}	Output voltage	36	
	Output short-circuit to ground ⁽¹⁾	Infinite	
R _{thja}	Thermal resistance junction to ambient ⁽²⁾	190	°C/W
R _{thjc}	Thermal resistance junction to case ⁽²⁾	39	
T _j	Maximum junction temperature	160	°C
T _{stg}	Storage temperature range	-65 to 160	
ESD	Human body model (HBM) ⁽³⁾	2000	V
	Machine model (MM) ⁽⁴⁾	200	
	CDM: charged device model ⁽⁵⁾	1500	

Notes:

⁽¹⁾Short-circuits from the output to V_{CC}⁺ can cause excessive heating and possible destruction. The maximum output current is approximately 20 mA and is independent of the V_{CC}⁺ magnitude.

⁽²⁾Short-circuits can cause excessive heating and destructive dissipation. Values are typical and for a four-layer PCB.

⁽³⁾Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

⁽⁴⁾Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.

⁽⁵⁾Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V _{icm}	Common mode input voltage range	0 to (V _{CC} ⁺) - 1.5	V
	-40 °C ≤ T _{amb} ≤ 150 °C	0 to (V _{CC} ⁺) - 2	
T _{oper}	Operating free-air temperature range	-40 to 150	°C

3 Electrical characteristics

Table 3: $V_{CC+} = 5\text{ V}$, $V_{CC-} = \text{GND}$, $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ⁽¹⁾			1	7	mV
		$-40\text{ }^{\circ}\text{C} \leq T_{\text{amb}} \leq 150\text{ }^{\circ}\text{C}$			15	
I_{io}	Input offset current			5	50	nA
		$-40\text{ }^{\circ}\text{C} \leq T_{\text{amb}} \leq 150\text{ }^{\circ}\text{C}$			150	
I_{ib}	Input bias current ⁽²⁾			25	250	nA
		$-40\text{ }^{\circ}\text{C} \leq T_{\text{amb}} \leq 150\text{ }^{\circ}\text{C}$			400	
A_{vd}	Large signal voltage gain	$V_{CC} = 15\text{ V}$, $R_L = 15\text{ k}\Omega$, $V_o = 1\text{ to }11\text{ V}$	25	200		V/mV
I_{CC}	Supply current (all comparators)	$V_{CC} = 5\text{ V}$, no load		0.4	1	mA
		$V_{CC} = 30\text{ V}$, no load		1	2.5	
V_{id}	Differential input voltage ⁽³⁾				V_{CC+}	V
V_{OL}	Low level output voltage	$V_{id} = -1\text{ V}$, $I_{\text{sink}} = 4\text{ mA}$		250	400	mV
		$-40\text{ }^{\circ}\text{C} \leq T_{\text{amb}} \leq 150\text{ }^{\circ}\text{C}$			700	
I_{OH}	High level output current	$V_{CC} = V_o = 30\text{ V}$, $V_{id} = 1\text{ V}$		0.1		nA
		$-40\text{ }^{\circ}\text{C} \leq T_{\text{amb}} \leq 150\text{ }^{\circ}\text{C}$			1	μA
I_{sink}	Output sink current	$V_{id} = -1\text{ V}$, $V_o = 1.5\text{ V}$	6	16		mA
t_{res}	Small signal response time ⁽⁴⁾	$R_L = 5.1\text{ k}\Omega$ to V_{CC+}		1.3		μs
t_{rel}	Large signal response time, TTL input ⁽⁵⁾	$V_{\text{ref}} = 1.4\text{ V}$, $R_L = 5.1\text{ k}\Omega$ to V_{CC+} , output signal at 50 % of final value			500	ns
		$V_{\text{ref}} = 1.4\text{ V}$, $R_L = 5.1\text{ k}\Omega$ to V_{CC+} , output signal at 95 % of final value			1	μs

Notes:

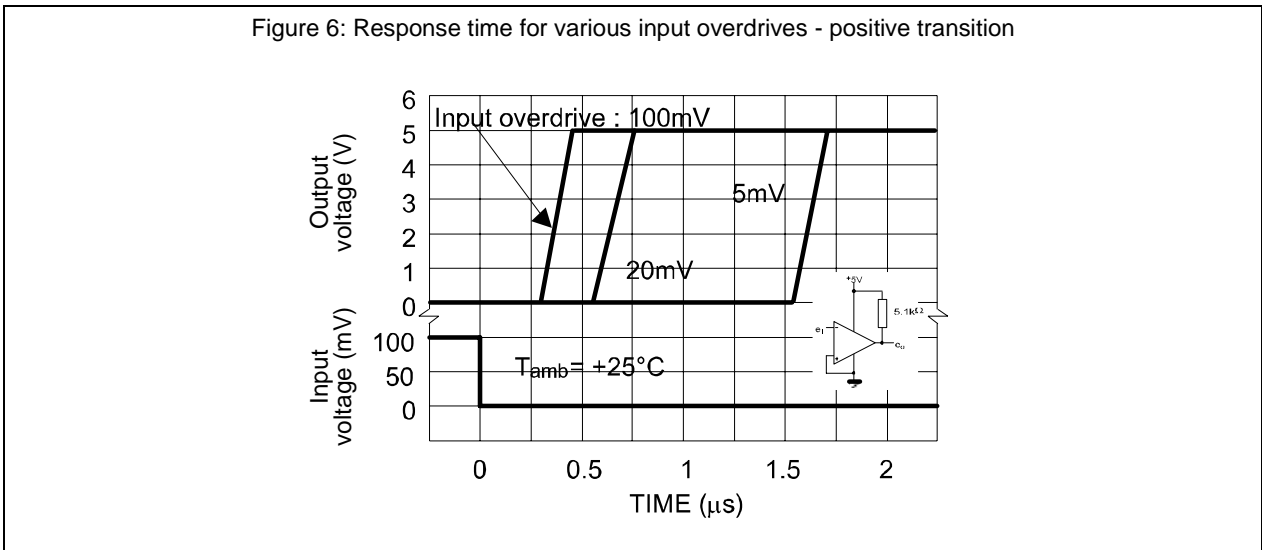
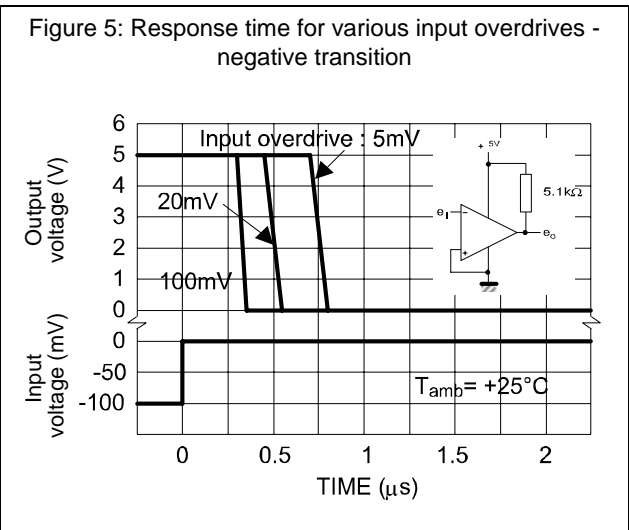
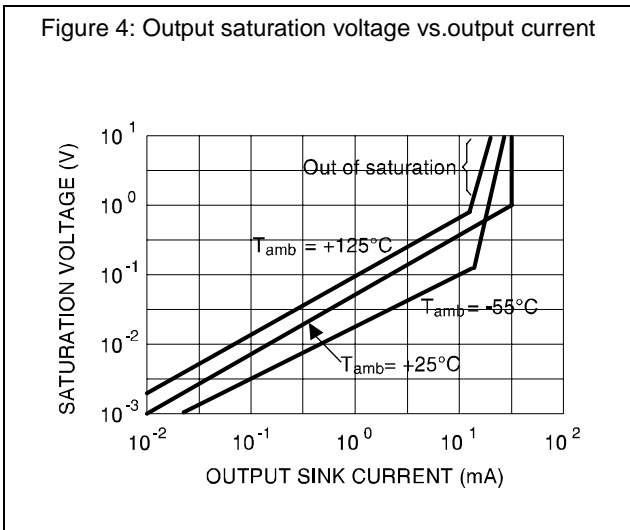
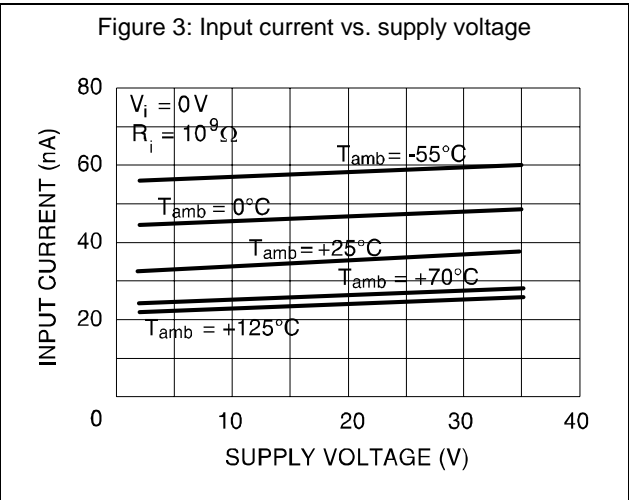
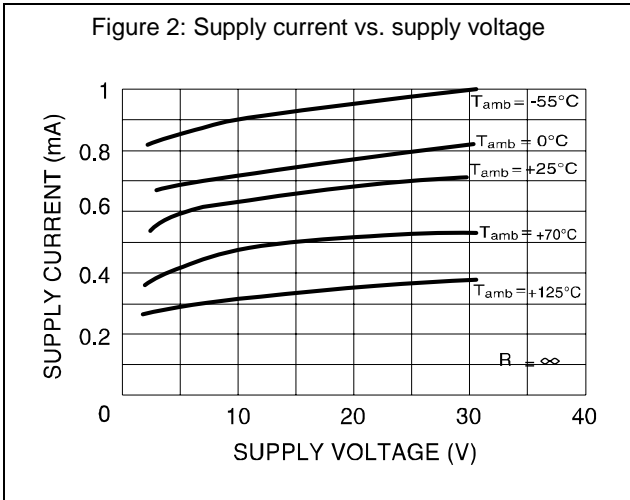
⁽¹⁾At output switch point, $V_o \approx 1.4\text{ V}$, $R_S = 0\text{ }\Omega$ with V_{CC+} from 5 V to 30 V, and over the full input common-mode range (0 V to $V_{CC+} - 1.5\text{ V}$).

⁽²⁾The direction of the input current is from the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference of input lines.

⁽³⁾Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator provides a proper output state. The low input voltage state must not be less than -0.3 V (or 0.3 V below the negative power supply, if used).

⁽⁴⁾The response time specified is for a 100 mV input step with 5 mV overdrive.

⁽⁵⁾Maximum values are guaranteed by design and evaluation.



4 Typical application schematics

Figure 7: Basic comparator

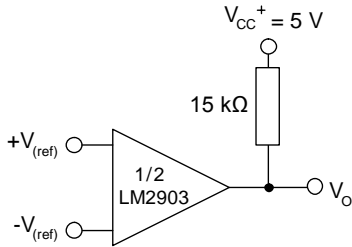


Figure 8: Driving CMOS

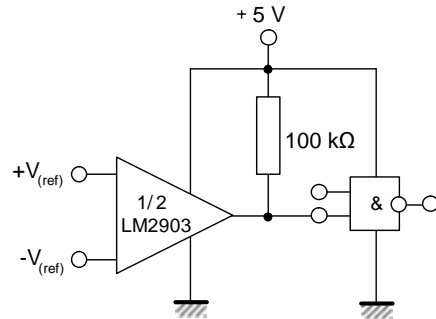


Figure 9: Driving TTL

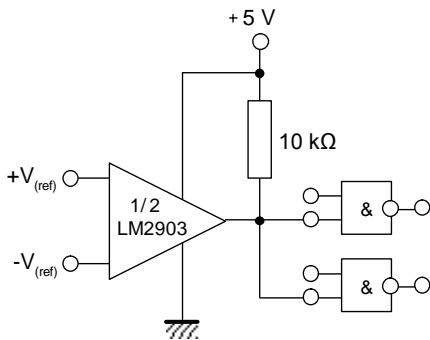


Figure 10: Low-frequency op amp

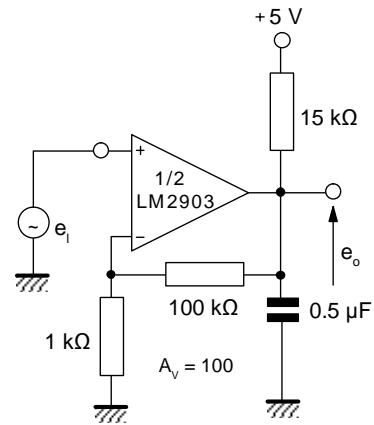


Figure 11: High-output current capability op amp

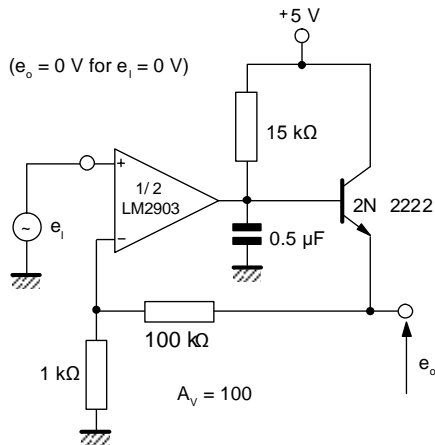


Figure 12: Transducer amplifier

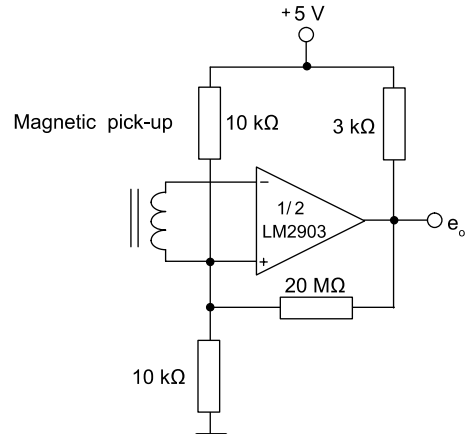


Figure 13: Low-frequency op amp with offset adjust

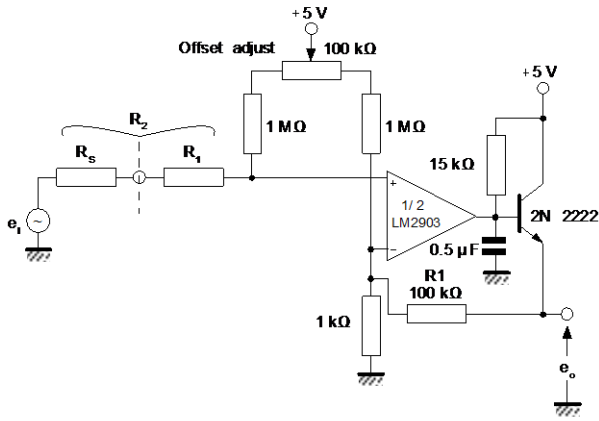


Figure 14: Zero crossing detector (single power supply)

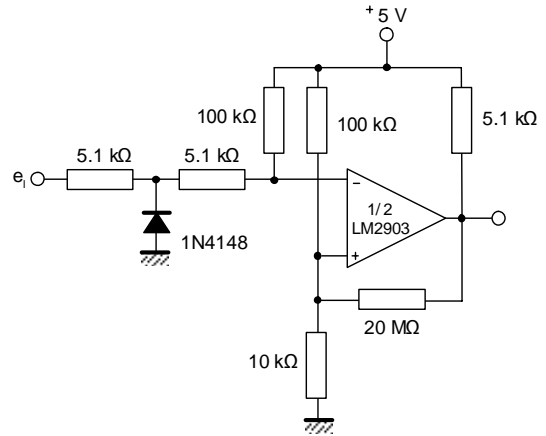


Figure 15: Limit comparator

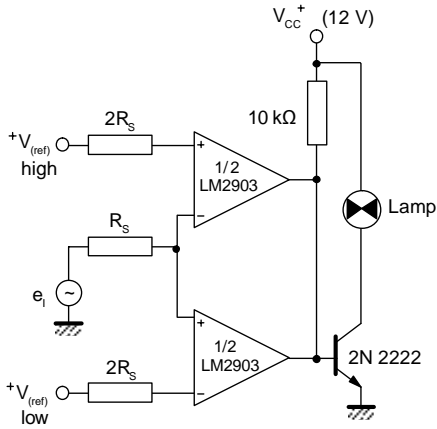


Figure 16: Split-supply applications - zero crossing detector

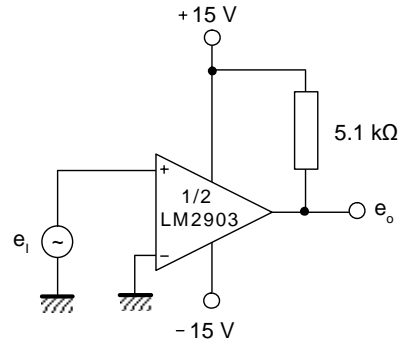


Figure 17: Crystal controlled oscillator

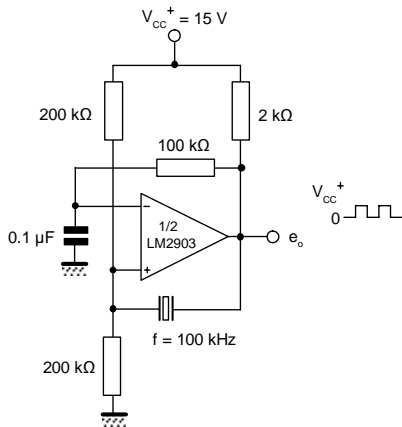


Figure 18: Comparator with a negative reference

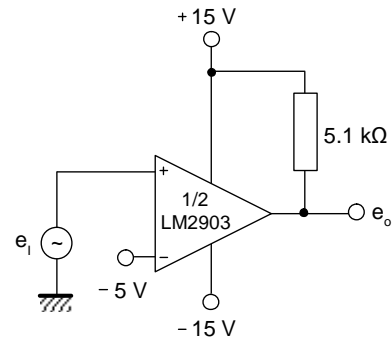


Figure 19: Time delay generator

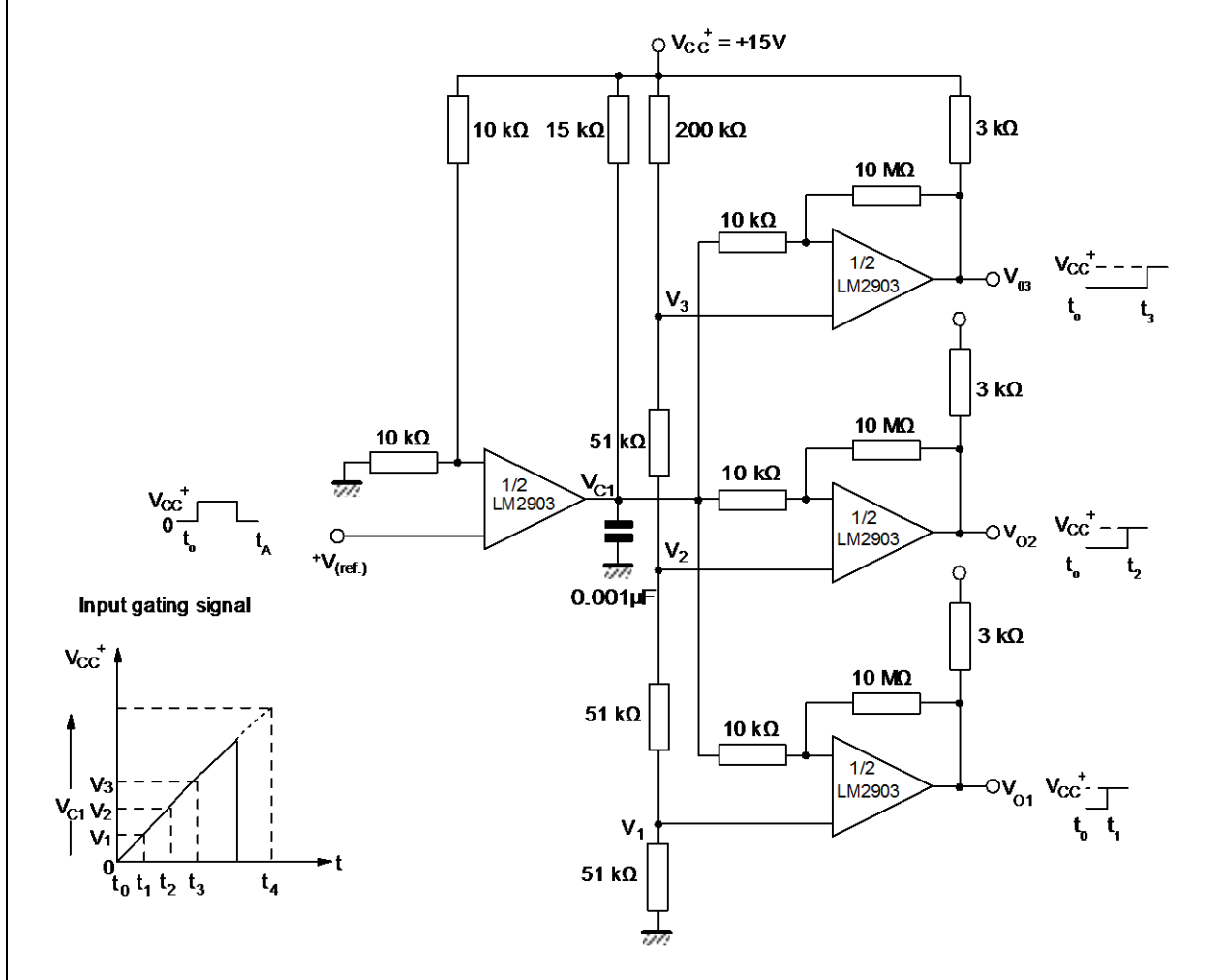
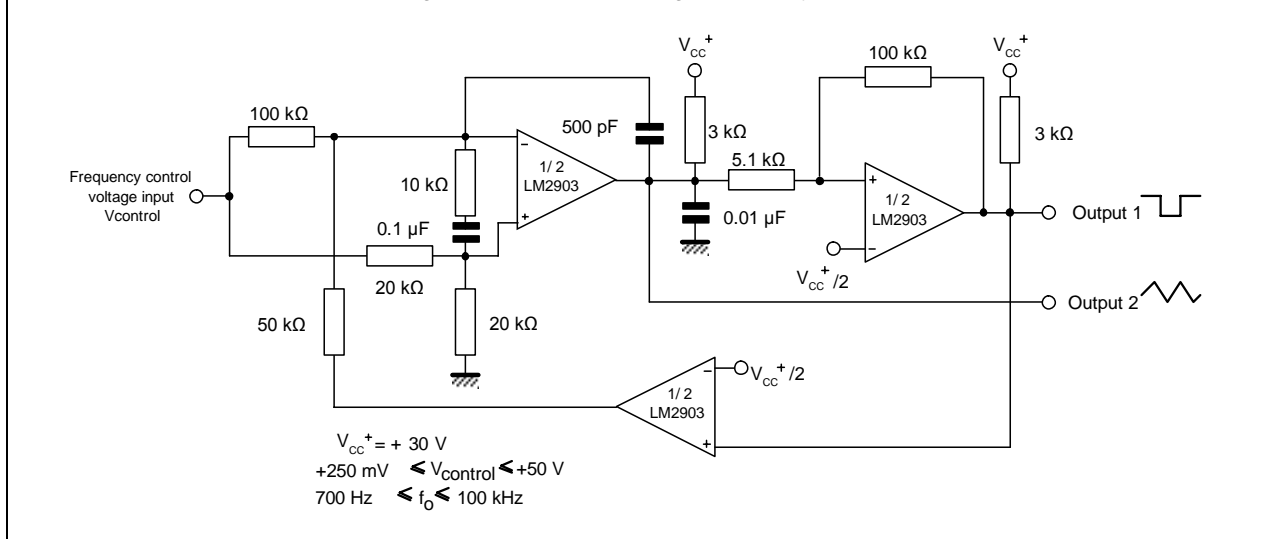


Figure 20: Two-decade high-frequency VCO



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

5.1 MiniSO8 package information

Figure 21: MiniSO8 package outline

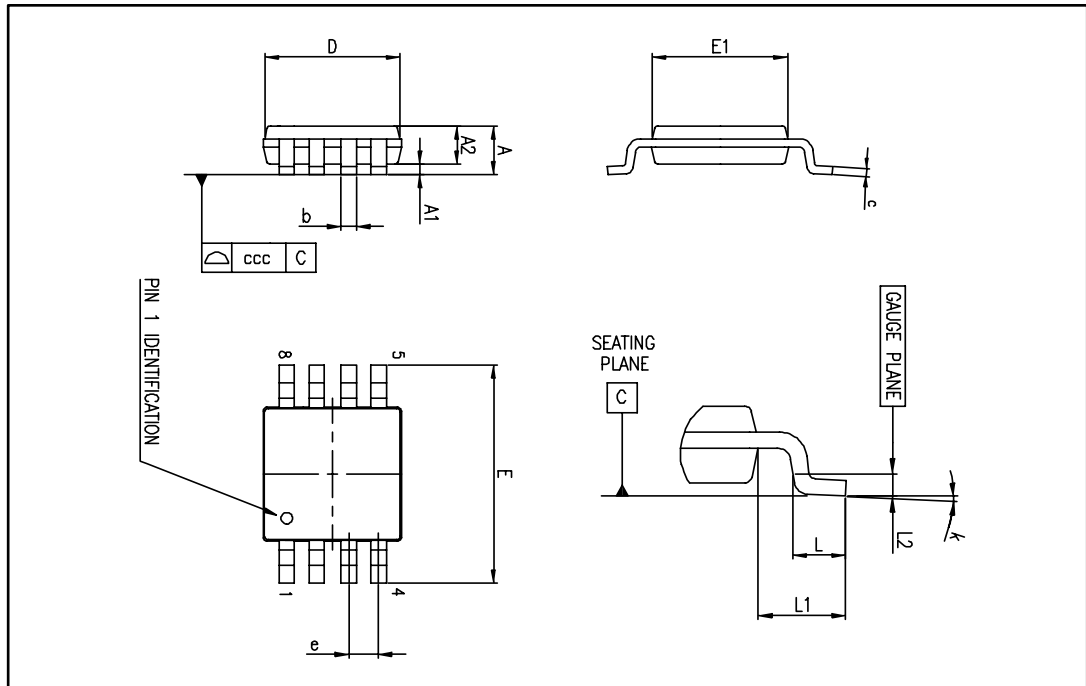


Table 4: MiniSO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

6 Ordering information

Table 5: Order codes

Order code	Temperature range	Package	Packing	Marking
LM2903WHYST ⁽¹⁾	-40 °C to +150 °C	MiniSO8 (automotive grade)	Tape and reel	K421

Notes:

⁽¹⁾Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent.

7 Revision history

Table 6: Document revision history

Date	Version	Changes
07-Oct-2015	1	Initial release

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