

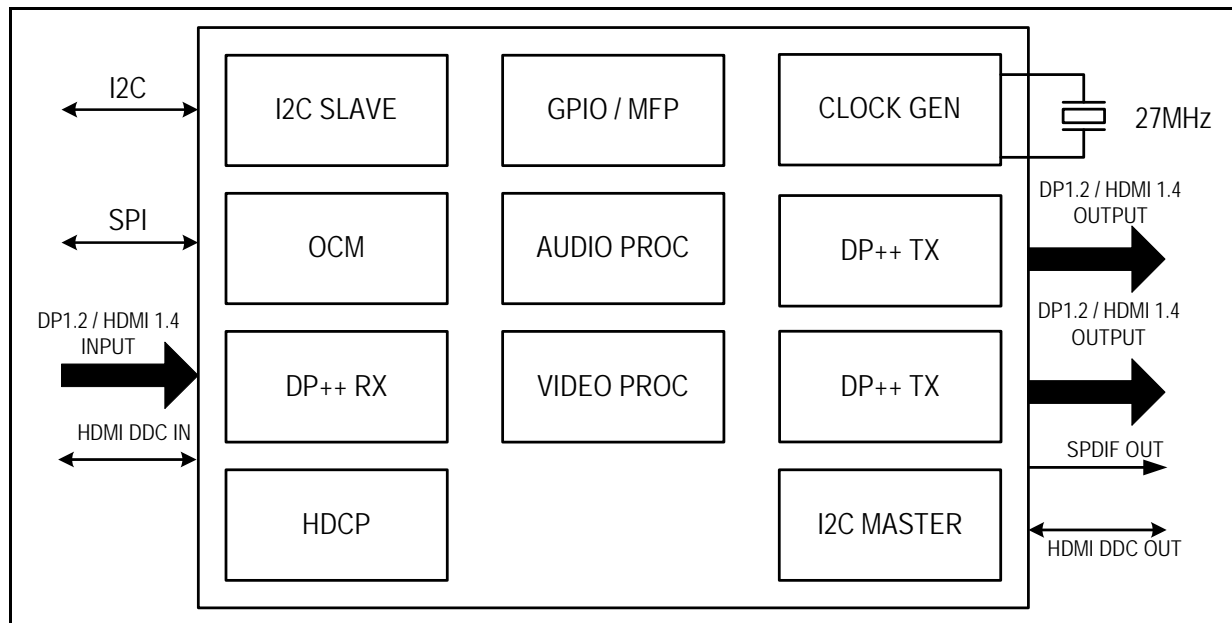
## Features

- DisplayPort® dual mode receiver
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - SST or MST (up to eight streams)
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - HPD out
  - HDMI/DVI operation (3.2 Gbps link rate)
  - Functions as eDP and MyDP receiver
- DisplayPort dual mode transmitters
  - Two transmitter ports
  - DP 1.2a compliant
  - Link rate HBR2/HBR/RBR
  - SST or MST (up to eight streams)
  - 1, 2, or 4 lanes
  - AUX CH 1 Mbps
  - HPD in
  - HDMI/DVI operation (3.2 Gbps link rate) with external level translator
  - Functions as eDP transmitter
- SPDIF audio output
  - Two SPDIF port pins
  - 192 kHz/24 bits
  - Compressed/LPCM
- Conversion from DP SST to TMDS format and vice versa
- HDCP repeater with embedded keys
- AUX to I2C bridge for EDID/MCCS pass through
  - Maps on DDC ports
- Device configuration options
  - SPI Flash
  - I2C host interface
- Deep color support
  - RGB/YCC (4:4:4) – 16-bit color
  - YCC (4:2:2) – 16-bit color
- Spread spectrum on DisplayPort interface for EMI reduction
- Bandwidth
  - Video resolution up to 4K2K @ 60 Hz
  - Audio 7.1 Ch up to 192 kHz sample rate

- Low power operation
  - Standby 30 mW
- Package
  - 172 LFBGA (12 x 12 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

## Applications

- Audio-video router for PC/notebooks, docking stations, hub, 4K2K TVs, daisy chain monitors, digital signage



## 1. Description

The STDP4320 is a high-speed DisplayPort dual mode splitter IC targeted for audio-video de-multiplexing and routing in applications such as notebooks, docking stations, video hub, 4K2K TVs, daisy chainable monitors, digital signage, etc. It consists of one dual mode input port and two dual mode output ports configurable as either DisplayPort or HDMI/DVI. STDP4320 is a VESA DP Standard Ver. 1.2a compliant device that supports advanced features such as MST, HBR2, 3D formats and GTC assist. Designs based on STDP4320 have the flexibility to offer either DP or HDMI/DVI connectors on its end product to interface with legacy and new generation video sources and sinks. In addition, STDP4320-based products with a DisplayPort output connector are DP++ compliant and work with any HDMI or single link DVI sink through a passive level translator (dongle).

The STDP4320 uses MegaChips' latest generation DisplayPort dual mode receiver and transmitter technology that supports both DisplayPort and TMDS signal formats. This device receives MST format up to eight audio-video streams, which can be further routed on either of the two outputs in any combination of eight streams depending on the capability of downstream sinks. This device can also replicate the incoming video streams on both output ports simultaneously, thus allowing cloning on two downstream sinks. For example, a 4K2K 60 Hz video input is replicated on two output ports simultaneously. The DisplayPort receiver and transmitters support HBR2 speed, a data rate of 5.4 Gbps per lane with a total bandwidth of 21.6 Gbps link rate. In HDMI mode, this device supports link rates up to 3.2 Gbps corresponding to a pixel rate of 300 MHz, adequate for supporting video resolution up to FHD 120 Hz with all 3D formats. The device is also capable of delivering deep color video up to 16-bits per color. The STDP4320 allows audio transport from the source to the desired audio rendering devices over the video output port or through an SPDIF port.

The STDP4320 supports RGB and YCbCr colorimetric formats with color depth of 16, 12, 10, and 8 bits. The STDP4320 features the HDCP 1.3 content protection scheme with embedded keys for secure transmission of protected audio-video content. It also operates as an HDCP repeater for the downstream sinks.

The DDC ports in the STDP4320 allow the upstream source to access EDID and transfer MCCS commands to downstream sinks when the physical ports are either HDMI or DVI type. If both the upstream source and downstream sinks are DP type, I2C transactions take place over the AUX CH. If one of them is a DP type and the other is either a HDMI or DVI type, STDP4320 converts the I2C over AUX message protocol to I2C commands and sends it on the DDC port.

The device has an on-chip microcontroller with SPI, UART, and I2C interface. The STDP4320 uses an external SPI Flash ROM for storing device configuration firmware. It has an I2C slave port for external host communication. Other system interface signals include general-purpose IO for source, sink communication, detection, monitoring, etc. When the downstream sink is disconnected, STDP4320 automatically turns off the inactive port for power saving purposes.

## 2. Application overview

Figure 1. STDP4320 in video hub application

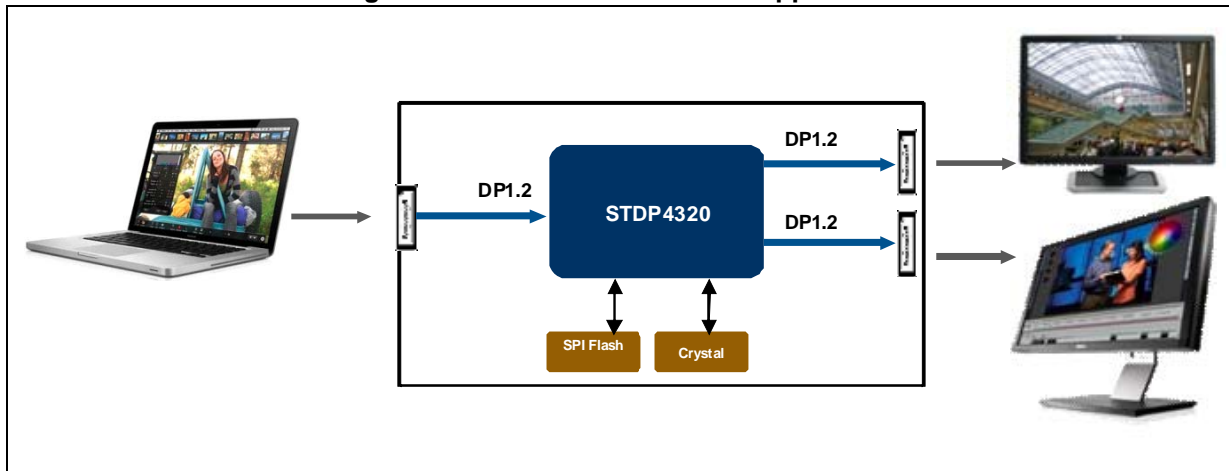
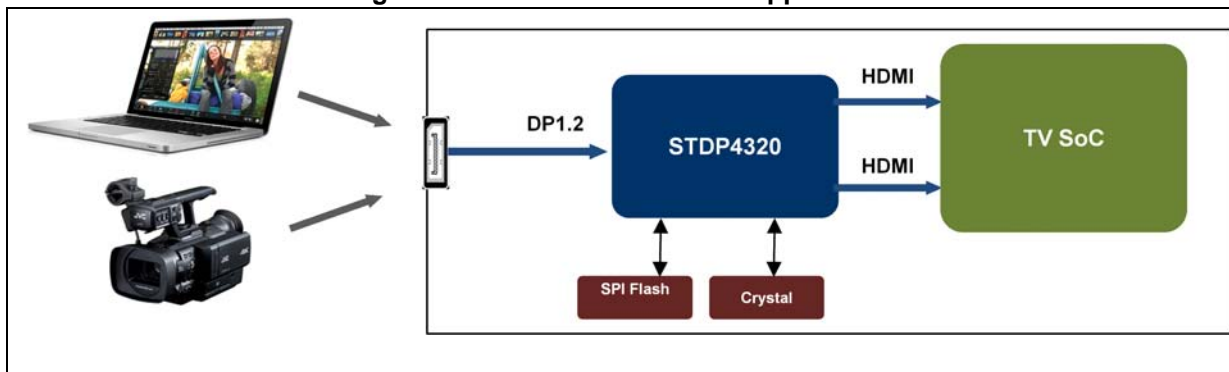


Figure 2. STDP4320 in 4K2K TV application



### 3. Feature attributes

#### 3.1 Input interface

- Single DP++ interface featuring
  - DisplayPort Ver. 1.2a compliant receiver; supports eDP and MyDP
  - HDMI 1.4 compliant receiver
- Main link configuration
  - SST or MST (up to eight streams)
  - HBR2/HBR/RBR link rate
  - 1, 2, or 4 lanes
- AUX CH: 1 Mbps Manchester transaction format
- HPD: IRQ\_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB, YCC422, or YCC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates
- HDMI link rate: 3.2 Gbps/data pair max

### 3.2 Output interface

- Two DP++ interfaces featuring
  - AC coupled DisplayPort Ver. 1.2a compliant transmitter: supports eDP
  - AC coupled HDMI 1.4 transmitter
- DP main link configuration
  - SST or MST (up to eight streams)
  - HBR2/HBR/RBR link rate
  - 1, 2, or 4 lanes
- AUX CH: Manchester transaction format
- HPD: IRQ\_HPD assertion
- Video: EDID 1.4 and CEA861 video timing and formats from 24 to 48 bits/pixel in RGB, YCC422, or YCC444 colorimetry
- Audio: DisplayPort 1.2a standard info frame packets and IEC60958/61937 type audio stream packets ranging from 16 to 24 bits/sample, 32 to 192 kHz sample rates
- HDMI link rate: 3.2 Gbps/data pair max

### 3.3 Supported video timings

- 4K2K 60 Hz: 24 bits/pixel in DP 1.2a configuration
- 1920 x 1080 (FHD) 240 Hz, 24 bits/pixel
- All 3D formats defined in DP 1.2a and HDMI 1.4 standards
- All standard CEA861 timing formats

### 3.4 Supported audio timings

- All audio formats as specified in DP 1.2a and HDMI 1.4 standards
- SPDIF; 2-Ch LPCM, AC3, DTS, bit depth up to 24 bits, sample rate up to 192 kHz (applicable in DP SST/HDMI output use case)

### 3.5 Control channel interfaces

- AUX CH, DDC, I2C host interface, and UART (UART for test/debug purposes only)

### 3.6 HDCP 1.3 support

- Key sets for DP/HDMI RX and DP/HDMI TX integrated in one-time programmable ROM (OTP)
- Standalone HDCP repeater capability

### 3.7 Package

- 172 LFBGA (12 x 12 mm), 0.8 ball pitch

### 3.8 Power supply voltages

- 3.3 V I/O; 1.2 V core

### 3.9 ESD

- 2 KV HBM, 450 V CDM



## 4. Ordering information

**Table 1. Order codes**

Part number	Description
STDP4320-BA	172 LFBGA (12 x 12 mm)

## 5. Revision history

**Table 2. Document revision history**

Date	Revision	Changes
02-Oct-2012	1	Preliminary release.
08-May-2013	2	Added eDP references throughout. Cover page: Low power operation standby changed to 30 mW. Updated link rate for HDMI/DVI operation on cover page; changed HDMI mode pixel rate in Description section. Removal of CEC throughout including in block diagrams. Ordering information section: Updated silicon revision in the table.
27-Jun-2013	3	Cover page: Deep color support YCC bullet updated. Section 3.9 ESD updated.
26-May-2014	4	Updated to comply with MegaChips documentation style/formatting.
15-Sep-2014	5	Updated footers and added copyright information to last page.

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