

74CB3Q3257

4-bit 1-of-2 FET multiplexer/demultiplexer with charge pump

Rev. 1 — 14 August 2017

Product data sheet

1 General description

The 74CB3Q3257 is a quad high-bandwidth single-pole, double-throw FET bus switch. The device features one select input (S) and one output enable input (\overline{OE}). The switch is disabled when the \overline{OE} input is HIGH. An internal charge-pump increases the gate voltage of the NMOS pass transistor. The result is improved R_{ON} and $R_{ON(flat)}$ performance and the ability to switch 5 V signals when $V_{CC} = 3.3$ V.

2 Features and benefits

- Wide supply voltage range from 2.3 V to 3.6 V
- Overvoltage switching on switch ports:
 - 0 V to 5 V switching with $V_{CC} = 2.5$ V
 - 0 V to 5 V switching with $V_{CC} = 3.3$ V
- 4 Ω (typical) ON resistance
- 3.5 pF (typical) OFF-state capacitance
- High bandwidth 0.5 GHz (maximum)
- Low input/output capacitance minimizes loading and signal distortion
- Fast switching frequency $f_{max} = 20$ MHz (maximum)
- Low power consumption $I_{CC} = 0.4$ mA (typical)
- Control inputs can be driven by TTL or 5 V/3.3 V CMOS outputs
- I_{OFF} supports partial power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78E Class II Level A
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001-2012 Class 2 exceeds 2 kV
 - CDM JESD22-C101F exceeds 1000 V
- Specified from -40 °C to $+85$ °C

3 Applications

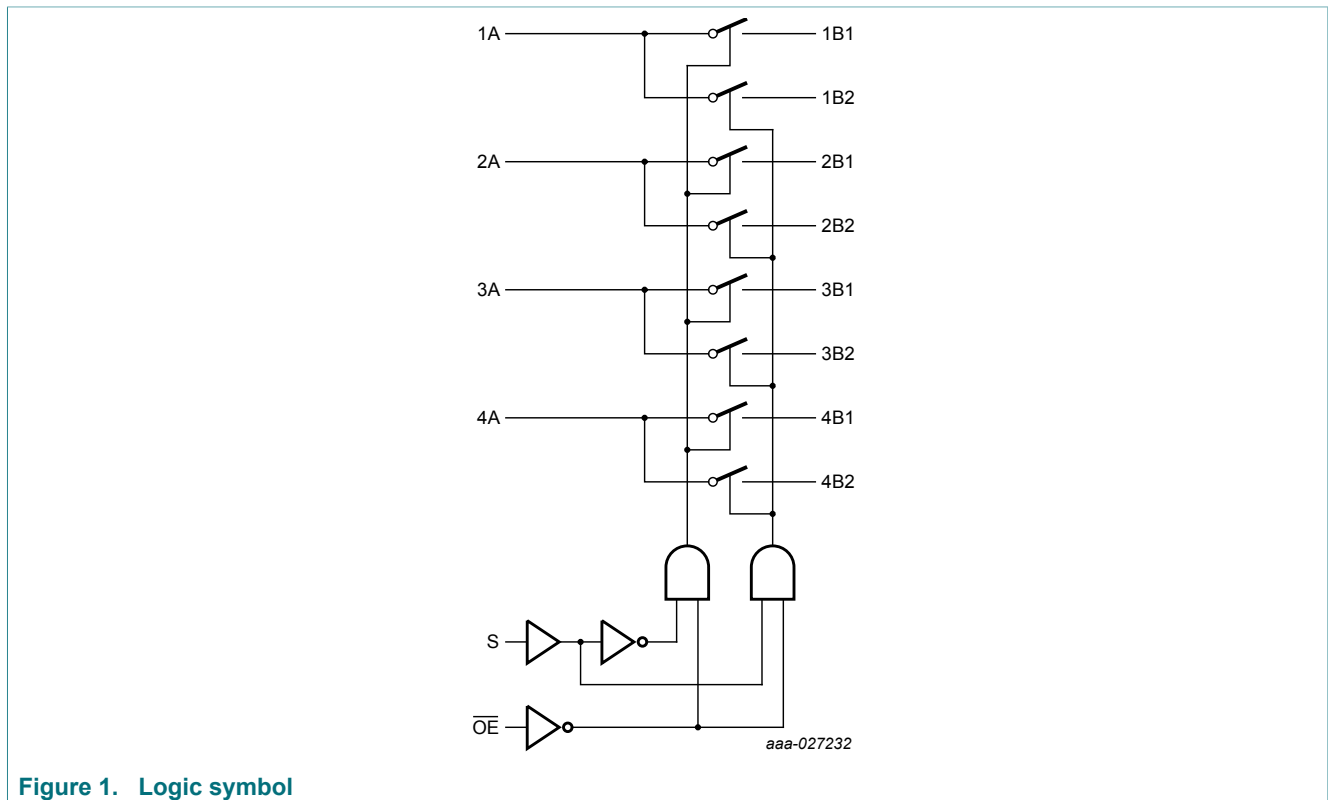
- Communication infrastructure
- Bus isolation
- Memory interleaving
- Sensor multiplexing

4 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74CB3Q3257PW	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74CB3Q3257BQ	-40 °C to +85 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm	SOT763-1

5 Functional diagram



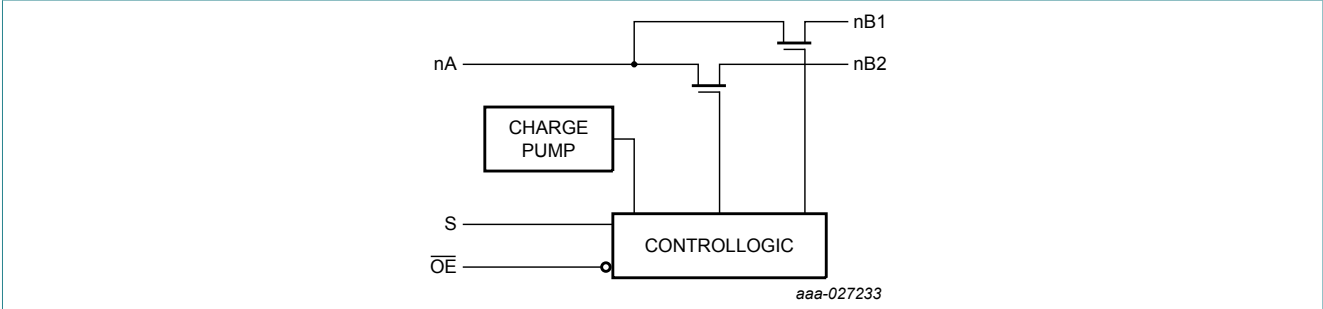


Figure 2. Logic diagram (one switch)

6 Pinning information

6.1 Pinning

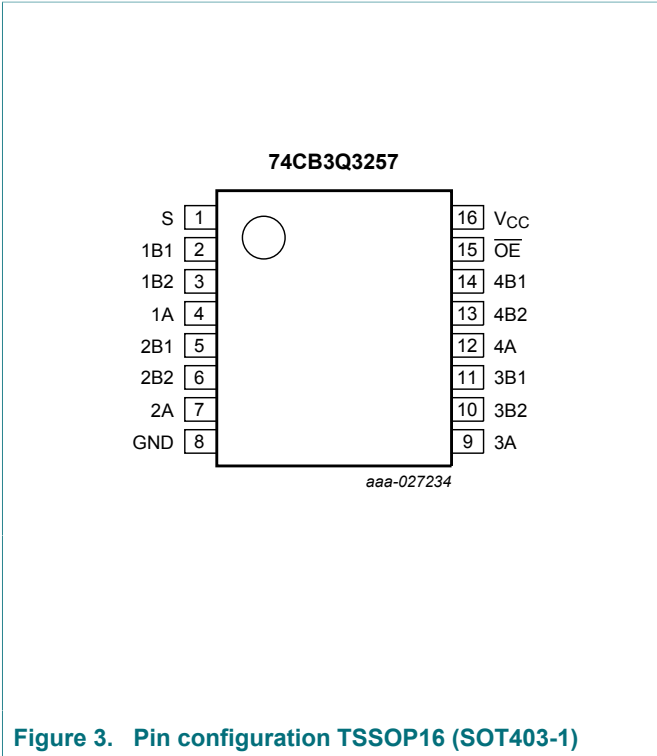


Figure 3. Pin configuration TSSOP16 (SOT403-1)

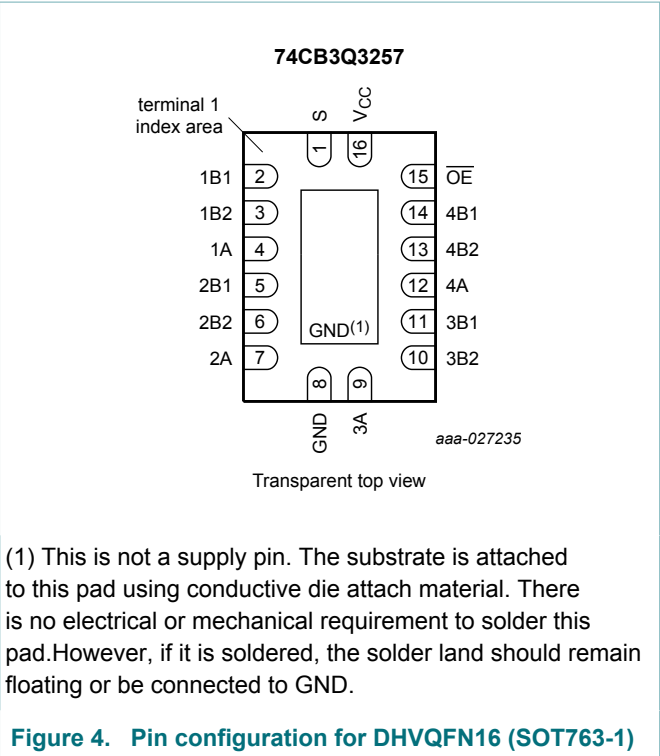


Figure 4. Pin configuration for DHVQFN16 (SOT763-1)

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	select input
1B1	2	independent input or output
1B2	3	independent input or output
1A	4	common output or input
2B1	5	independent input or output
2B2	6	independent input or output
2A	7	common output or input
GND	8	ground (0 V)
3A	9	common output or input
3B2	10	independent input or output
3B1	11	independent input or output
4A	12	common output or input
4B2	13	independent input or output
4B1	14	independent input or output
$\overline{\text{OE}}$	15	output enable input (active-LOW)
V _{CC}	16	supply voltage

7 Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Channel on
S	OE	
L	L	nA = nB1
H	L	nA = nB2
X	H	Z (switch off)

8 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	S, \overline{OE} input [1]	-0.5	+7.0	V
V_{SW}	switch voltage	[2]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SW}	switch current		-	± 120	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C [3]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
V_I	input voltage	S, \overline{OE} input	0	5.5	V
V_{SW}	switch voltage		0	5.5	V
T_{amb}	ambient temperature		-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	S, \overline{OE} input			
		$V_{CC} = 2.3$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	10	ns/V

10 Static characteristics

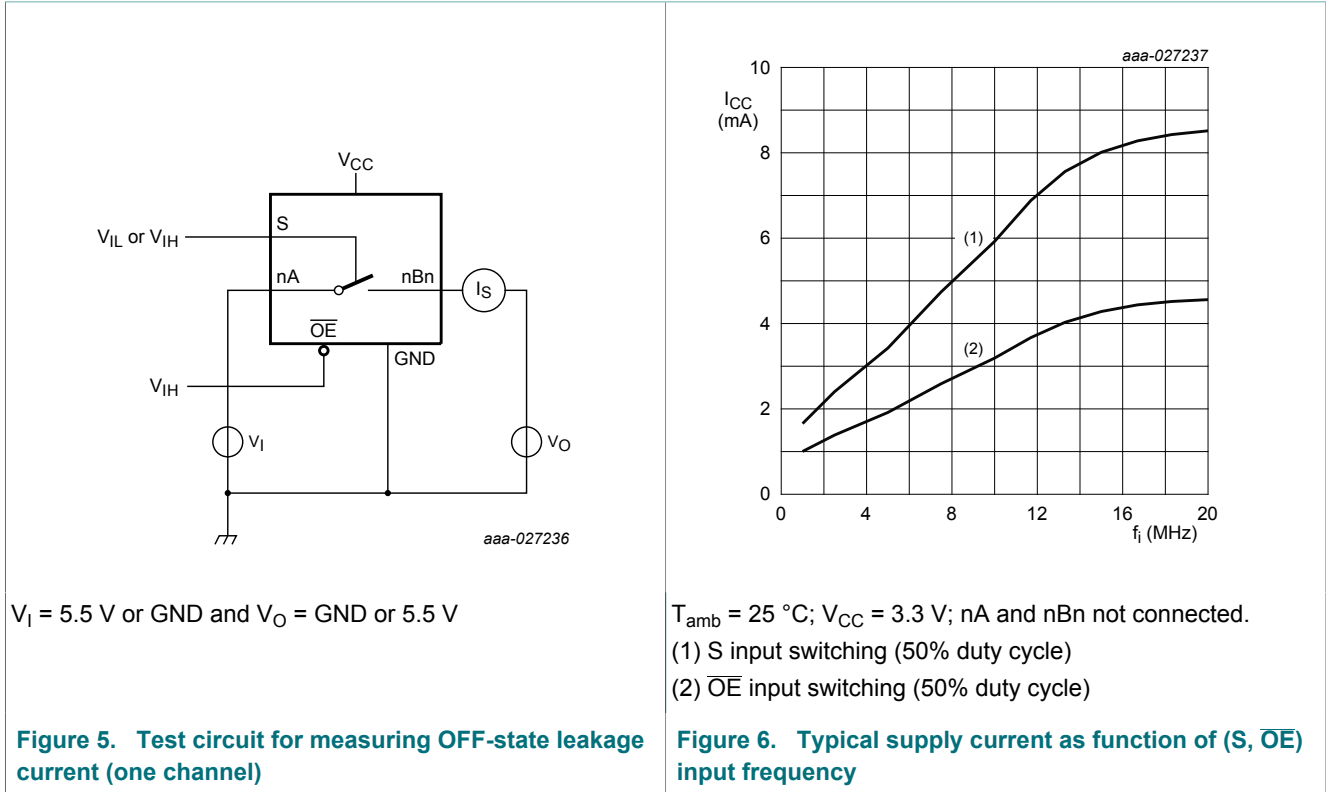
Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85°C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	-	-	-	2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	-	-	0.8	V
V _{IK}	input clamping voltage	nA, nBn; V _{CC} = 3.6 V; I _I = -18 mA	-	-	-	-	-1.8	V
I _I	input leakage current	S, \overline{OE} ; V _{CC} = 3.6 V; V _I = GND to 5.5 V	-	-	-	-	±1	μA
I _{OFF}	power-off leakage current	per pin; V _{CC} = 0 V; V _{SW} or V _I = 0 V to 5.5 V	-	-	-	-	±1	μA
I _{S(OFF)}	OFF-state leakage current	nA, nBn; V _{CC} = 3.6 V; see Figure 5	-	-	-	-	±1	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V	-	0.4	-	-	0.6	mA
ΔI _{CC}	additional supply current	S, \overline{OE} ; V _{CC} = 3.6 V; one input at 3 V, other inputs at GND or V _{CC}	-	-	-	-	30	μA
C _I	input capacitance	V _{CC} = 3.3 V; V _{SW} = GND or V _{CC} ; V _I = 0 V, 3.3 V, 5.5 V						
		S, \overline{OE}	-	2.5	-	-	3.5	pF
C _{S(OFF)}	OFF-state capacitance	V _{CC} = 3.3 V; V _{SW} = 0 V, 3.3 V, 5.5 V						
		nA	-	5.5	-	-	7	pF
		nBn	-	3.5	-	-	5	pF
C _{S(ON)}	ON-state capacitance	V _{CC} = 3.3 V; V _{SW} = 0 V, 3.3 V, 5.5 V						
		nA, nBn	-	10.5	-	-	13	pF

[1] Typical values are measured at V_{CC} = 3.3 V unless otherwise specified.

10.1 Test circuit and graph



10.2 ON resistance

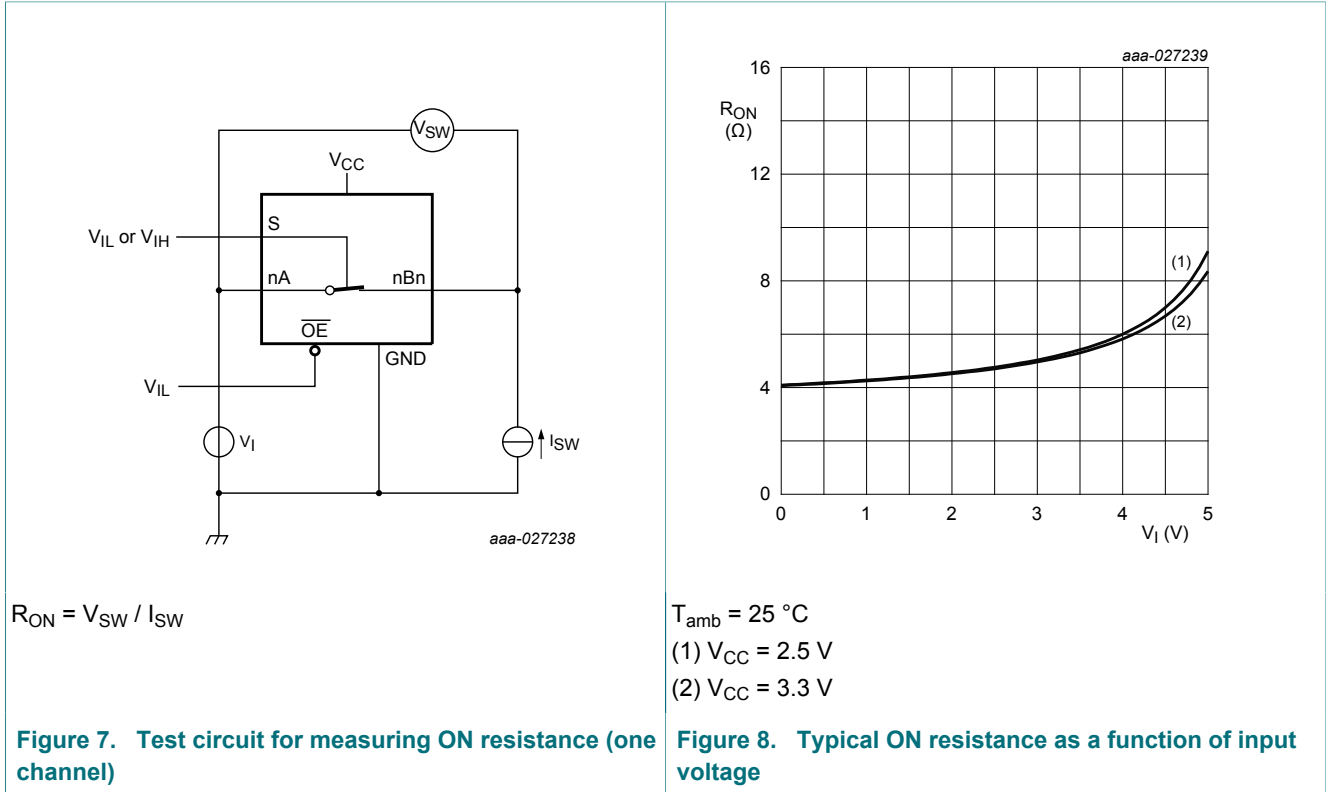
Table 7. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	$T_{\text{amb}} = 25\text{ }^\circ\text{C}$			$T_{\text{amb}} = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	$V_{\text{CC}} = 2.3\text{ V};$ see Figure 8						
		$V_I = 0\text{ V}; I_{\text{SW}} = 30\text{ mA}$ [1]	-	4	-	-	8	Ω
		$V_I = 1.7\text{ V}; I_{\text{SW}} = -15\text{ mA}$ [1]	-	4.4	-	-	9	Ω
		$V_{\text{CC}} = 3.0\text{ V};$ see Figure 8						
		$V_I = 0\text{ V}; I_{\text{SW}} = 30\text{ mA}$ [2]	-	4	-	-	6	Ω
		$V_I = 2.4\text{ V}; I_{\text{SW}} = -15\text{ mA}$ [2]	-	4.7	-	-	8	Ω

[1] Typical values are measured at $V_{\text{CC}} = 2.5\text{ V}$.
 [2] Typical values are measured at $V_{\text{CC}} = 3.3\text{ V}$.

10.3 ON resistance test circuit and graph



11 Dynamic characteristics

Table 8. Dynamic characteristics

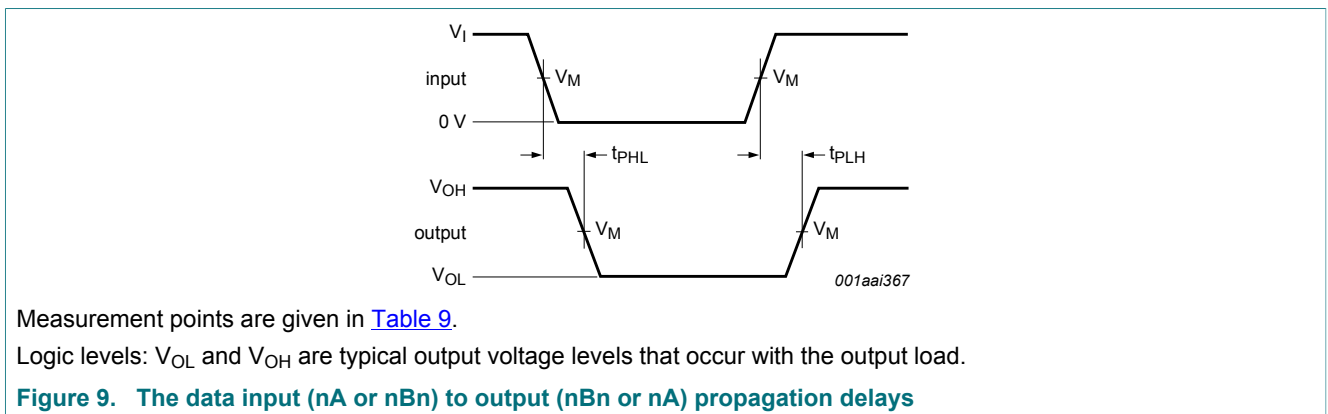
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 11.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$		Unit
			Min	Max	
t_{pd}	propagation delay	nA to nBn or nBn to nA; see Figure 9 [1] [2]			
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	0.12	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	0.20	ns
		S to nA; see Figure 9 [1]			
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.5	6.5	ns
	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	5.5	ns	

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C		Unit
			Min	Max	
t _{en}	enable time	\overline{OE} to nA, nBn; see Figure 10 [1]			
		V _{CC} = 2.3 V to 2.7 V	1.5	6.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	5.5	ns
		S to nBn; see Figure 10 [1]			
		V _{CC} = 2.3 V to 2.7 V	1.5	6.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	5.5	ns
t _{dis}	disable time	\overline{OE} to nA, nBn; see Figure 10 [1]			
		V _{CC} = 2.3 V to 2.7 V	1.0	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	6.0	ns
		S to nBn; see Figure 10 [1]			
		V _{CC} = 2.3 V to 2.7 V	1.0	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	6.0	ns
f _{max}	maximum frequency	S, \overline{OE} ; V _O > V _{CC} ; V _I = 5 V; R _L ≥ 1 MΩ; C _L = 0 pF			
		V _{CC} = 2.3 V to 2.7 V	-	10	MHz
		V _{CC} = 3.0 V to 3.6 V	-	20	MHz

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [2] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

11.1 Waveforms and test circuit



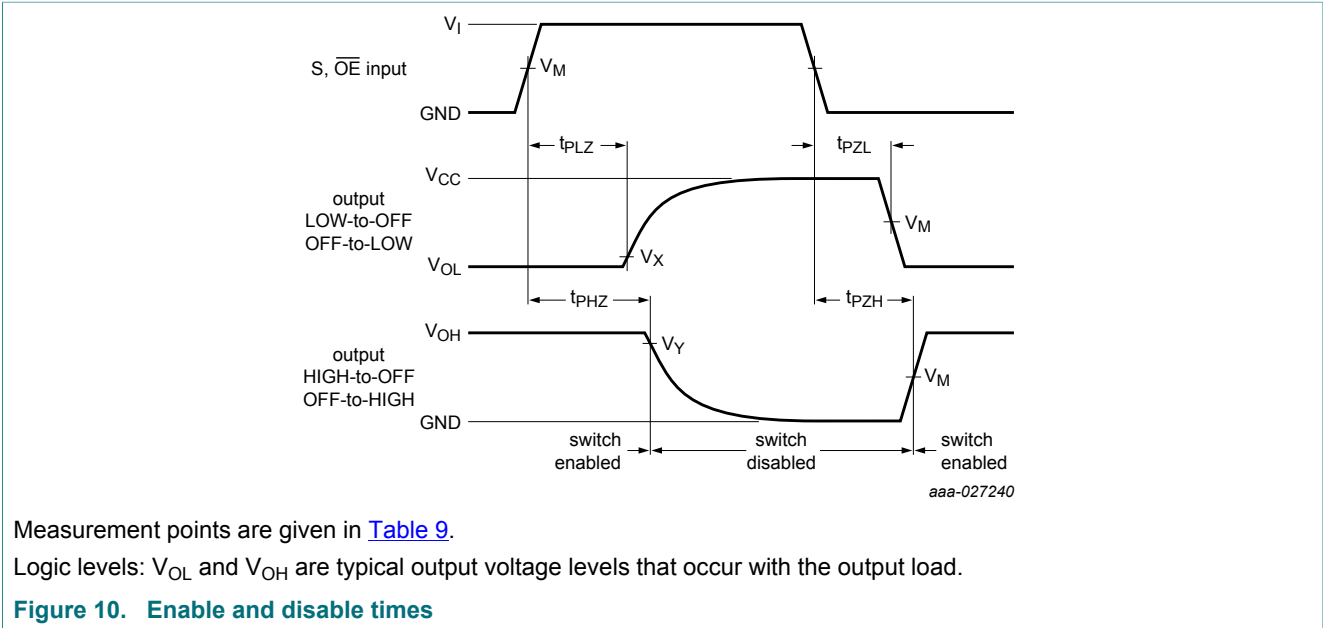
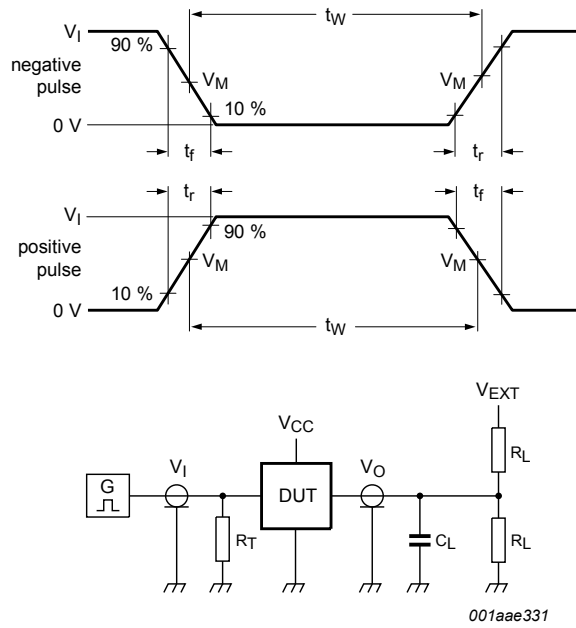


Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
3.0 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Figure 11. Test circuit for measuring switching times

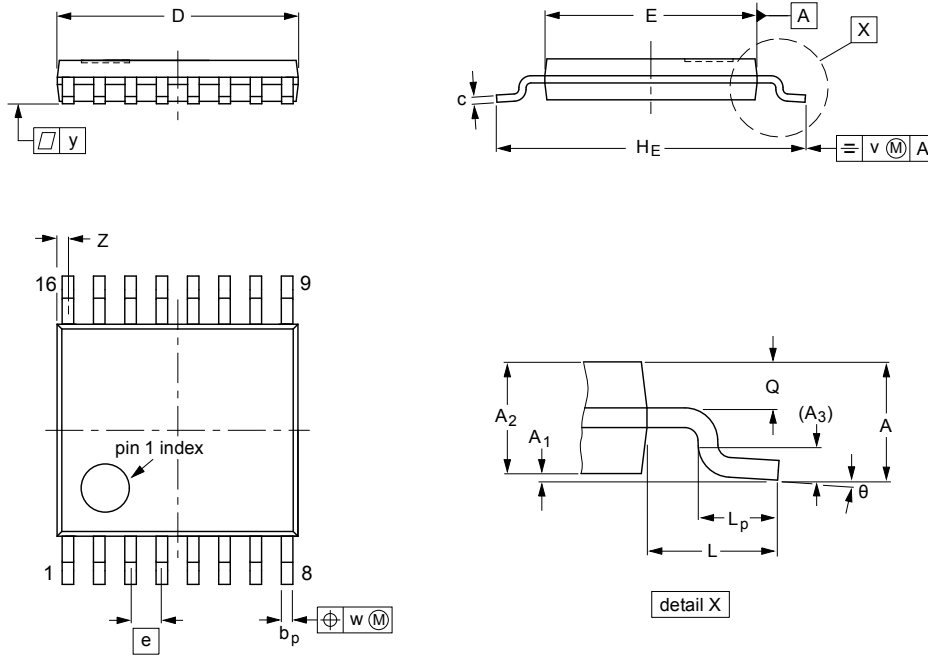
Table 10. Test data

Supply voltage	Input	Load			V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PZH}, t_{PHZ}
2.3 V to 2.7 V	V_{CC}	≤ 2.5 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

12 Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				99-12-27 03-02-18

Figure 12. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

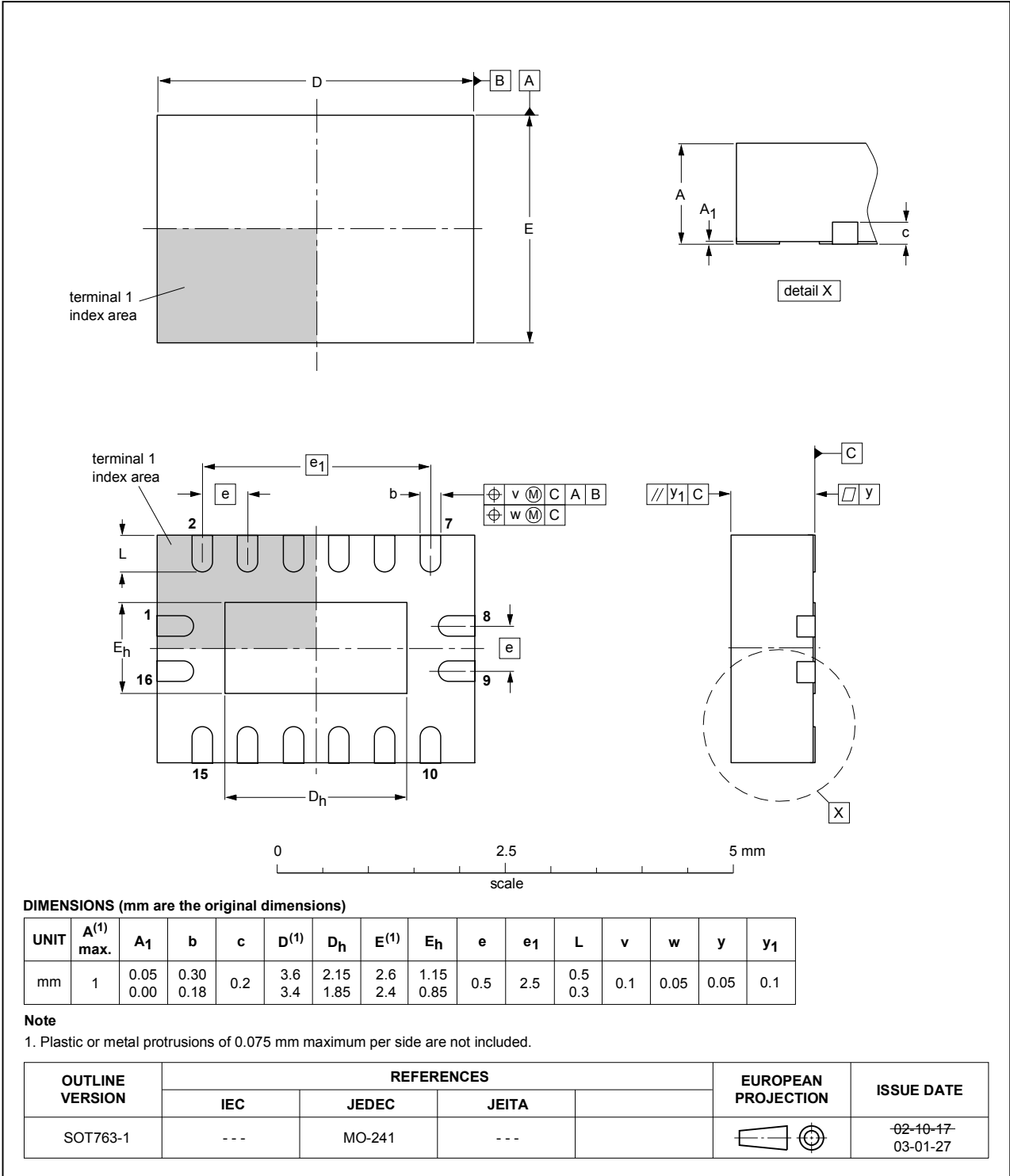


Figure 13. Package outline SOT763-1 (DHVQFN16)

13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CB3Q3257 v.1	20170814	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	4
7	Functional description	4
8	Limiting values	5
9	Recommended operating conditions	5
10	Static characteristics	6
10.1	Test circuit and graph	7
10.2	ON resistance	7
10.3	ON resistance test circuit and graph	8
11	Dynamic characteristics	8
11.1	Waveforms and test circuit	9
12	Package outline	12
13	Abbreviations	14
14	Revision history	14
15	Legal information	15

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Date of release: 14 August 2017
Document identifier: 74CB3Q3257