MICROCHIP

PIC18F6390/6490/8390/8490

PIC18F6390/6490/8390/8490 Rev. C1 Silicon Errata

The PIC18F6390/6490/8390/8490 Rev. C1 parts you have received conform functionally to the Device Data Sheet (DS39629**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F6390/6490/8390/8490 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F6390/6490/8390/8490 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F6390	0000 1011 101	0 0110
PIC18F6490	0000 0110 101	0 0110
PIC18F8390	0000 1011 100	0 0110
PIC18F8490	0000 0110 100	0 0110

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F6390/6490/8390/8490 silicon.

1. Module: Master Synchronous Serial Port (MSSP)

Configured in SPI Slave mode, the MSSP will generate a write collision if SSPBUF is updated and the previous SSPBUF contents have not been transferred to the shift register.

Reinitializing the MSSP – by clearing and setting the SSPEN bit (SSPCON1<5>) prior to rewriting SSPBUF – will *not* prevent the error condition.

Work around

Prior to updating the SSPBUF register with a new value, verify that the previous contents have been transferred by reading the BF bit (SSPSTAT<0>). If the previous byte has *not* been transferred:

- Update SSPBUF
- If necessary, clear the WCOL bit (SSPCON1<7>)

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Master Synchronous Serial Port (MSSP) – Serial Peripheral Interface (SPI)

In SPI mode, the Buffer Full flag (BF bit in the SSPSTAT register), the Write Collision Detect bit (WCOL in SSPCON1) and the Receive Overflow Indicator bit (SSPOV in SSPCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPCON1 register).

For example, if SSPBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

Work around

If the buffer is full, before disabling the MSSP module, ensure that:

- SSPBUF is read (thus clearing the BF flag)
- WCOL is clear

If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Master Synchronous Serial Port (MSSP) – I^{2}C™

In the 10-Bit Slave mode, the I^{2}C™ mode does not work correctly.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Master Synchronous Serial Port (MSSP) – I^{2}C

When configured for I^{2}C slave reception, the MSSP module may not receive the correct data in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer (SSPBUF) register is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I^{2}C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).

- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

<u>Rev A Document (11/2009)</u>
First release of this document. Includes silicon issues 1 (MSSP), 2 (MSSP – SPI) and 3-4 (MSSP – I^{2}C).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

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- Microchip is willing to work with the customer who is concerned about the integrity of their code.

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03/26/09