

# FQD13N10L / FQU13N10L

## N-Channel QFET MOSFET

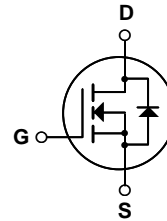
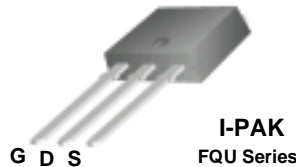
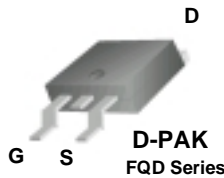
100 V, 10 A, 180 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- 10 A, 60 V,  $R_{DS(on)} = 180 \text{ m}\Omega$  (Max) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 5.0 \text{ A}$
- Low Gate Charge (Typ. 8.7 nC)
- Low Crss (Typ. 20 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	FQD13N10L / FQU13N10L	Unit
$V_{DSS}$	Drain-Source Voltage	100	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	10	A
		6.3	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	40	A
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	95	mJ
$I_{AR}$	Avalanche Current (Note 1)	10	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above 25°C	40	W
		0.32	W/°C
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	°C
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	3.13	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

\* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.09	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 5.0\text{ A}$	--	0.142	0.18	$\Omega$
		$V_{GS} = 5\text{ V}, I_D = 5.0\text{ A}$	--	0.158	0.2	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 30\text{ V}, I_D = 5.0\text{ A}$ (Note 4)	--	8.7	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	400	520	pF
$C_{oss}$	Output Capacitance		--	95	125	pF
$C_{rss}$	Reverse Transfer Capacitance		--	20	25	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 12.8\text{ A},$ $R_G = 25\ \Omega$	--	7.5	25	ns	
$t_r$	Turn-On Rise Time		--	220	450	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4, 5)	--	22	55	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	72	150	ns
$Q_g$	Total Gate Charge	$V_{DS} = 80\text{ V}, I_D = 12.8\text{ A},$ $V_{GS} = 5\text{ V}$	--	8.7	12	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4, 5)	--	2.0	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4, 5)	--	5.3	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	10	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	40	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 12.8\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	75	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	0.17	--	$\mu\text{C}$

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 1.43\text{ mH}, I_{AS} = 10\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 12.8\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

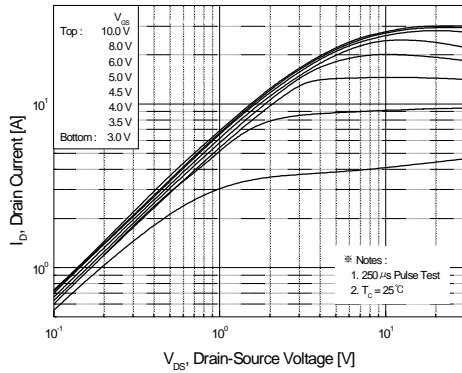


Figure 1. On-Region Characteristics

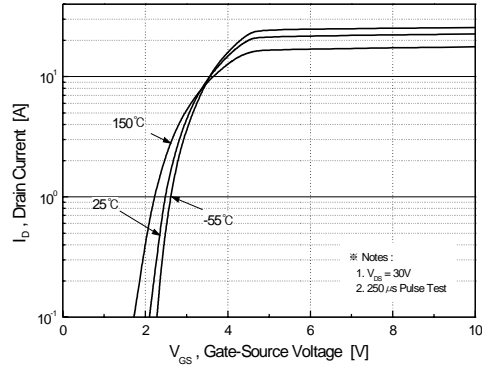


Figure 2. Transfer Characteristics

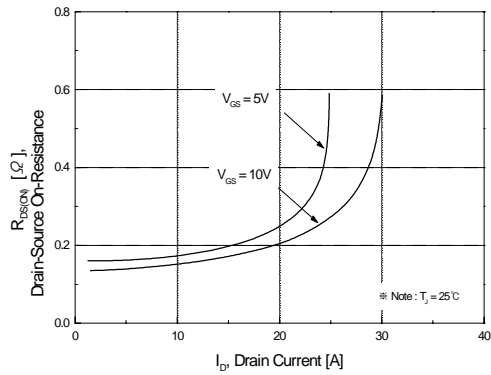


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

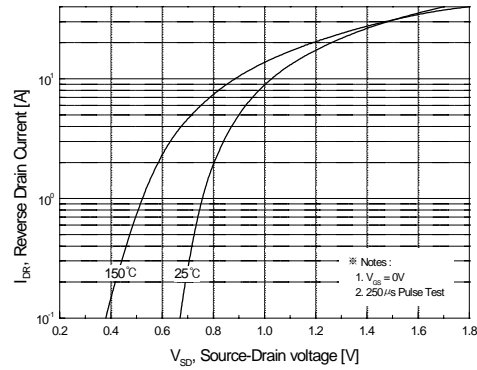


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

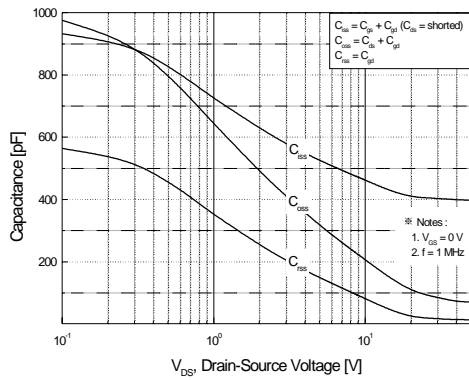


Figure 5. Capacitance Characteristics

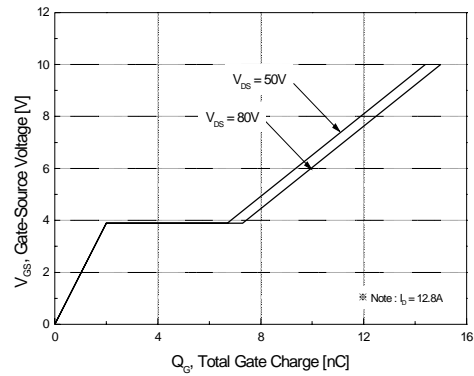
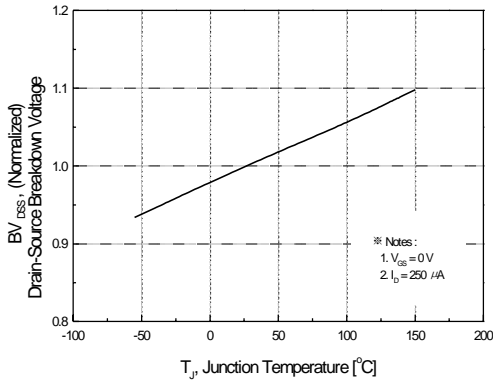
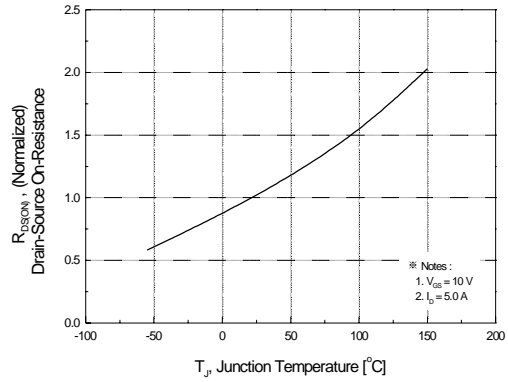


Figure 6. Gate Charge Characteristics

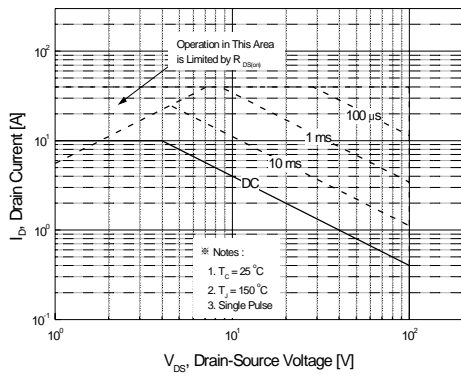
**Typical Characteristics** (Continued)



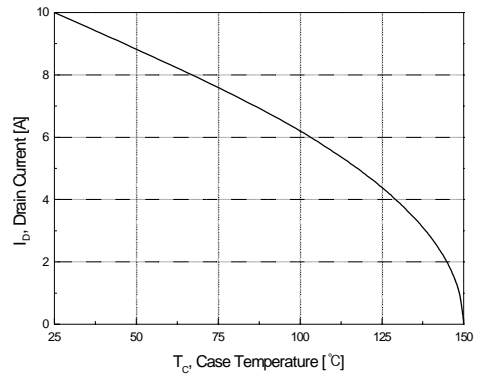
**Figure 7. Breakdown Voltage Variation vs. Temperature**



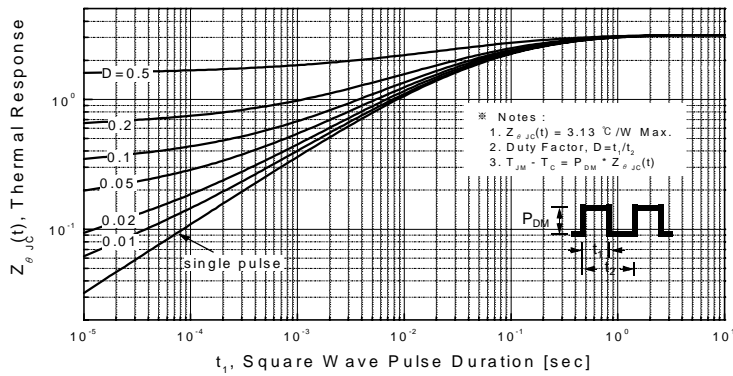
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

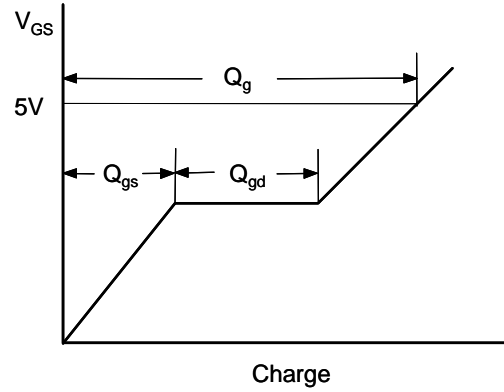
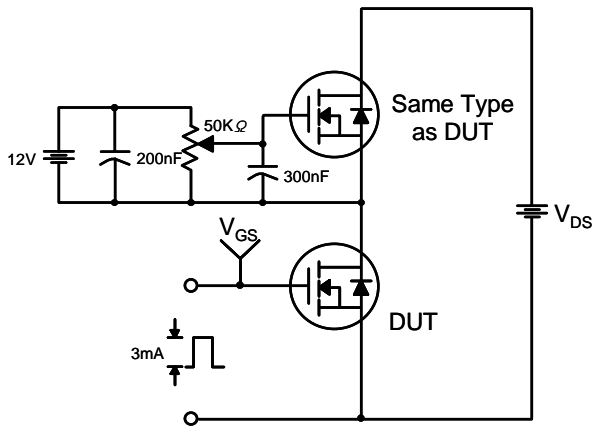


**Figure 10. Maximum Drain Current vs. Case Temperature**

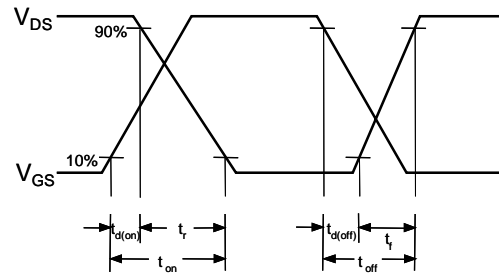
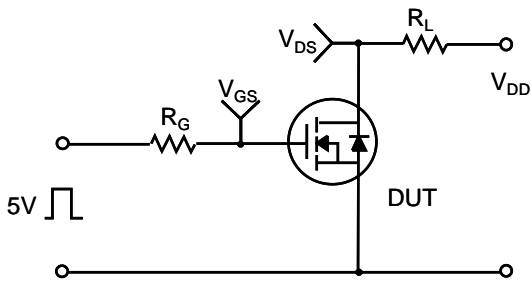


**Figure 11. Transient Thermal Response Curve**

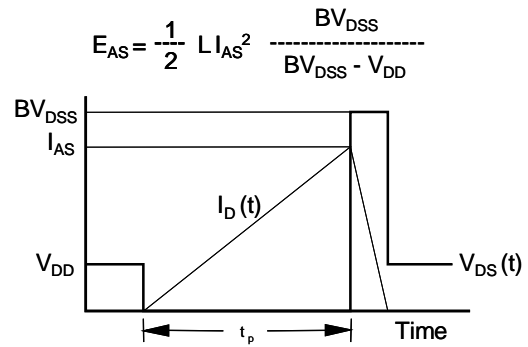
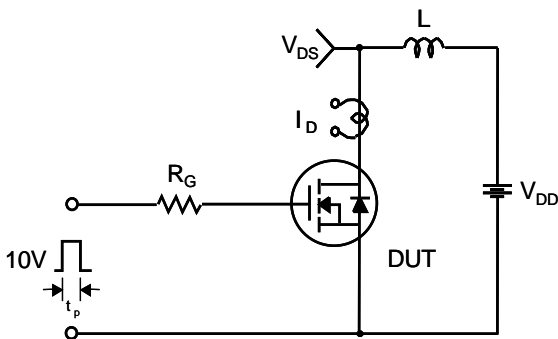
**Gate Charge Test Circuit & Waveform**



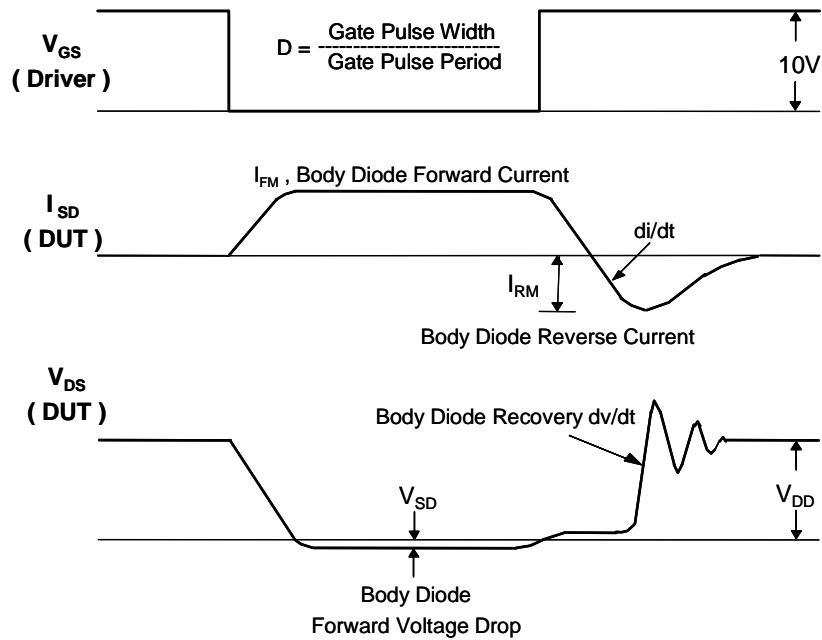
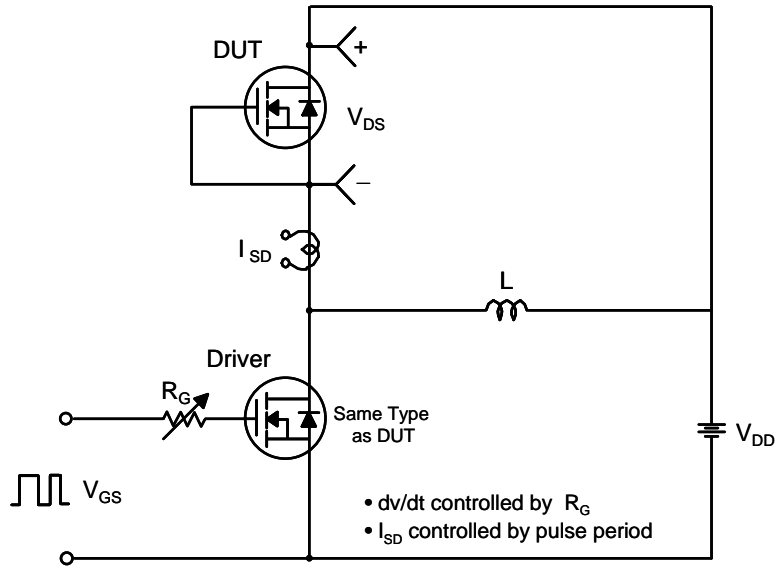
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

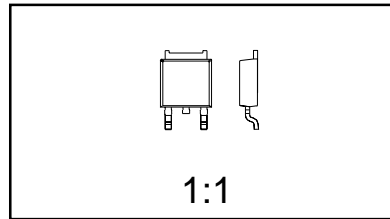
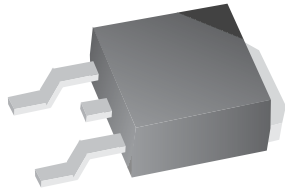


Peak Diode Recovery dv/dt Test Circuit & Waveforms



**Package Dimensions**

**TO-252 (DPAK) (FS PKG Code 36)**

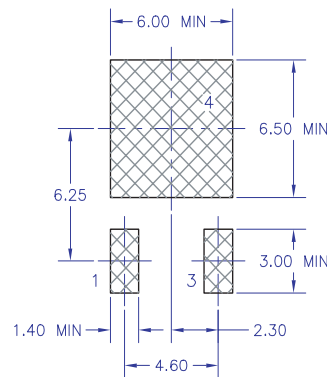
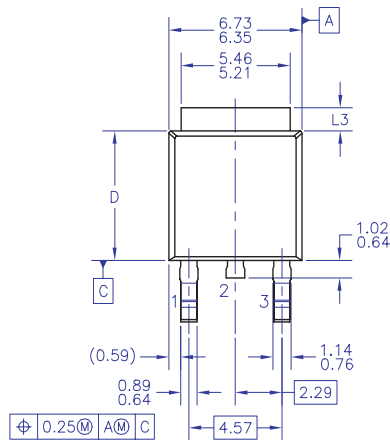


1:1

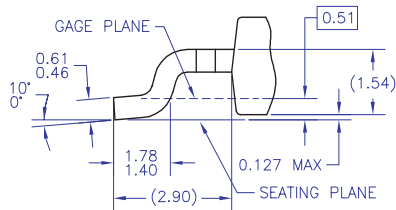
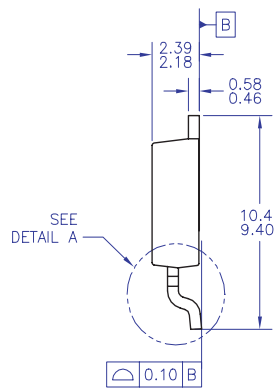
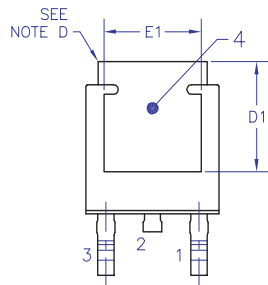
Scale 1:1 on letter size paper

Dimensions shown below are in:  
millimeters

Part Weight per unit (gram): 0.33



LAND PATTERN RECOMMENDATION



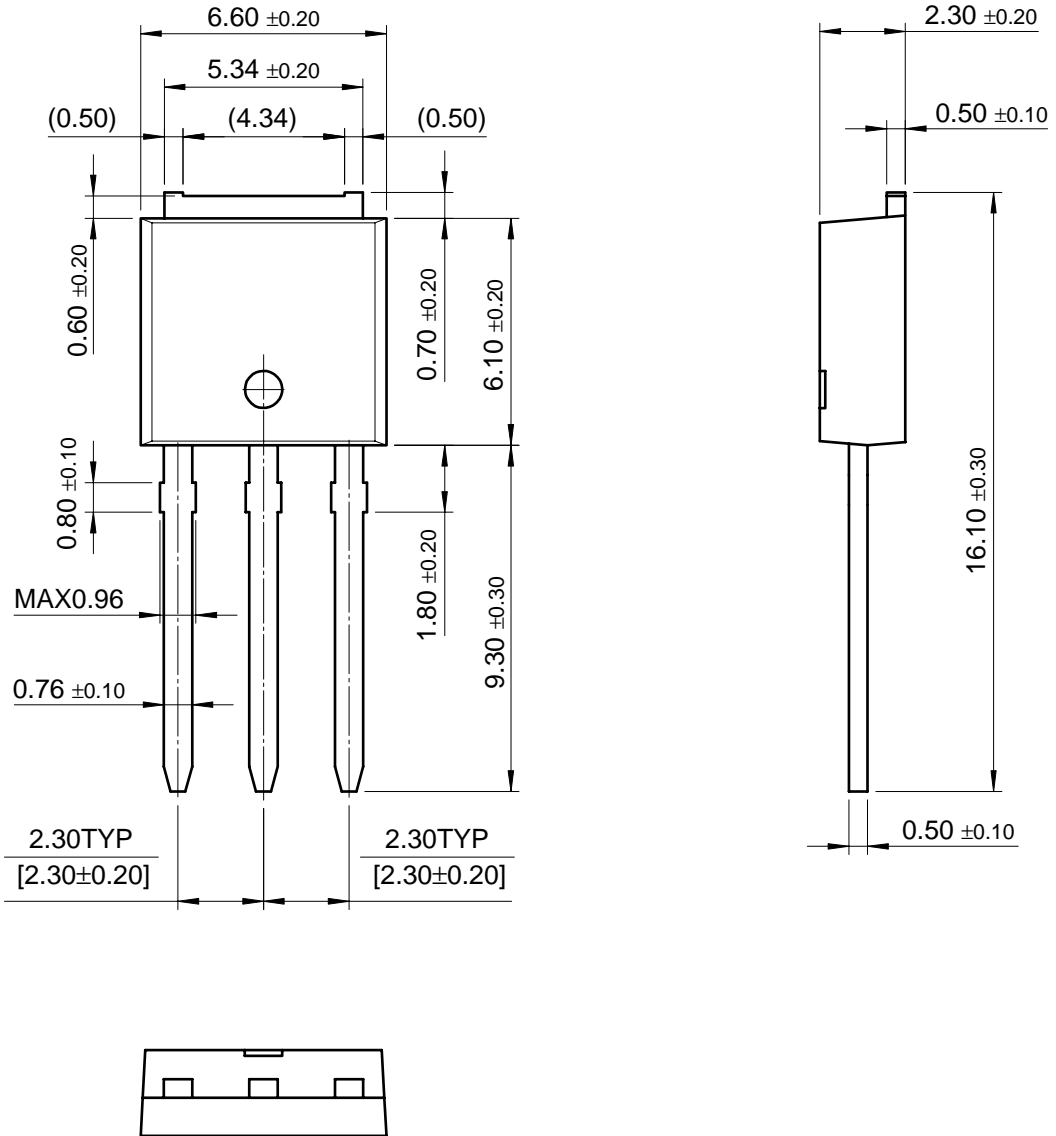
DETAIL A  
(ROTATED -90°)  
SCALE: 12X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89-1.27	1.52-2.03
D	5.97-6.22	5.33-5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

Package Dimensions (Continued)

IPAK









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	QFET®	
	QS™	
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	SuperFET®	
	SuperSOT™-3	
	SuperSOT™-6	
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- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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