KS8737

3.3V 10/100BaseTX/FX MII Physical Layer Transceiver

Rev 3.11

General Description

Operating at 3.3 Volts to meet low voltage and low power requirement, the KS8737 is a 10/100BaseTX/FX Physical Layer Transceiver which provides MII interface to transmit and receive data. It contains the 100BaseTX/FX Physical Medium Attachment (PMA), Physical Medium Dependent (PMD), and Physical Coding Sub-layer (PCS) functions. Moreover, the KS8737 has on-chip 10BaseT encoder/decoder and output filtering, which eliminates the need for external filters and makes possible a single set of line magnetics to be used to meet requirement for both 100BaseTX/FX and 10BaseT.

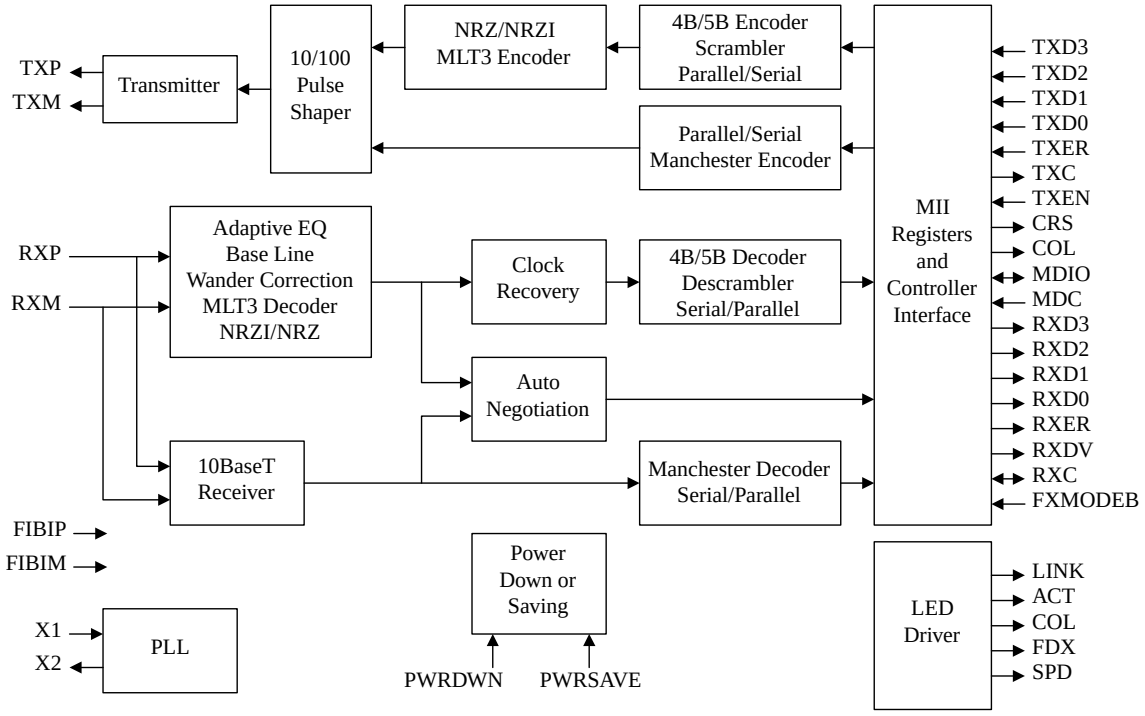
The KS8737 can automatically configure itself for 100 or 10 Mbps and full or half duplex operation, using on-chip Auto-Negotiation algorithm. It's an ideal choice of physical layer transceiver for 100BaseTX/100BaseFX/10BaseT applications.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

Features

- Single chip 100BaseTX/100BaseFX/10BaseT physical layer solution
- 3.3V CMOS design, 70mA operating current (excluding transmit output driver current)
- Fully compliant to IEEE 802.3u standard
- Support Media Independent Interface (MII) mode
- Support 10BaseT, 100BaseTX and 100BaseFX Fiber Channel with Far_End_Fault Detection
- Support power down mode and power saving mode
- Configurable through MII serial management ports or via external control pins
- Support auto-negotiation and manual selection for 10Mbps or 100Mbps speed
- Support auto-negotiation and manual selection for full- and half-duplex mode
- Standard CSMA/CD or full-duplex operation at 10Mbps or 100Mbps
- On-chip built-in filtering for both 100BaseTX and 10BaseT

Functional Diagram



Features (continued)

- LED outputs for link, activity, full/half duplex, collision and speed
- Supports back to back FX to TX for media converter applications
- Available in 64-pin TQFP surface mount package (10 mm × 10 mm × 1.0 mm)

Ordering Information

Part Number	Temperature Range	Package
KS8737	0°C to +70°C	64-Pin TQFP

Revision History

Revision	Date	Summary of Changes
3.0	7/01/02	Update to company logo and format. Add new feature on pin 33(DISTX/LPBK); disable the transmit only during media converter mode and select the loopback mode with TST2 pin. Change RXC type from I/O to O. Change the Register 1fh.9 to reserved. Change the Register 1fh.5 mode from RW to RO. Update on the 10/100BT MII receiving timing. Change on register 1fh.1 to reserved. Add the fiber mode description.
3.1	4/01/03	Change the company logo, legal disclaimer, contact info.
3.11	8/29/03	Convert to new format.

Table Of Contents

Pin Description

Pin Number	Pin Name	Type(Note 1)	Pin Function
1	CRS	O	MII Carrier Sense Output. Active High. High impedance when PHY is isolated.
2	INTRPT		I/O Interrupt Output. This pin requires an external 10k pull-up resistor. This pin becomes an I/O pin for factory testing in the test mode.
3	RXENB	I/O	MII Receive Enable Input. Active Low. If this pin is High, the Receive output of MII (RXD[3:0], RXDV, RXER, RXC) will be in tri-state. This pin becomes an I/O pin for factory testing in the test mode.
4	PHYAD4	I/O	PHY Address Bit [4] Input. This pin becomes an I/O pin for factory testing in the test mode.
5	PHYAD3	I/O	PHY Address Bit [3] Input. This pin becomes an I/O pin for factory testing in the test mode.
6	PHYAD2	I/O	PHY Address Bit [2] Input. This pin becomes an I/O pin for factory testing in the test mode.
7	PHYAD1	I/O	PHY Address Bit [1] Input. This pin becomes an I/O pin for factory testing in the test mode.
8	PHYAD0	I/O	PHY Address Bit [0] Input. This pin becomes an I/O pin for factory testing in the test mode.
9, 19, 24, 37, 53	VDD	P	3.3V power supply
10, 22, 26, 31, 43, 52, 63	GND	GND	Ground.
11	X2	O	Crystal Oscillator Output. This pin is connected to the other terminal of the 25MHz crystal. If X1 is driven by an external clock, X2 must be left open.
12	X1	I	Crystal Oscillator Input. Input for a crystal or an external 25MHz clock.
13	FDX	I/O	Full-Duplex Input. If this pin is High, it sets full-duplex operation. If this pin is Low, it sets half duplex operation. The input signal of this pin is latched at reset. After reset, this pin becomes test pin for factory test.
14 15	MODE0 MODE1	I/O	Mode Select Input. These pins carry encoded input signals that are latched at reset and power up to set mode of operation. After reset, they become test pins for factory test. These pins are I/O pins in the test mode.
16	RSTB*	I	Hardware Reset Input. Active Low signal. It forces the device to a known state. Internal 100kΩ pull-up.
17,35, 36	NC		No Connect.
33	DISTX/LPBK	I	Disable transmit Input. If this pin is high, it disables transmit only during the Media converter mode. Floating is for normal operation. The DISTX/LPBK pin also selects several functions together with the TST2 pin.

LPBK/DISTX	TST2	
High	High	Disable Transmit
High	Float	Local Loopback
Low	High	Remote Loopback
Low	Float	Remote Loopback

18	FXSD	I	Fiber Signal Detect. To detect fiber signal. Left open when not in use.
20	PWRSAVE/ FXSD_THD	I	Power Saving Mode Initialization Input. (Affecting Register 1f.15). To disable power saving mode, tie this pin low; otherwise, power saving mode is asserted. This pin can also be used to set FX signal detect threshold in fiber mode.

Note 1. P = power supply
G = ground
I = input
O = output
I/O = bi-directional

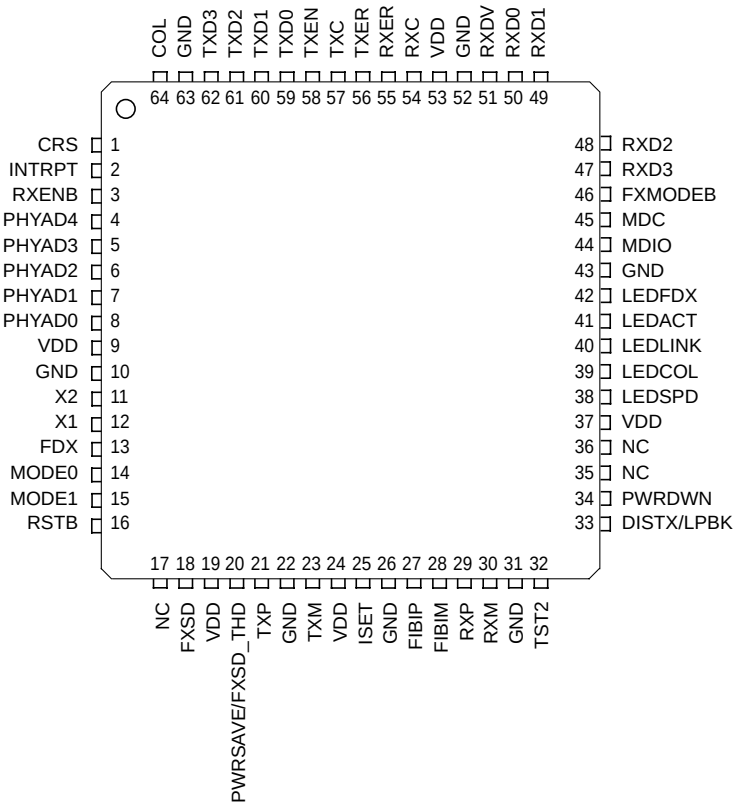
Pin Number	Pin Name	Type(Note 1)	Pin Function
21 23	TXP TXM	O	Twisted Pair Transmit Outputs. Differential transmit outputs for 100BaseTX or 10BaseT to magnetic.
25	ISET	O	Transmit Current Set. Connecting an external reference resistor to set transmitter output current. This pin connected to a 22.1kΩ 1% resistor to ground if a transformer of 1:1 turns ratio is used.
27 28	FIBIP FIBIM	I	Fiber Receive Inputs. Differential pseudo-ECL receive pairs compatible with standard fiber transceiver for 100BaseFX. Both pins should be tied to ground if not used or if not in the FX mode.
29 30	RXP RXM	I	Twisted Pair Receive Input. Differential receive input pins for 100BaseTX or 10BaseT from the magnetics.
32	TST2	I	Test Pin. During normal operation this pin should be left open. When tied high through a 1k resistor the chip will operate in back to back TX to FX mode. In this case, TXC becomes an input pin.
34	PWRDWN	I	Power Down Select Input. When this pin is tied high, the chip is in power down mode. When this pin is open or tied low, the chip is in normal operation..
38	LEDSPD	I/O	LED Output. During normal operation, this pin lights the SPEED LED to indicate 100Mbps is selected. This pin becomes an I/O pin for factory testing in the test mode. Active Low.
39	LEDCOL	I/O	LED Output. During normal operation, this pin lights the COL LED to indicate a collision. It will flash at a rate of 50ms high and 50ms low when active. This pin becomes an I/O pin for factory testing in the test mode. Active Low.
40	LEDLINK	I/O	LED Output. During normal operation, this pin lights the LINK LED to indicate a good link is detected. This pin becomes an I/O pin for factory testing in the test mode. Active Low.
41	LEDACT	I/O	LED Output. During normal operation, this pin lights the Activity LED when transmitting or receiving. It will flash at a rate of 50ms high and 50ms low when active. This pin becomes an I/O pin for factory testing in the test mode. Active Low.
42	LEDFDX	I/O	LED Output. During normal operation, this pin lights the FDX LED to indicate a full-duplex mode. This pin becomes an I/O pin for factory testing in the test mode. Active Low.
44	MDIO	I/O	Serial Management Data Input/Output. This pin requires an external 10k pull-up resistor.
45	MDC	I	Serial Management Interface Clock Input. This pin is synchronous to the MDIO data interface.
46	FXMODEB	I	FX Mode Select Input. Active Low. When this pin is low, the KS8737 is in the 100BaseFX mode.
47 48 49 50	RXD3 RXD2 RXD1 RXD0	O	MII Receive Data Output. Active High, clocked out on the falling edge of RXCLK. RXD0 is the LSB. High impedance when PHY is isolated or if RXEN is de-asserted.
51	RXDV/ CRSDV	O	MII Receive Data Valid Output. Active High, clocked out on the falling edge of RXCLK. This signal indicates that recovered and decoded data nibbles are being presented synchronously to RXCLK. High impedance when PHY is isolated or if RXEN is de-asserted.
54	RXC	O	MII Receive Clock Output. 25MHz in 100BaseTX mode, 2.5MHz in 10BaseT nibble mode. High impedance when PHY is isolated or if RXEN is de-asserted.

Note 1. P = power supply
G = ground
I = input
O = output
I/O = bi-directional

Pin Number	Pin Name	Type(Note 1)	Pin Function
55	RXER	O	MII Receive Error Output. Driven High synchronously on the falling edge of RXCLK when invalid symbol has been detected in 100BaseTX mode. This pin is ignored in 10BaseT operation. High impedance when PHY is isolated
56	TXER	I	MII Transmit Error Input. A High on this pin causes the 4B/5B encode process to substitute the Transmit Error code-group for the encoded data word. This pin is ignored in a 10BaseT operation. When TXER is not used, this pin should be tied Low through a 10kΩ resistor.
57	TXC	I/O	MII Transmit Clock Output / Back to Back Mode Clock Input. During normal operation TXC is an output pin. It provides 25MHz in 100BaseTX mode, 2.5MHz in 10BaseT nibble mode. In back to back mode it becomes an input pin. High impedance when PHY is isolated.
58	TXEN	I/O	MII Transmit Enable Input. A High on this pin causes the transmit data TXD[3:0] to be encoded and scrambled for transmission.
59 60 61 62	TXD0 TXD1 TXD2 TXD3	I	MII Transmit Data Input. TXD0 is the LSB. High impedance when PHY is isolated.
64	COL	O	MII Collision Detect Output. Active High. High impedance when PHY is isolated. This signal is de-asserted in full-duplex operation.

Note 1. P = power supply
G = ground
I = input
O = output
I/O = bi-directional

Pin Configuration



64-Pin TQFP (TQ)

Functional Description

100BaseTX Transmit

The 100BaseTX transmit function performs parallel to serial conversion, NRZ to NRZI conversion, MLT-3 encoding and transmission. The circuit starts with a parallel to serial conversion, which converts the 25 MHz, 4-bit nibbles into a 125 MHz serial bit stream. The incoming data is clocked in at the positive edge of the TXC signal. The serialized data is further converted from NRZ to NRZI format, then transmitted in MLT3 current output. The output current is set by an external 1% 22.1kΩ resistor for the 1: 1 transformer ratio. It has a typical rise/fall times of 4 ns and is complied to the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitters. The wave-shaped 10BaseT output driver is also incorporated into the 100BaseTX driver, and the total output capacitance is typical 7pF with short PC board traces assumed.

100BaseTX Receive

The 100BaseTX receive function performs adaptive equalization, DC restoration, MLT-3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, and serial to parallel conversion. The receiving side starts with the equalization filter to compensate inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristic to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self adjust against the environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate effect of base line wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. Finally, the NRZ serial data is converted to 4-bit parallel 4B nibbles. A synchronized 25MHz RXC is generated so that the 4B nibbles is clocked out at the negative edge of RCK25 and is valid for the receiver at the positive edge. When no valid data is present, the clock recovery circuit is locked to the 25MHz reference clock and both TXC and RXC clocks continue to run.

PLL Clock Synthesizer

The KS8737 generates 125MHz, 25MHz and 20MHz clocks for system timing. An internal crystal oscillator circuit provides the reference clock for the synthesizer.

Scrambler/De-scrambler (100BaseTX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The KS8737 provides a scrambler-bypass mode for testing purpose. Bypassing the scrambler causes the PCS-layer encoder to be bypassed such that the MII is operated in the 5B mode.

10BaseT Transmit

When TXEN (transmit enable) goes high, data encoding and transmission will begin. The KS8737 will continue to encode and transmit data as long as TXEN remains high. The data transmission will end when TXEN goes low. The last transition occurs at the boundary of the bit cell if the last bit is zero, or at the center of the bit cell if the last bit is one. The output driver is incorporated into the 100Base driver to allow transmission with the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with typical 2.5V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10BaseT Receive

On the receive side, input buffer and level detecting squelch circuit are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8737 decodes a data frame. This activates the carrier sense (CRS) ad RXDV signals and makes the receive data (RXD) available. The receive clock is maintained active during idle periods in between data reception. The KS8737 supports extended length cables for 10BaseT by selecting a lower squelch level around 150mV.

SQE and Jabber Function (10BaseT only)

In 10BaseT operation, a short pulse will be put out on the COL pin after each packet is transmitted. This is required as a test of the 10BaseT transmit/receive path and is called SQE test. The 10BaseT transmitter will be disabled and COL will go High if TXEN is High for more than 46 us (Jabbering) If TXEN then goes Low for more than 368 us, the 10BaseT transmitter will be re-enabled and COL will go Low.

Auto-Negotiation

The KS8737 performs auto-negotiation by hardware (mode[1:0]) or software (Register 0.12). It will automatically choose its mode of operation by advertising its abilities and comparing them with those received from its link partner whenever auto-negotiation is enabled. It can also be configured to advertise 100BaseTX or 10BaseT in either full- or half-duplex mode. The auto-negotiation is disabled in the FX mode.

During auto-negotiation, the contents of Register 4, coded in Fast Link Pulse (FLP), will be sent to its link partner under the conditions of power-on, link-loss or re-start. At the same time, the KS8737 will monitor incoming data to determine its mode of operation. Parallel detection circuit will be enabled as soon as either 10BaseT idle or 100BaseTX idle is detected. The operation mode gets configured based on the following priority:

Priority 1: 100BaseTX, Full-duplex

Priority 2: 100BaseTX, Half-duplex

Priority 3: 10BaseT, Full-duplex

Priority 4: 10BaseT, Half-duplex

When the KS8737 receives a burst of FLP from its link partner with 3 identical link code words (ignoring acknowledge bit), it will store these code words in Register 5 and wait for the next 3 identical code words. Once the KS8737 detects the second code words, it then configures itself according to above-mentioned priority. In addition, the KS8737 also checks 100BaseTX idle or 10BaseT NLP symbol. If either is detected, the KS8737 automatically configures to match the detected operating speed.

MII Management Interface

The KS8737 supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KS8737. The MDIO interface consists of the following:

- A physical connection including a data line (MDIO), a clock line (MDC) and an optional interrupt line (INTRPT)
- A specific protocol which runs across the above-mentioned physical connection and allows one controller to communicate with multiple KS8737 devices. Each KS8737 assigned an MII address between 0 and 31 by the PHYAD inputs.
- An internal addressable set of fourteen 16-bit MDIO registers. Register [0:6] are required and their functions are specified by the IEEE 802.3 specifications. Additional registers are provided for expanded functionality.

The INTPRT pin functions as a management data interrupt in the MII. An active Low or High in this pin indicates a status change on the KS8737 based on 1fh.14 level control. Register 1bh[15:8] are the interrupt enable bits. Register 1bh[7:0] are the interrupt conditions bits. The interrupt is activated when changes made to the following conditions:

- Link Status
- Duplex Status

Reading Register 1bh clears this interrupt.

MII Data Interface

The data interface consists of separate channels for transmitting data from a 10/100 802.3 compliant Media Access Controller (MAC) to the KS8737, and for receiving data from the line. Normal data transmission is implemented in 4B Nibble Mode (4-bit wide nibbles).

Transmit Clock (TXC): The transmit clock is normally generated by the KS8737 from an external 25MHz reference source at the X1 input. The transmit data and control signals must always be synchronized to the TXC by the MAC. The KS8737 normally samples these signals on the rising edge of the TXC.

Receive Clock (RXC): For 100BaseTX links, the receive clock is continuously recovered from the line. If the link goes down, and auto-negotiation is disabled, receive clock operates off the master input clock (X1 or TXC). For 10BaseT links, received is recovered from the line while carrier is active, and operates from the master input clock when the line is idled. The KS8737 synchronizes the receive data and control signals on the falling edge of RXC in order to stabilize the signals at the rising edge of the clock with 10ns setup and hold times.

Transmit Enable: The MAC must assert TXEN the same time as the first nibble of preamble, and de-assert TXEN after the last bit of the packet.

Receive Data Valid: The KS8737 asserts RXDV when it receives a valid packet. Line operating speed and MII mode will determine timing changes in the following way:

- For 100BaseTX link with the MII in 4B mode, RXDV is asserted from the first nibble of preamble to the last nibble of the data packet.
- For 10BaseT links, the entire preamble is truncated. RXDV is asserted with the first nibble of the SFD " 5D" and remains asserted until the end of the packet.

Error Signals: Whenever the KS8737 receives an error symbol from the network, it asserts RXER and drives “1110” (4B) on the RXD pins. When the MAC asserts TXER, the KS8737 will drive “H” symbols out on the line.

Carrier Sense (CRS): For 100TX links, a start-of-stream delimiter, or /J/K symbol pair causes assertion of Carrier Sense (CRS). An end-of-stream delimiter, or /T/R symbol pair causes de-assertion of CRS. The PMA layer will also de-assert CRS if IDLE symbols are received without /T/R, yet in this case RXER will be asserted for one clock cycle when CRS is de-asserted. For 10T links, CRS assertion is based on reception of valid preamble, and de-assertion on reception of an end-of-frame (EOF) marker.

Collision: Whenever the line state is half-duplex and the transmitter and receiver are active at the same time, the KS8737 asserts its collision signal which is asynchronous to any clock.

Power Management

The KS8737 offers the following modes for power management:

- Power Down Mode: This mode can be achieved by writing to Register 0.11 or pulling pin PWRDWN High.
- Power Saving Mode: This mode can be enabled by writing to Register 1fh.15. or using an external initialization pin. The KS8737 will then turn off everything except for the Energy Detect and PLL circuits when the cable is not installed. In other words, the KS8737 will shutdown most of the internal circuits to save power if there is no link.

Fiber Mode

Fiber mode is activated by setting FXMODEB (pin46) low. Under this mode, the FIBP/M are become the receiving port, and the TXP/M are the transmit port. FXSD (+) and FXSD_THD (-) are used as differential signal for Fiber signal detect port. If driven single-ended with FXSD and FXSD_THD should be set by an external voltage divider for the proper reference voltage, there is no internal voltage for this pin.

Under Fiber mode, the link is up only when FXSD>FXSD_THD and the proper idle pattern is received. If FXSD<FXSD_THD, then a Far-end-fault (FEF) pattern will be sent out. The link partner that receives FEF will have its link turn off. The link partner, however, will still send the normal transmission while receiving FEF. This feature can be turned off by setting the Pin 17 low.

Media Converter Mode

The KS8737 provides a special fiber mode in which allows back-to-back FX to TX media conversion using two KS8737’s. This special mode can be activated by pulling pin 32 high through an external 1k resistor. The detailed connection between the two KS8737’s is shown in the application circuit on the data sheet. In this case TXC become an input pin. The internal FIFO’s will take care of the transition of the receive to transmit clock domain changes. The KS8737 in media converter mode can also handle the jumbo frames. The recovered clock and parallel data (RXC, RXD[0:3]) from the other chip will feed the chip through TXC and TXD[0:3].

Under the Media Converter mode, the KS8737 support disable transmit feature by pull-up on DSITX/LPBK (pin 33) pin. For more details, see *“Pin Description”* section.

Register Map

Register No.	Description
0h	Basic Control Register
1h	Basic Status Register
2h	PHY Identifier I
3h	PHY Identifier II
4h	Auto-Negotiation Advertisement Register
5h	Auto-Negotiation Link Partner Ability Register
6h	Auto-Negotiation Expansion Register
7h	Auto-Negotiation Next Page Register
15h	RXER Counter Register
1bh	Interrupt Control/Status Register
1ch	Reserved
1dh	Reserved
1eh	Reserved
1fh	100BaseTX PHY Control Register

Address	Name	Description	Mode(Note 1)	Default
Register 0h - Basic Control				
0.15	Reset	1 = software reset. Bit is self-clearing	RW/SC	0
0.14	Loopback	1 = loopback mode 0 = normal operation	RW	0
0.13	Speed Select	1 = 100Mbps 0 = 10Mbps Ignored if Auto-Negotiation is enabled (0.12 = 1)	RW	Set by MODE Selection Table
0.12	Auto-Negotiation Enable	1 = enable auto-negotiation process (override 0.13 and 0.8) 0 = disable auto-negotiation process	RW	Set by MODE Selection Table
0.11	Power Down	1 = power down mode 0 = normal operation	RW	0
0.10	Isolate	1 = electric isolation of PHY from MII and TXP/TXM 0 = normal operation	RW	Set by MODE Selection Table
0.9	Restart Auto-Negotiation	1 = restart auto-negotiation process 0 = normal operation. Bit is self-clearing	RW/SC	0
0.8	Duplex Mode	1 = full-duplex 0 = half duplex	RW	Set by FDX (pin 13)
0.7	Collision Test	1 = enable COL test 0 = disable COL test	RW	0
0.6:0	Reserved		RO	0
Register 1h - Basic Status				
1.15	100BaseT4	1 = T4 capable 0 = no T4 capable	RO	0
1.14	100BaseTX Full-Duplex	1 = capable of 100BaseX full-duplex 0 = not capable of 100BaseX full-duplex	RO	1
1.13	100BaseTX Half-Duplex	1 = capable of 100BaseX half duplex 0 = not capable of 100BaseX half duplex	RO	1

Note 1. RW: Read/Write, RO: Read only, SC: Self clear, LH: Latch High, LL: Latch Low.

Address	Name	Description	Mode(Note 1)	Default
1.12	10BaseT Full-Duplex	1 = 10Mbps with full-duplex 0 = no 10Mbps with full-duplex capability	RO	1
1.11	10BaseT Half-Duplex	1 = 10Mbps with half duplex 0 = no 10Mbps with half duplex capability	RO	1
1.10:7	Reserved		RO	0000
1.6	No Preamble	1 = preamble suppression 0 = normal preamble	RO	0
1.5	Auto-Negotiation Complete	1 = auto-negotiation process completed 0 = auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = remote fault 0 = no remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = capable to perform auto-negotiation 0 = unable to perform auto-negotiation	RO	1
1.2	Link Status	1 = link is up 0 = link is down	RO/LL	0
1.1	Jabber Detect	1 = jabber detected 0 = jabber not detected. Default is Low	RO/LH	0
1.0	Extended Capability	1 = supports extended capabilities registers	RO	1
Register 2h - PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Micrel Semiconductor's OUI is 0010A1 (hex)	RO	0022h
Register 3h - PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Micrel Semiconductor's OUI is 0010A1 (hex)	RO	000101
3.9:4	Model Number	Six bit manufacturer's model number	RO	110010
3.3:0	Revision Number	Four bit manufacturer's model number	RO	0000
Register 4h - Auto-Negotiation Advertisement				
4.15	Next Page	1 = next page capable 0 = no next page capability. KS8737 supports next page capability	RW	0
4.14	Reserved		RO	00
4.13	Remote Fault	1 = remote fault supported 0 = no remote fault	RW	0
4.12:11	Reserved		RO	0
4.10	Pause	1 = pause function supported 0 = no pause function	RW	0
4.9	100BaseT4	1 = T4 capable 0 = no T4 capability	RO	0
4.8	100BaseTX Full-Duplex	1 = 100 full-duplex capable 0 = no 100 full-duplex capability	RW	Set by MODE Selection Table
4.7	100BaseTX Half-Duplex	1 = 100Mbps half-duplex capable 0 = no 100Mbps half-duplex capability	RW	Set by MODE Selection Table
4.6	10BaseT Full-Duplex	1 = 10Mbps full-duplex 0 = no 10Mbps full-duplex capability	RW	Set by MODE Selection Table
4.5	10BaseT Half-Duplex	1 = 10Mbps half-duplex capable 0 = no 10Mbps half-duplex capability	RW	Set by MODE Selection Table
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	00001

Note 1. RW: Read/Write, RO: Read only, SC: Self clear, LH: Latch High, LL: Latch Low.

Address	Name	Description	Mode(Note 1)	Default
Register 5h - Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = next page capable 0 = no next page capability KS8737 supports next page capability.	RO	0
5.14	Acknowledge	1 = link code word received from partner 0 = link code word not yet received	RO	0
5.13	Remote Fault	1 = remote fault detected 0 = no remote fault	RO	0
5.12:11	Reserved		RO	00
5.10	Pause	1 = pause function supported 0 = no pause function	RO	0
5.9	100 BaseT4	1 = T4 capable 0 = no T4 capability	RO	0
5.8	100BaseTX Full-Duplex	1 = 100Mbps full-duplex capable 0 = no 100Mbps full-duplex capability	RO	0
5.7	100BaseTX Half-Duplex	1 = 100Mbps half-duplex capable 0 = no 100Mbps half-duplex capability	RO	0
5.6	10BaseT Full-Duplex	1 = 10Mbps with full-duplex capable 0 = no 10Mbps full-duplex capability	RO	0
5.5	10BaseT Half-Duplex	1 = 10Mbps half-duplex capable 0 = no 10Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	00000
Register 6h - Auto-Negotiation Expansion				
6.15:5	Reserved		RO	0×00
6.4	Parallel Detection Fault	1 = fault detected by parallel detection 0 = no fault detected by parallel detection.	RO/LH	0
6.3	Link Partner Next Page Able	1 = link partner has next page capability 0 = link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = local device has next page capability 0 = local device does not have next page capability	RO	1
6.1	Page Received	1 = new page received 0 = new page not yet received	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = link partner has auto-negotiation capability 0 = link partner does not have auto-negotiation capability	RO	0
Register 7h - Auto-Negotiation Next Page				
7.15	Next Page	1 = additional next page(s) will follow 0 = last page	RW	0
7.14	Reserved		RO	0
7.13	Message Page	1 = message page 0 = unformatted page	RW	1
7.12	Acknowledge2	1 = will comply with message 0 = cannot comply with message	RW	0
7.11	Toggle	1 = previous value of the transmitted link code word equaled logic One 0 = logic Zero	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	0×01
Register 15h - RXER Counter				
15h.15:0	RXER Counter	RX Error counter for the RX_ER in each package	RO	0×00

Note 1. RW: Read/Write, RO: Read only, SC: Self clear, LH: Latch High, LL: Latch Low.

Address	Name	Description	Mode(Note 1)	Default
Register 1bh - Interrupt Control/Status Register				
1bh.15	Jabber Interrupt Enable	1 = Enable jabber interrupt 0 = Disable jabber interrupt	RW	0
1bh.14	Receive Error Interrupt Enable	1 = Enable receive error interrupt 0 = Disable receive error interrupt	RW	0
1bh.13	Page Received Interrupt Enable	1 = Enable page received interrupt 0 = Disable page received interrupt	RW	0
1bh.12	Parallel Detect Fault Interrupt Enable	1 = Enable parallel detect fault interrupt 0 = Disable parallel detect fault interrupt	RW	0
1bh.11	Link Partner Acknowledge Interrupt Enable	1 = Enable link partner acknowledge interrupt 0 = Disable link partner acknowledge interrupt	RW	0
1bh.10	Link Down Interrupt Enable	1 = Enable link down interrupt 0 = Disable link down interrupt	RW	0
1bh.9	Remote Fault Interrupt Enable	1 = Enable remote fault interrupt 0 = Disable remote fault interrupt	RW	0
1bh.8	Link Up Interrupt Enable	1 = Enable link up interrupt 0 = Disable link up interrupt	RW	0
1bh.7	Jabber Interrupt	1 = Jabber interrupt 0 = No jabber interrupt	RO	0
1bh.6	Receive Error Interrupt	1 = Receive error interrupt 0 = No receive error interrupt	RO	0
1bh.5	Page Receive Interrupt	1 = Page receive interrupt 0 = No page receive interrupt	RO	0
1bh.4	Parallel Detect Fault Interrupt	1 = Parallel detect fault interrupt 0 = No parallel detect fault interrupt	RO	0
1bh.3	Link Partner Acknowledge Interrupt	1 = Link partner acknowledge interrupt 0 = No link partner acknowledge interrupt	RO	0
1bh.2	Link Down Interrupt	1 = Link down interrupt 0 = No link down interrupt	RO	0
1bh.1	Remote Fault Interrupt	1 = Remote fault interrupt 0 = No remote fault interrupt	RO	0
1bh.0	Link Up Interrupt	1 = Link up interrupt 0 = No link up interrupt	RO	0
Register 1fh - 100BaseTX PHY Controller				
1fh.15	Power Saving	1 = enable power saving 0 = disable	RW	1
1fh.14	Interrupt Level	1 = interrupt pin active high 0 = active low	RW	0
1fh.13	Reserved			
1fh.12	Auto-Negotiation Complete	1 = auto-negotiation complete 0 = not complete	RO	0
1fh.11	Enable Link Fail Counter in 100BaseTX	1 = enable link fail counter 0 = disable	RW	1
1fh.10	Enable Jabber	1 = enable jabber counter 0 = disable	RW	1
1fh.9	Reserved	Reserved		
1fh.8	Enable Pause (Flow-Control Result)	1 = flow control capable 0 = no flow control	RO	0

Note 1. RW: Read/Write, RO: Read only, SC: Self clear, LH: Latch High, LL: Latch Low.

Address	Name	Description	Mode(Note 1)	Default
1fh.7	Enable SQE Test	1 = enable SQE test 0 = disable	RW	1
1fh.6	Enable Symbol Mode	1 = enable symbol mode 0 = disable	RO	0
1fh.5	Transmit Isolate	1 = isolate transmit 0 = not isolate	RO	0
1fh.4:2	Operation Mode Indication	[000] = still in auto-negotiation [001] = 10BaseT half duplex [010] = 100BaseTX half duplex [011] = default [101] = 10BaseT full-duplex [110] = 100BaseTX full-duplex [111] = PHY/MII isolate	RO	Set by MODE
1fh.1	Reserved	Reserved	RW	0
1fh.0	Disable Data Scrambling	1 = disable scrambler 0 = enable	RW	0

Note 1. RW: Read/Write, RO: Read only, SC: Self clear, LH: Latch High, LL: Latch Low.

Mode Selection for Register 1fh 4:2

KS8737 can be forced into a specific mode on reset by configuring MODE pins specified in the following table. The strapping option of MODE pins are latched on the rising edge of reset to set the default value of various registers. The values can be modified by writing into the registers.

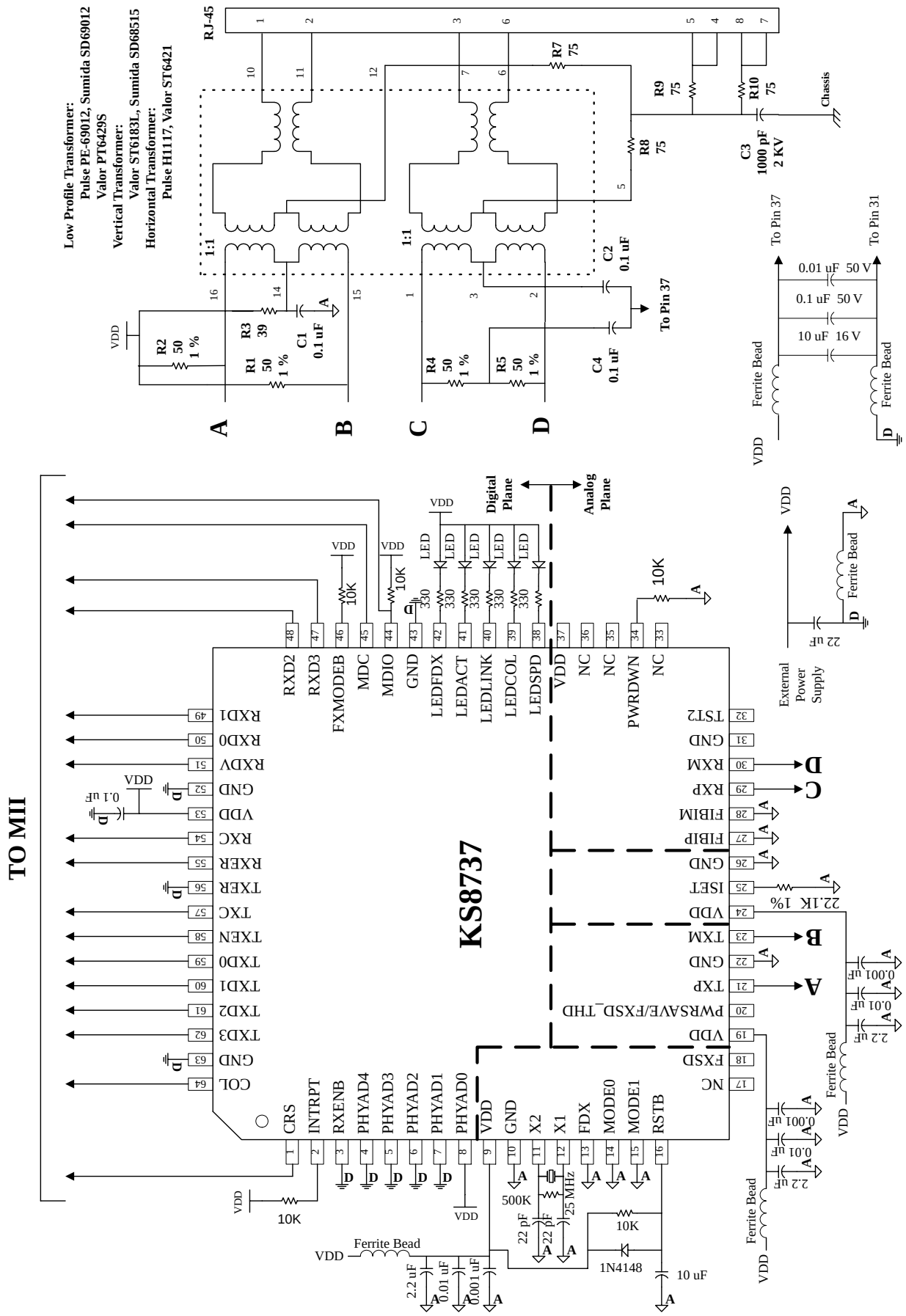
			Default Register Bit Values		
Mode (Note 1)	**FDX** (Note 2)	**Mode Definition**	**Register 0h Bit [8,10,12,16]**	**Register 4h Bit [5,6,7,8]**	**Register 1fh Bit 5**
1 0	0	Force 10BaseT Half-Duplex. No Auto-Negotiation.	0 0 0 0	1 0 0 0	0
1 0	1	Force 10BaseT Full-Duplex. No Auto-Negotiation.	1 0 0 0	1 1 0 0	0
0 1	0	Force 100BaseTX Half-Duplex. No Auto-Negotiation.	0 0 0 1	0 0 1 0	0
0 1	1	Force 100BaseTX Full-Duplex. No Auto-Negotiation.	1 0 0 1	0 0 1 1	0
Z 1	*	100 BaseTX Half & Full-Duplex Advertised via Auto-Negotiation.	* 0 1 1	0 0 1 1	0
Z 0	*	10 BaseT Half & Full-Duplex Advertised via Auto-Negotiation.	* 0 1 0	1 1 0 0	0
1 1	*	Isolated MII and TXP/TXM	* 1 0 1	0 0 0 0	1
0 0	*	All Capable Auto-Negotiation Enabled	* 0 1 0	1 1 1 1	0

Table 1. Mode Selection

Note 1. Z indicates that input is floating.

Note 2. * indicates that values are controlled by FDX.

Typical Application Circuit



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{DD}) ..... +4.0V
Supply Reference to GND ..... –0.5V to +7.0V
Input Voltage (All Inputs) ..... –0.5V to +4.0V
Output Voltage (All Outputs) ..... –0.5V to +4.0V
Lead Temperature (soldering, 10 sec.) ..... 270°C
Storage Temperature (T_S) ..... –55°C to +150°C

Operating Ratings (Note 2)

Supply Voltage (V_{DD}) ..... +3.135V to +3.465V
Ambient Temperature (T_A) ..... 0°C to +70°C
Package Thermal Resistance, **(Note 3)**
TQFP (θ_{JA}) No Air Flow ..... 53.7°C/W

Electrical Characteristics (Note 4)

V_{DD} = 3.3V ±5%; T_A = 0°C to +70°C; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Total Supply Current (including TX output driver current)						
I_{DD1}	Normal 100BaseTX			100	120	mA
I_{DD2}	Normal 10BaseT (50% utilization)			135	150	mA
I_{DD3}	Power Saving Mode 100BaseTX			80	90	mA
I_{DD4}	Power Save Mode 10BaseT			40	45	mA
I_{DD5}	Power Down Mode			9	10	mA
TTL Inputs						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current	V_{IN} = GND ~ V_{DD}	–10		10	µA
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4	V
$\|I_{OZ}\|$	Output Tr-State Leakage				10	µA
100BaseTX Receive						
V_B	RXP/RXM Input Bias Voltage			2.7		V
R_{IN}	RXP/RXM Differential Input Resistance			8		kΩ
	Propagation Delay	from magnetics to RDTX		50	110	ns
100BaseTX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	50Ω from each output to V_{DD}	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	50Ω from each output to V_{DD}			2	%
t_r, t_t	Rise/Fall Time Rise/Fall Time Imbalance		3 0		5 0.5	ns ns
100BaseTX Transmit (measured differentially after 1:1 transformer)						
	Duty Cycle Distortion				±0.5	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of ISET			1.25		V
	Propagation Delay	from TDTX to magentics		45	60	ns
	Jitters			0.7	1.4	$ns_{(pk-pk)}$

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to V_{DD}).

Note 3. No HS (heat spreader) in package.

Note 4. Specification for packaged product only.

Symbol	Parameter	Condition	Min	Typ	Max	Units
10BaseTX Receive						
V_B	RXP/RXM Input Bias Voltage			1.4		V
R_{IN}	RXP/RXM Differential Input Resistance			8		kΩ
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV
10BaseTX Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	50Ω from each output to V_{DD}	2.2		2.8	V
	Jitters Added	50Ω from each output to V_{DD}			±3.5	ns
t_r, t_t	Rise/Fall Time			25		ns
Clock Outputs						
X1, X2	Crystal Oscillator			25		MHZ
RXC_{100}	Receive Clock, 100TX			25		MHZ
RXC_{10}	Receive Clock, 10T			2.5		MHZ
	Receive Clock Jitters			3.0		$ns_{(pk-pk)}$
TXC_{100}	Transmit Clock, 100TX			25		MHZ
TXC_{10}	Transmit Clock, 10T			2.5		MHZ
	Transmit Clock Jitters			1.8		$ns_{(pk-pk)}$

Timing Diagrams

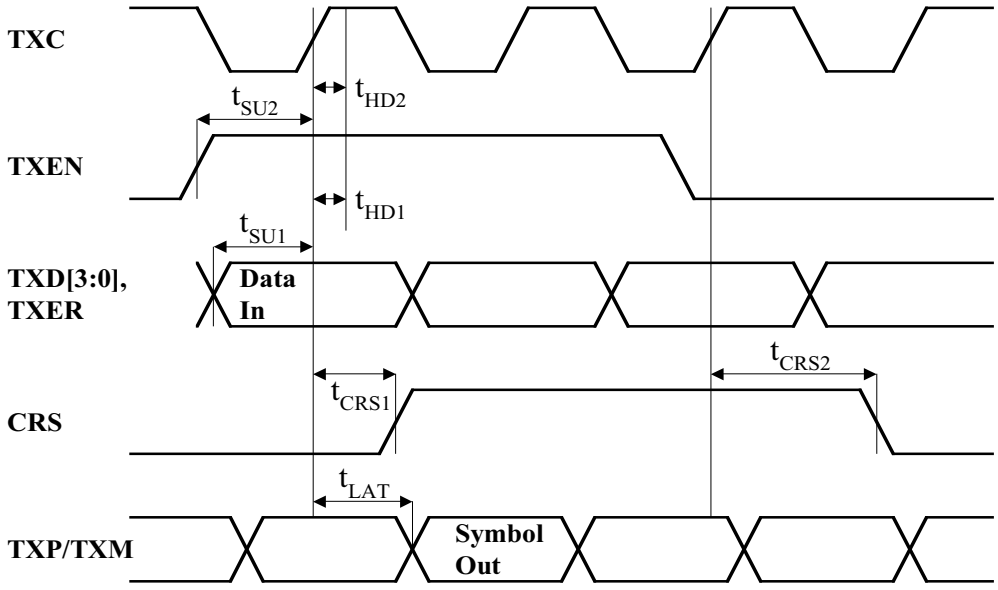


Figure 1. 10BaseT MII Transmit Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{SU1}	TXD [3:0] Set-Up to TXC High	10			ns
t_{SU2}	TXEN Set-Up to TXC High	10			ns
t_{HD1}	TXD [3:0] Hold After TXC High	0			ns
t_{HD2}	TXEN Hold After TXC High	0			ns
t_{CRS1}	TXEN High to CRS Asserted Latency			2	BT
t_{CRS2}	TXEN Low to CRS De-Asserted Latency			5	BT
t_{LAT}	TXEN High to TXP/TXM Output (TX Latency)			3	BT
t_{SQE}	COL (SQE) Delay Aftter TXEN Ae-Asserted		1.5		µs
t_{SQEP}	COL (SQE) Pulse Duration		1.0		µs

Table 2. 10BaseT MII Transmit Timing Parameters

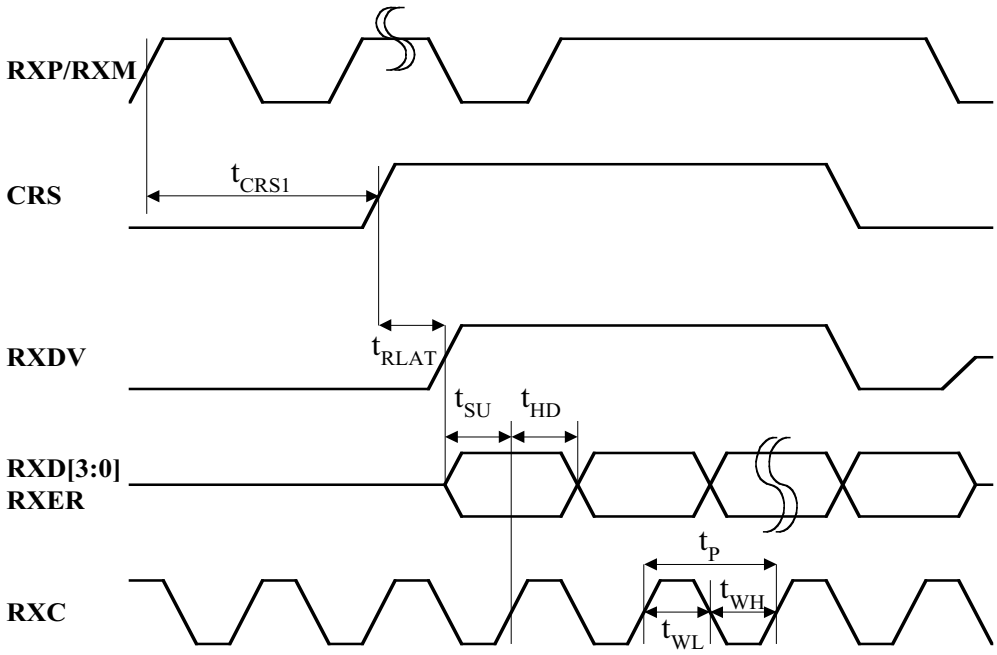


Figure 2. 10BaseT MII Receive Timing

Symbol	Parameter	Min	Typ	Max	Units
t_P	RXC Period		400		ns
t_{WL}	RXC Pulse Width		200		ns
t_{WH}	RXC Pulse Width		200		ns
t_{SU}	RXD [3:0], RXER, RXDV Set-Up to Rising Edge of RXC		200		ns
t_{HD}	RXD [3:0], RXER, RXDV Hold from Rising Edge of RXC		200		ns
t_{RLAT}	RXDV Data Vaild from CSR			6.5	µs
t_{CRS1}	RXP/RXM Preamble to CRS Asserted		5		BT

Table 3. 10BaseT MII Receive Timing Parameters

Note 1. CRS is asserted but RXD/RXDV are driven from SFD as the first byte of packet.

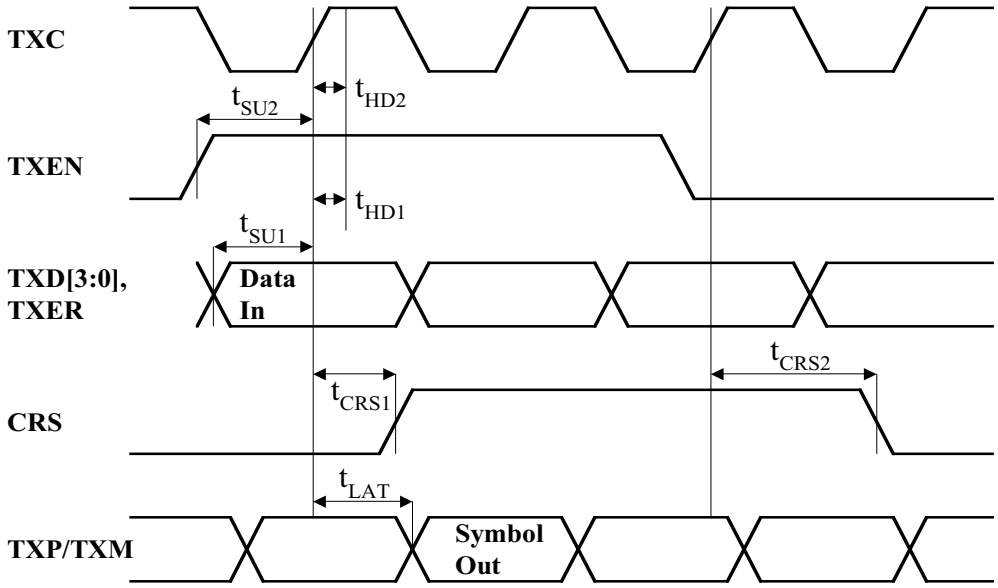


Figure 3. 100BaseT MII Transmit Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{SU1}	TXD [3:0] TXER Set-Up to TXC High	10			ns
t_{SU2}	TXEN Set-Up to TXC High	10			ns
t_{HD1}	TXD [3:0] TXER Hold After TXC High	0			ns
t_{HD2}	TXEN Hold After TXC High	0			ns
t_{CRS1}	TXEN High to CRS Asserted Latency		1		BT
t_{CRS2}	TXEN Low to CRS De-Asserted Latency		1		BT
t_{LAT}	TXEN High to TXP/TXM Output (TX Latency)		7		BT

Table 4. 100BaseT MII Transmit Timing Parameters

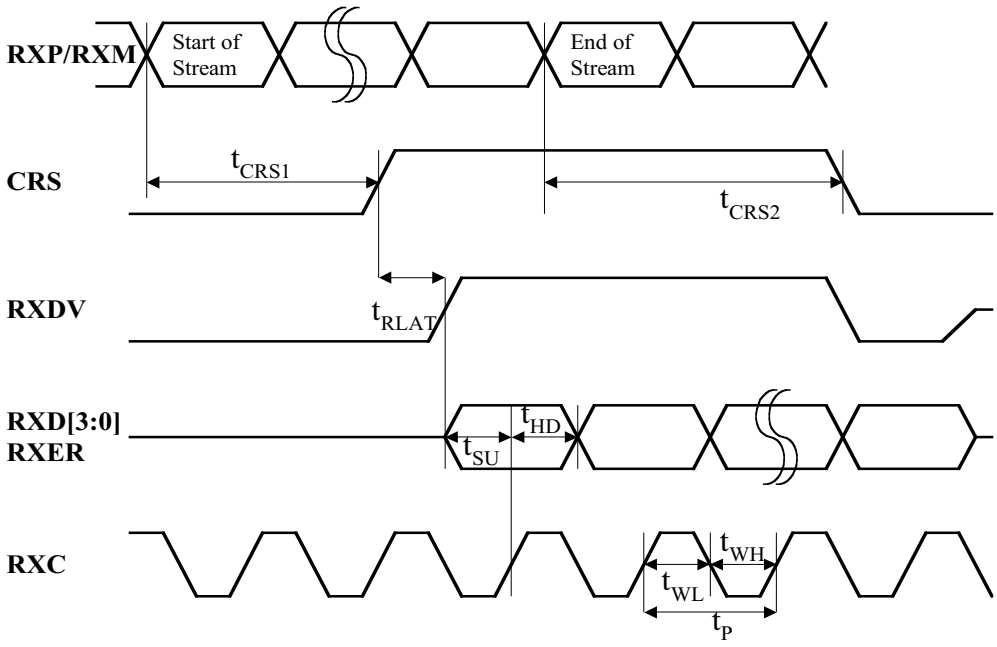


Figure 4. 100BaseT MII Receive Timing

Symbol	Parameter	Min	Typ	Max	Units
t_P	RXC Period		40		ns
t_{WL}	RXC Pulse Width	20			ns
t_{WH}	RXC Pulse Width	20			ns
t_{SU}	RXD [3:0], RXER, RXDV Set-Up to Rising Edge of RXC		20		ns
t_{HD}	RXD [3:0], RXER, RXDV Hold from Rising Edge of RXC		20		ns
t_{RLAT}	CRS to RXD Latency, 4B or 5B Aligned		4		BT
t_{CRS1}	“Start of Stream” to CSR Asserted		140		ns
t_{CRS2}	“End of Stream” to CSR De-Asserted		170		ns

Table 5. 100BaseT MII Receive Timing Parameters

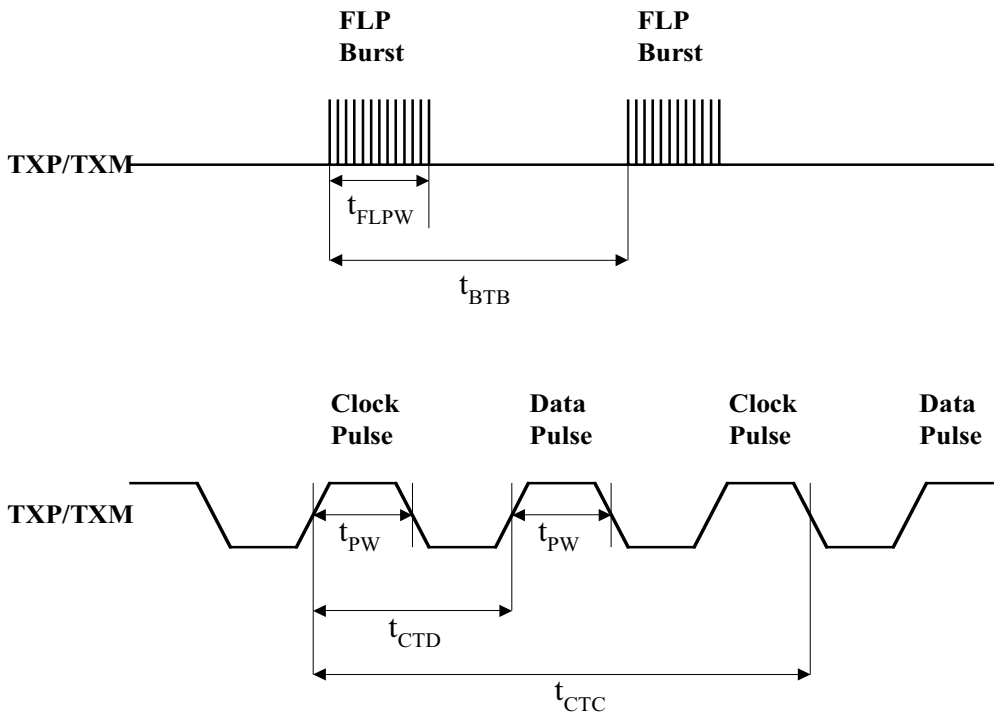


Figure 5. Auto Negotiation/Fast Link Pulse Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst Width		2		ms
t_{PW}	Clock/Data Pulse Width		100		ns
t_{CTD}	Clock Pulse to Data Pulse		69		µs
t_{CTC}	Clock Pulse to Clock Pulse Number of Clock/Data Pulses per Burst	 17	136	 33	µs µs

Table 6. Auto Negotiation/Fast Link Pulse Timing Parameters

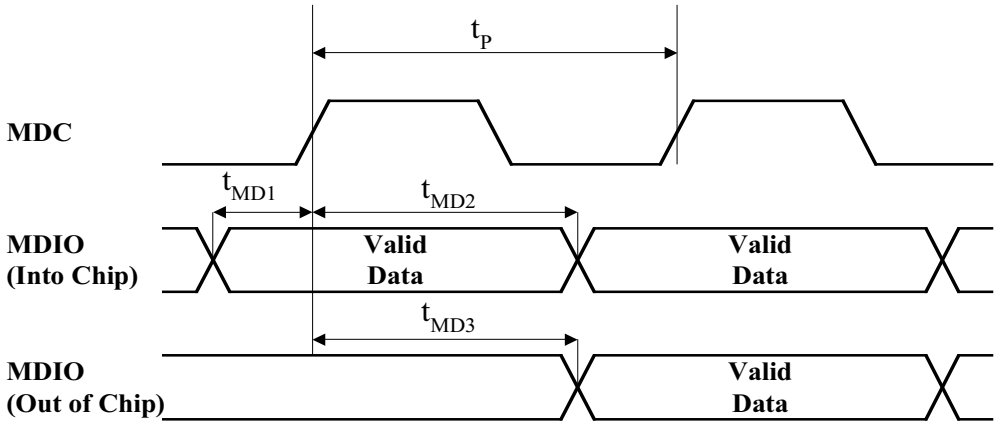


Figure 6. Serial Management Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t_P	MDC Period		400		ns
t_{MDI}	MDIO Set-Up to MDC (MDIO as Input)	10			ns
t_{MD2}	MDIO Hold After MDC (MDIO as Input)	10			ns
t_{MD3}	MDC to MDIO Valid (MDIO as Output)		250		ns

Table 7. Serial Management Interface Timing Parameters

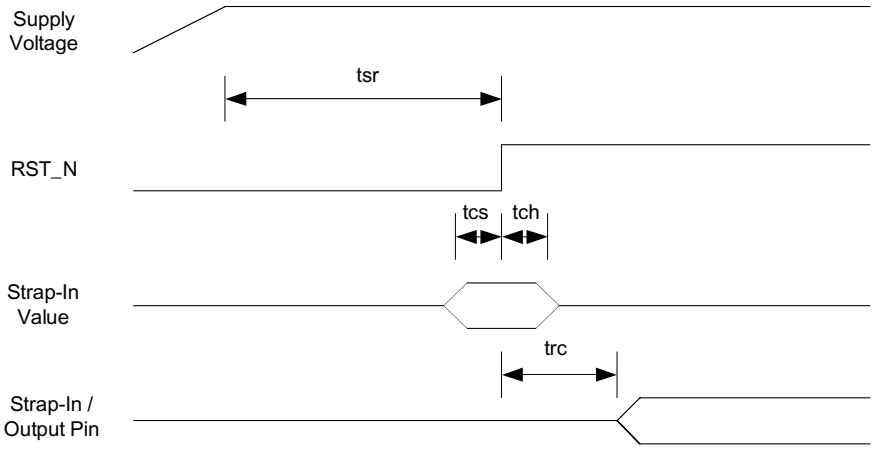


Figure 7. Reset Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{sr}	Stable Supply Voltages to Reset High	10			ms
t_{cs}	Configuration Set-Up Time	50			ns
t_{ch}	Configuration Hold Time	50			ns
t_{rc}	Reset to Strap-In Pin Output	50			µs

Table 8. Reset Timing Parameters

Selection of Isolation Transformer(Note 1)

One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

Characteristics Name	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (min.)	350µH	100mV, 100kHz, 8mA
Leakage Inductance (max.)	0.4µH	1MHz (min.)
Inter-Winding Capacitance (max.)	12pF	
D.C. Resistance (max.)	0.9Ω	
Insertion Loss (max.)	1.0dB	0MHz – 65MHz
HIPOT (min.)	1500Vrms	

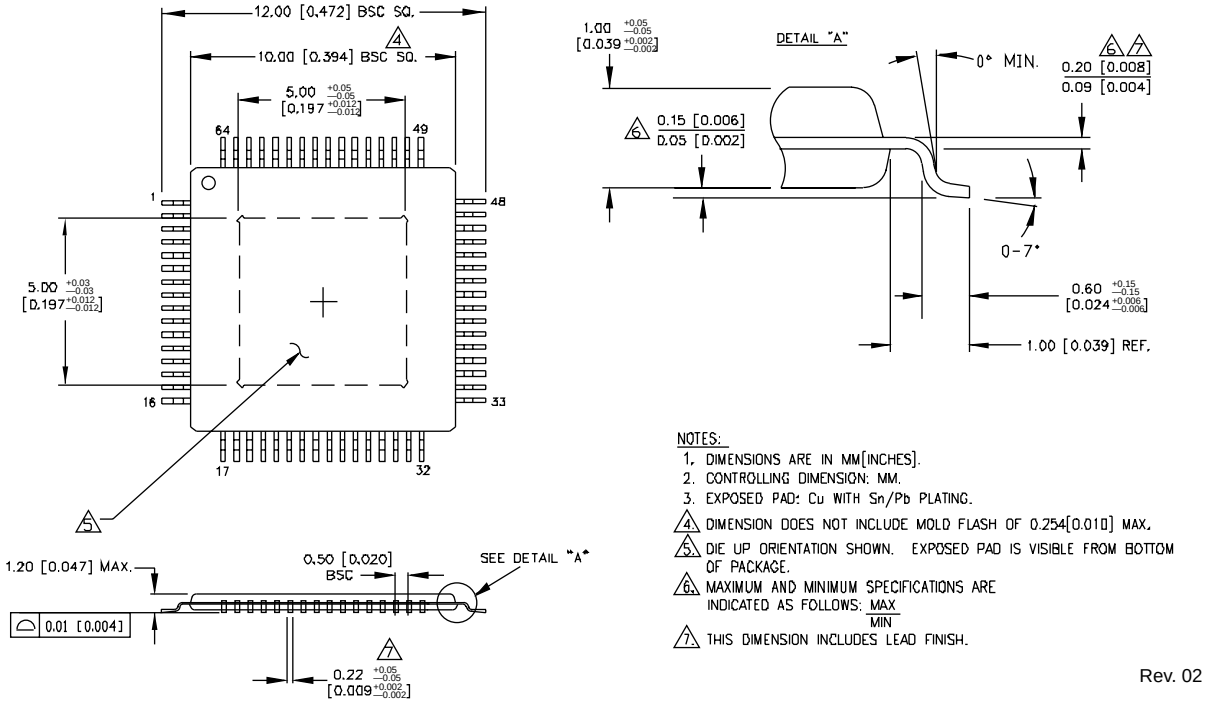
Note 1. The IEEE 802.3u standard for 100BaseTX assumes a transformer loss of 0.5 dB. For the transmit line transformer, insertion loss of up to 1.3dB can be compensated by increasing the line drive current by means of reducing the ISET resistor value.

Selection of Reference Crystal

An oscillator or crystal with the following typical characteristics is recommended.

Characteristics Name	Value	Units
Frequency	25.00000	MHz
Frequency Tolerance (max.)	±100	ppm
Load Capacitance (max.)	20	pF
Series Resistance (max.)	25	Ω

Package Information



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 02

64-Pin TQFP (TQ)

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