LTC4263
Main Board, Single Port Autonomous PSE/Daughter Card PSE

DESCRIPTION

Demonstration circuits 981A and 981B feature the LTC®4263 in single port Power over Ethernet (PoE) power sourcing equipment (PSE) midspan and endpoint solutions. The LTC4263 is an autonomous single-channel PSE controller for use in IEEE802.3af compliant PoE systems. It includes an onboard planar power MOSFET, internal inrush, current limit, and short-circuit control, powered device (PD) detection and classification circuitry, and selectable AC or DC disconnect sensing. Onboard control algorithms provide complete PSE control operation without the need of a microcontroller. The LTC4263 simplifies PSE implementation, needing only a single 48V supply and a small number of passive support components. Other options shown on the DC981A include legacy PD detection enable, midspan backoff timer enable, power class enforce mode, and power management enable. An LED for each port is driven by the respective LTC4263 to indicate the state of the port.

Design files for this circuit board are available at http://www.linear.com/demo/DC981A

PERFORMANCE SUMMARY

Table 1. Typical DC981, Specifications are at T_A = 25°C

PARAMETER	CONDITION	VALUE
Supply Voltage	Voltage for IEEE802.3af Compliance at Port Output	46V to 57V
Midspan Mode Detection Backoff	Midspan Enabled, Failed Detection	3.2s
Detection Range	Valid IEEE802.3af PD Detection	17kΩ to 29.7kΩ
Set Maximum Allocated Power	Power Management Enabled, RPM = 12.4kΩ	17W
Ethernet Powered Pairs Pinout	Endpoint PSE, Alternative A (MDI) Midspan PSE, Alternative B	1/2(+), 3/6(–) 4/5(+), 7/8 (–)

QUICK START PROCEDURE

Demonstration circuits 981A and 981B are easy to set up to evaluate the performance of the LTC4263. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

1. Place jumpers in the following positions:

JP1	EN
JP2	EN
JP3	DIS
JP4	AC
JP5	AC
JP6	EN

2. Insert daughter card (DC981B) to main board (DC981A) at polarized connector J3.
3. Apply 48V across VDD48 and VSS.
4. Connect a scope probe at VOUT_MD and VOUT_EP both referenced to positive rail VDD48.
5. Connect a valid PD to either midspan PSE or endpoint PSE.
6. Connect a second PD to the open port.

OPERATING PRINCIPLES

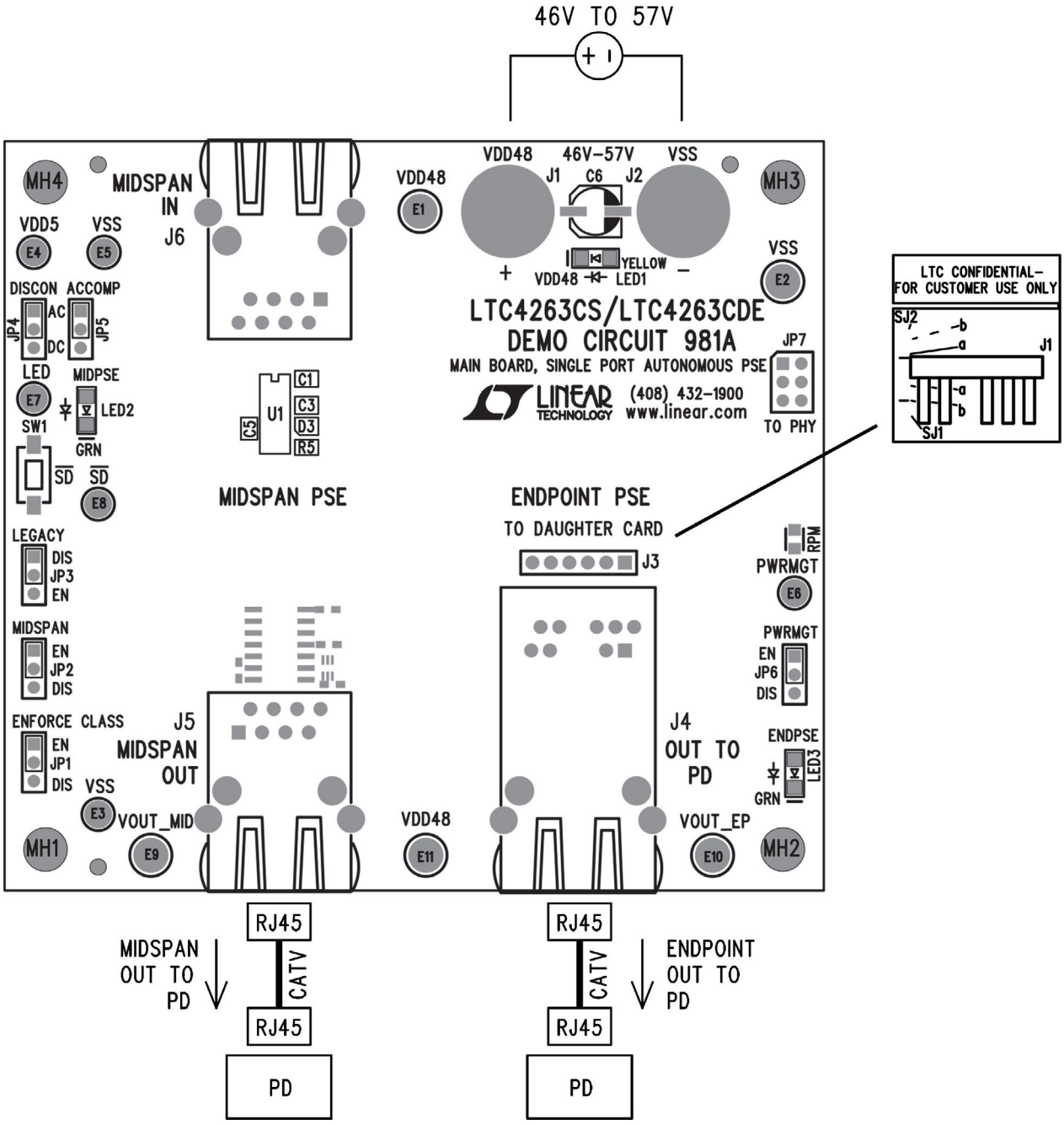


Figure 1. Basic DC981A/DC981B Equipment Setup

OPERATING PRINCIPLES

The DC981 provides two implementations of a PSE controlled by the LTC4263, a midspan PSE and an endpoint PSE. A single 48V supply is all that is required to power the board. This in turn provides power to the midspan PSE and endpoint PSE outputs. On each solution, an LTC4263 provides detection, classification, power management, safe power on, port current limit, and disconnect detection.

Midspan PSE

In the midspan solution, a legacy device (router, switch, etc.) that does not have PoE is connected to MIDSPAN IN. Data is passed through to MIDSPAN OUT along with PoE which goes out to a PD. Power is applied directly to Ethernet pairs 4/5 and 7/8. The LTC4263 circuitry is located in a small layout area behind the RJ45 connector and switches power on the negative rail. To show the different functions of the LTC4263, jumpers allow for the user to select the options of AC or DC disconnect, legacy detection, midspan backoff timing, and class enforcement. An LED that shows the status of the port is driven by a switcher in the LTC4263 to improve efficiency when VDD5 is provided internally. Push button switch SW1 ties the shutdown pin to ground to disable the LTC4263 in the midspan solution.

A PSE implementing alternative B pin out must back off from detection for at least two seconds after a failed attempt. This is to avoid conflict of detection, for example, should a potential endpoint PSE and midspan PSE be connected to the same PD. To enable this feature, set JP2 to DIS. JP2 ties the MIDSPAN pin to VDD5 to enable the LTC4263 backoff timer or to VSS to disable. A 3.2s delay occurs after every failed detect cycle unless the result is open circuit. If held at VSS, no delay occurs after failed detect cycles.

Endpoint PSE

The endpoint solution is primarily shown on a small daughter card (DC981B). This card is the same height and width as the integrated RJ45 connector that it slides behind on the main board (DC981A). The RJ45 includes Ethernet magnetics and common mode termination. A layout option shows the same components can be placed under the same RJ45 connector. The minimum connections to the daughter card are VSS, VDD48 and VOUT. Power is switched over from the daughter card out to the Ethernet data pairs (1/2 and 3/6). A PHY can be connected to the *TO PHY* connector to pass data through to the data pairs along with PoE. LED drive and power management pins are also brought out for additional board functions. The board is set up for AC disconnect, but can be reworked for DC disconnect by removing components and replacing with shorts in certain locations. Two solder jumpers also provide selectable options for legacy detection and class enforce.

Power Management

The midspan and endpoint PSEs, although separate solutions on the DC981, are tied together at the PWRMGT pin for demonstration of the LTC4263 power management capability. Programmable onboard power management circuitry allows multiple LTC4263s to allocate and share power in multiport systems, allowing maximum utilization of the 48V power supply – all without the intervention of a host processor.

The LTC4263 sources current (IPM) at the PWRMGT pin proportional to the class of the PD that it is powering. The voltage of this pin (VPM) is checked before powering the port (Table 2). The port will not turn on if this pin is more than 1V above VSS. The PWRMGT pins of the LTC4263s are tied together and connect to a resistor (RPM) and capacitor (CPM) in parallel to VSS to implement power management. This resistor is selected with the following equation:

$$R_{PM} = 213k\Omega \bullet W/P_{FULL\_LOAD}$$

On the DC981A, the default RPM is 12.4kΩ for a full load power of 17W.

Table 2. Power Management Voltage

PD CLASS	POWER REQUEST	IPM (TYP)	VPM*
Class 1	4W	19µA	236mV
Class 2	7W	33µA	409mV
Class 0, 3, or 4	15.4W	73µA	905mV

*RPM = 12.4kΩ

OPERATING PRINCIPLES

Table 3. Powered Device Combinations

PD COMBINATION	1ST PD	2ND PD
Class 1 / Class 1	Powered	Powered
Class 1 / Class 2	Powered	Powered
Class 1 / Class 3**	Powered	Power Denied
Class 2 / Class 2	Powered	Powered
Class 2 / Class 3**	Powered	Power Denied
Class 3 **/ Class 3**	Powered	Power Denied

**Class 3 substitutable with Class 0 or 4.

If power management is not used, move JP6 to DIS to tie the PWRMGT pins to VSS and disable this feature.

Class Enforce Mode

ENFORCE CLASS jumper JP1 ties the ENFCLS pin of the LTC4263 to either VDD5 or VSS to respectively enable or disable class enforce current limits. If held at VDD5, the LTC4263 will reduce the ICUT threshold for Class 1 or Class 2 PDs. If ENFCLS is held at VSS, ICUT remains at 375mA (typical) for all classes.

Table 4. Port Current Limit According to Class

PD CLASS	CURRENT THRESHOLD (TYPICAL)
Class 1	100mA
Class 2	175mA
Class 0, 3, 4, or Class Enforce Disabled	375mA

LED Drive

An LED pin indicates the state of the port controlled by the LTC4263. When the port is powered, the LED is on; when disconnected or detecting, the LED is off. If an invalid signature is detected or a fault occurs, the LED will flash a pattern that the user or host system can read to indicate the nature of the problem. When run from a single 48V supply, the LED pin can operate as a simple switching current source to reduce power dissipation in the LED drive circuitry.

VDD5 Option

The logic 5V power supply can be supplied from the internal LTC4263 5V supply or an external 5V supply when above the internal supply. If the internal regulator is used, this pin should only be connected to the bypass capacitor and to logic pins of the LTC4263 held at VDD5.

AC and DC Disconnect

AC and DC disconnect are two different methods of detecting whether a valid PD is present and requires power. AC disconnect is the default method for the DC981 but can be converted to DC disconnect in the midspan solution through two jumpers. Moving DISCON (JP4) to DC will short the ACCOUT pin to VSS and configure the LTC4263 to DC disconnect. Moving jumper setting for ACCOMP (JP5) to DC bypasses the AC blocking diode and removes the RC used for AC disconnect from the main circuit.

Legacy Detection

LEGACY jumper JP3 controls whether legacy detect is enabled. If the LEGACY pin is held at VDD5 (EN selected), legacy detect is enabled and testing for a large capacitor is performed to detect the presence of a legacy PD on the port. If held at VSS (DIS selected), only IEEE 802.3af compliant PDs are detected. If left floating (no jumper), the LTC4263 enters force-power-on mode and any PD that generates between 1V and 10V when biased with 270µA of detection current will be powered as a legacy device. This mode is useful if the system uses a differential detection scheme to detect legacy devices. Warning: Legacy modes are not IEEE 802.3af compliant.

OPERATING PRINCIPLES

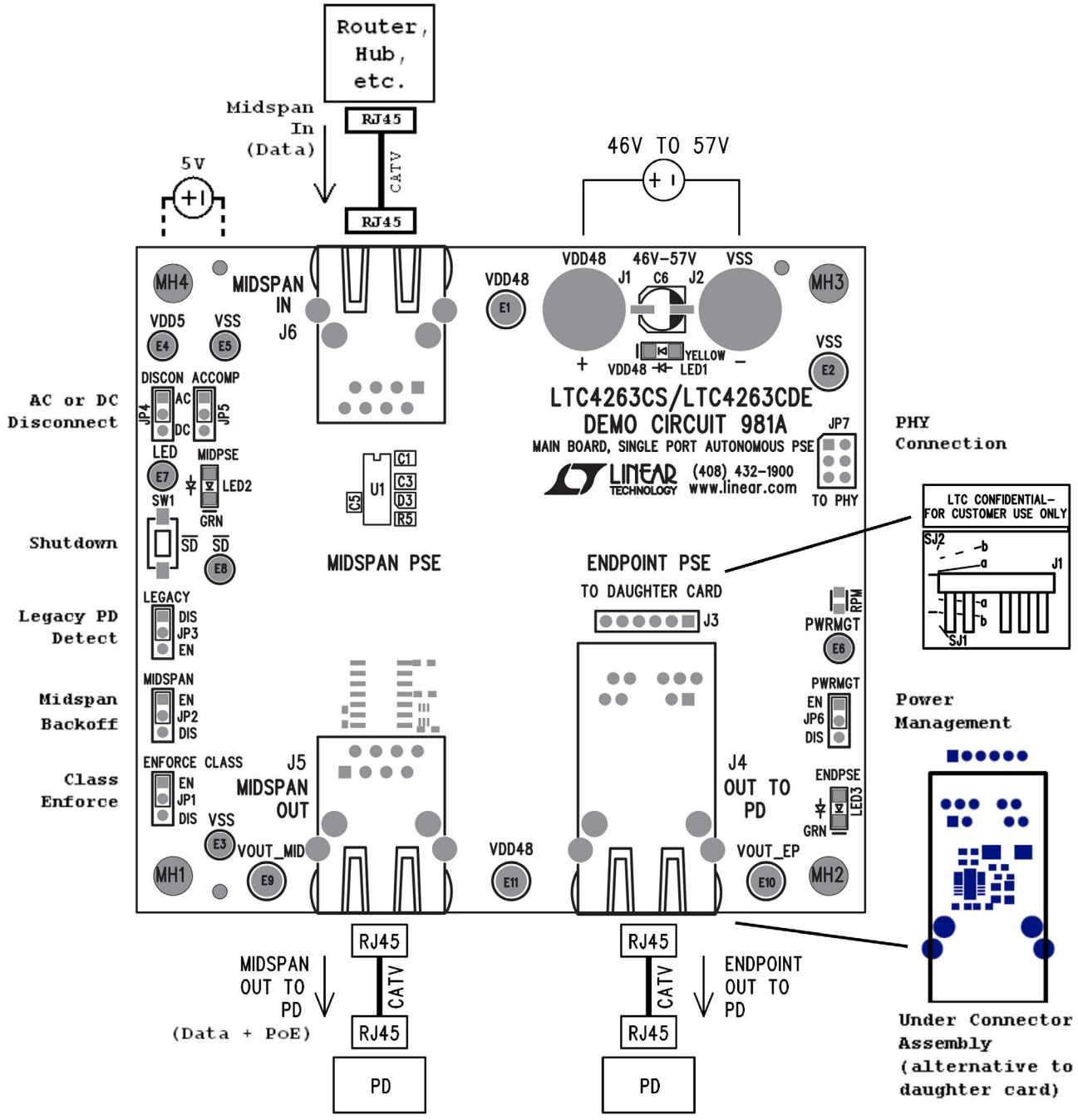
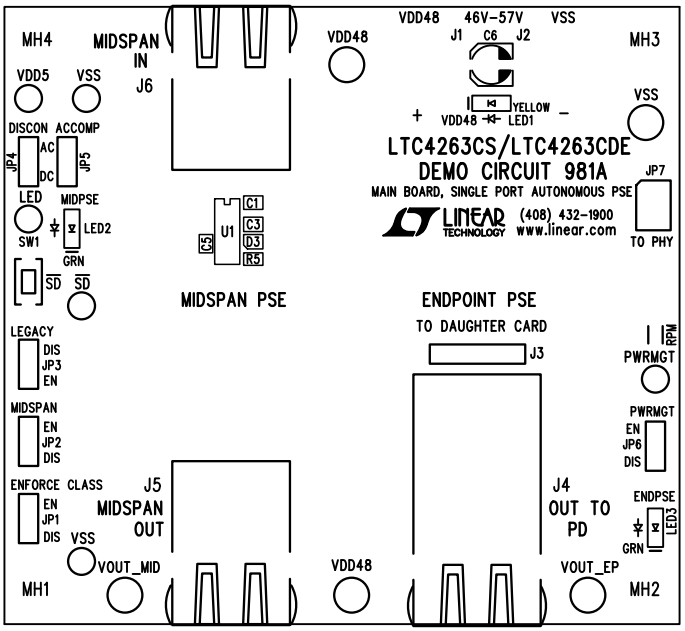


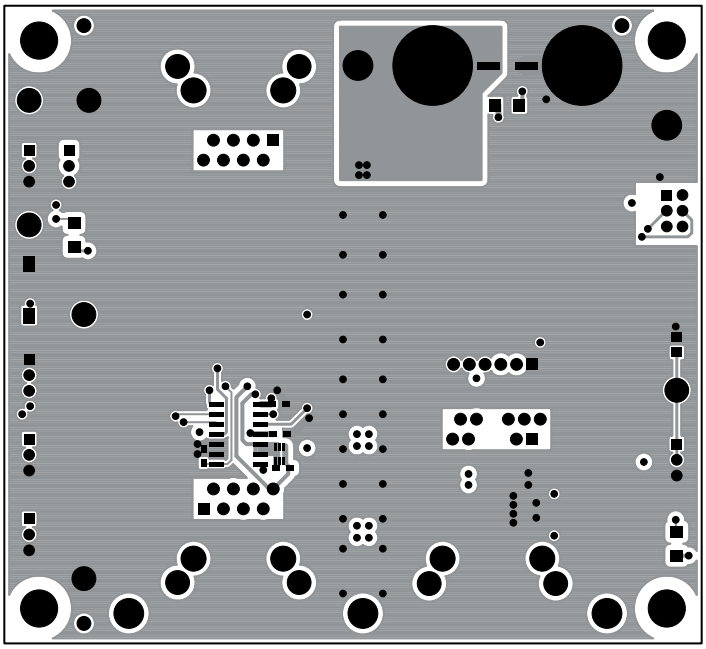
Figure 2. DC981 Options

DC981A LAYOUT

Top Silkscreen

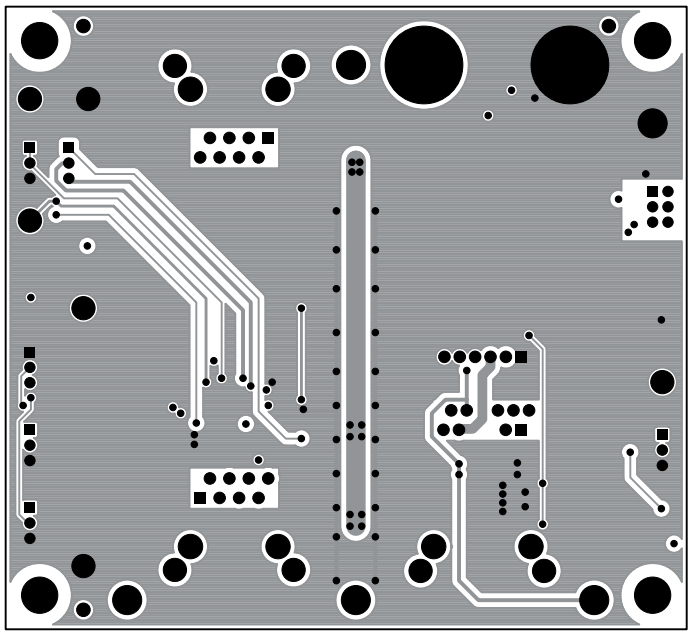


Layer 1



DC981A LAYOUT

Layer 2



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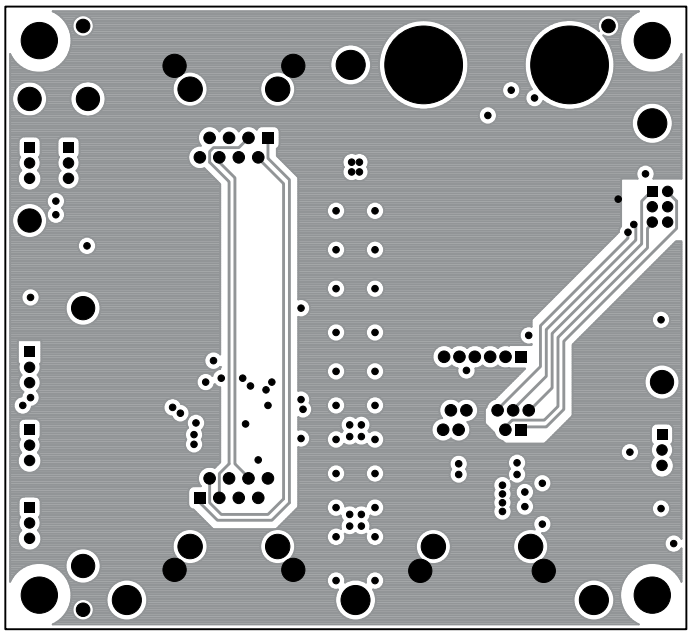
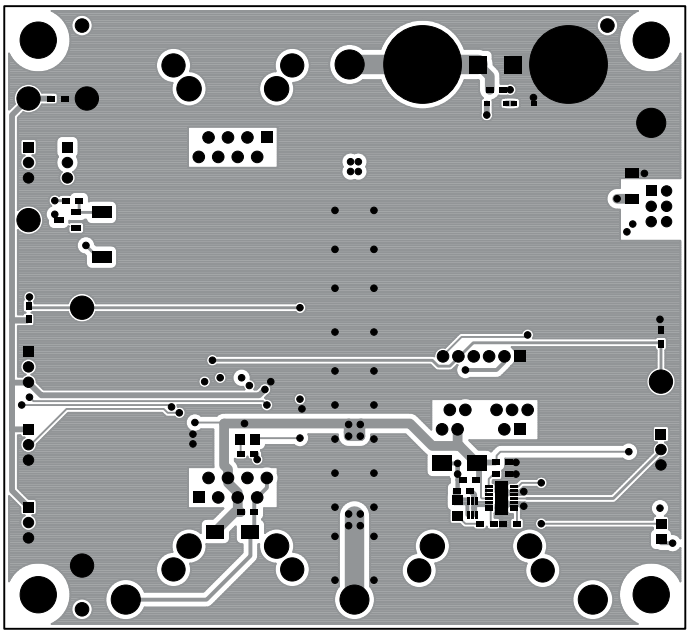
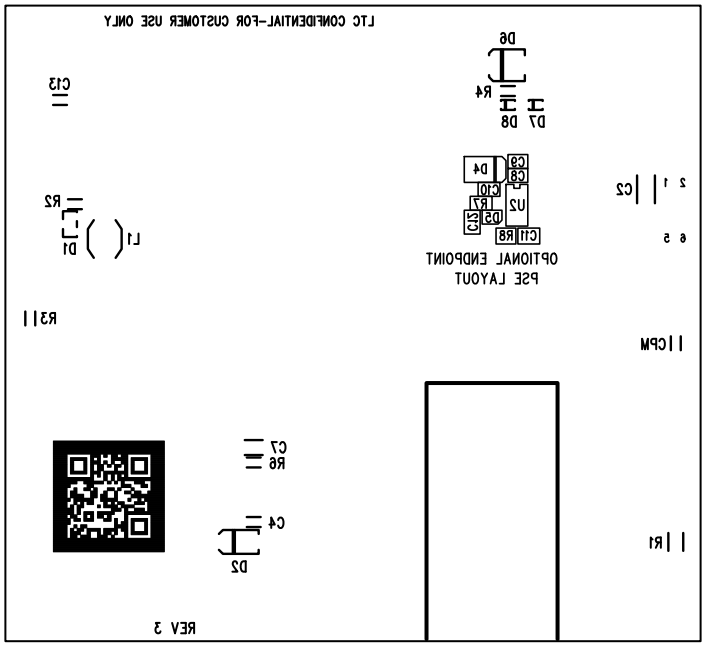


DC981A LAYOUT

Layer 4

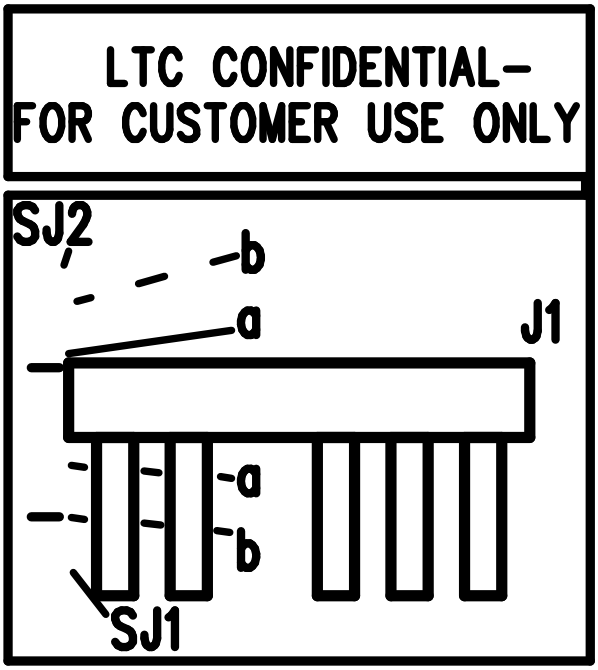


Silkscreen Bottom



DC981B LAYOUT

Top Silkscreen



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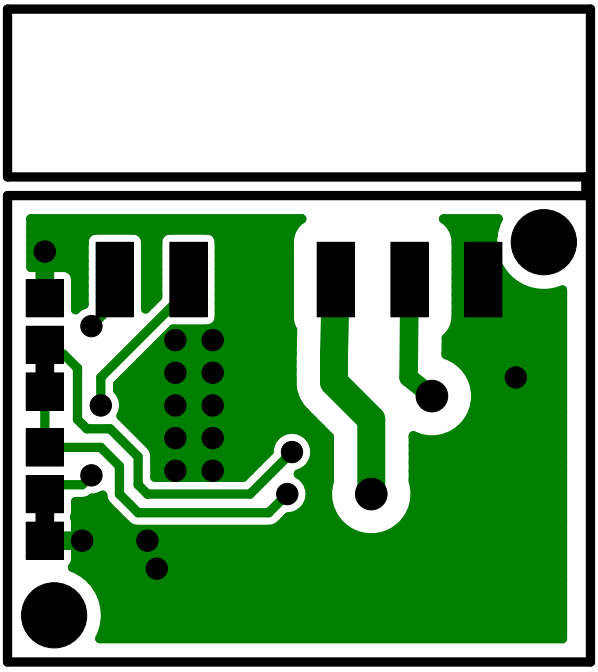
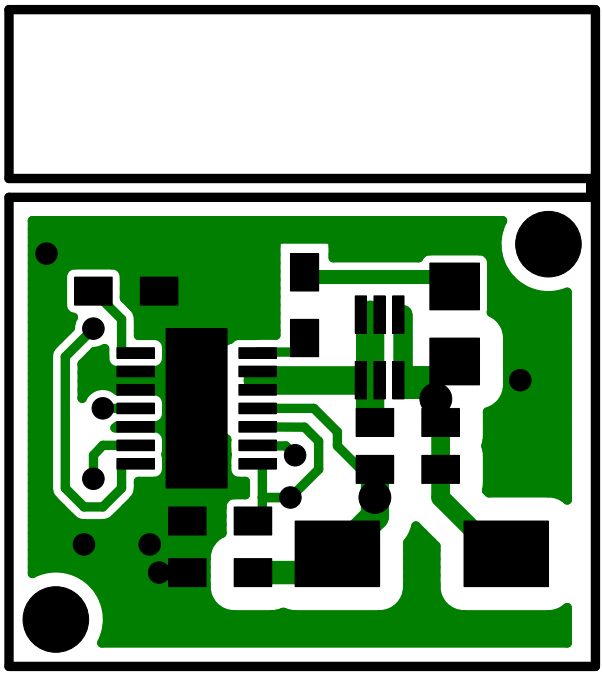
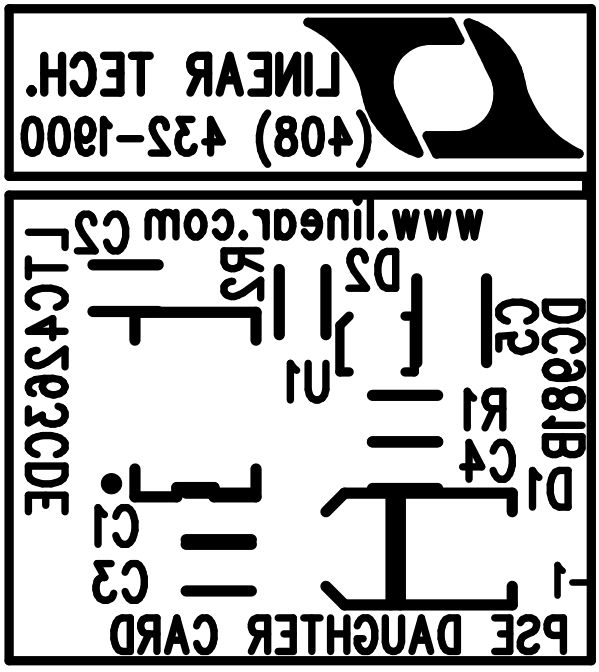


DC981B LAYOUT

Bottom Layer



Bottom Silkscreen



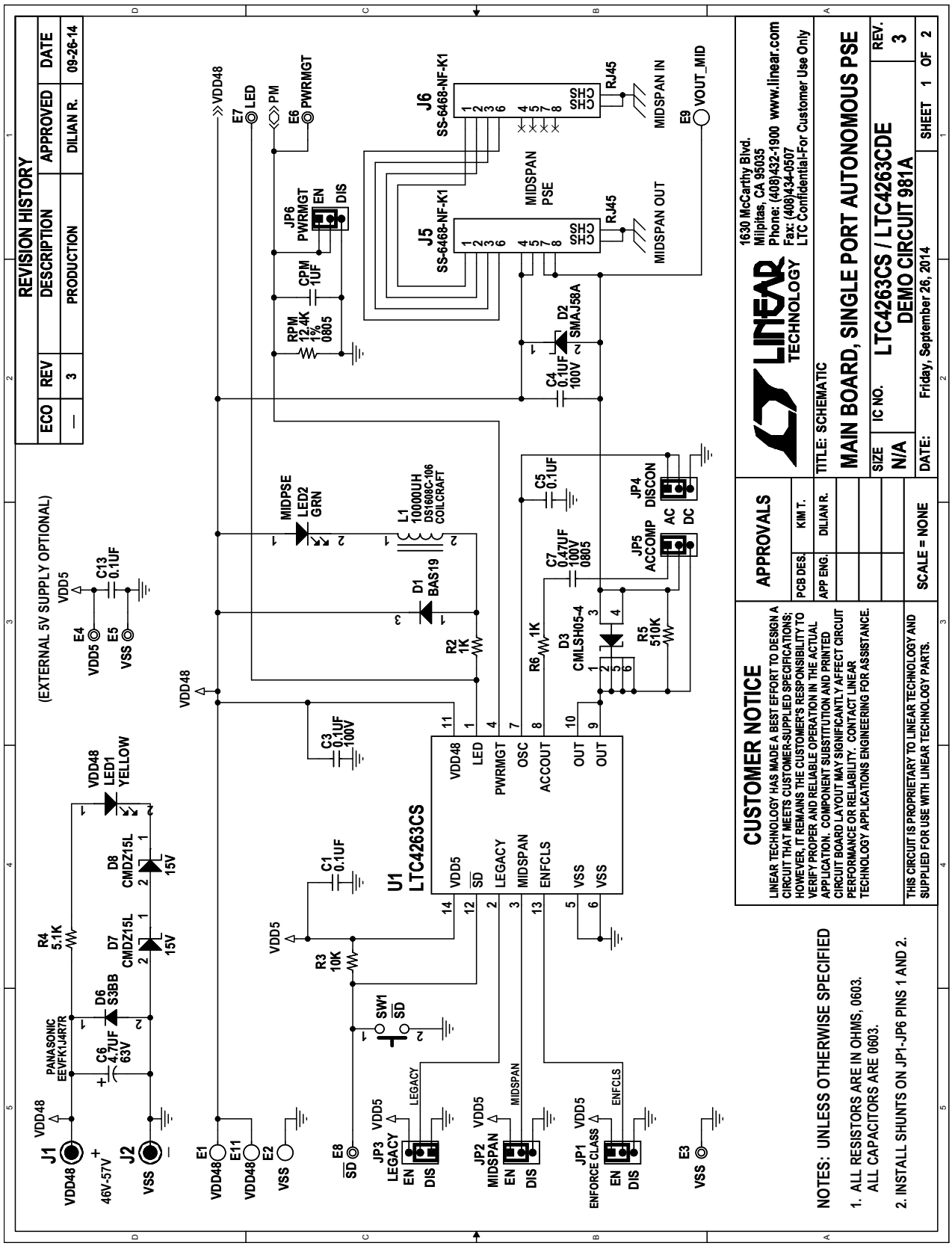
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC981A-3 Required Circuit Components				
1	1	CPM	CAP, X5R, 1µF 16V, 10%, 0603	MURATA, GRM185R61C105KE44D
2	2	C1	CAP, X7R, 0.1µF 16V, 10%, 0603	MURATA, GRM188R71C104KA01D
3	2	C3, C4	CAP, X7R 0.1µF 100V, 10%, 0603	MURATA, GRM188R72A104KA35D
4	1	D1	DIODE, SWITCHING, SOT23	DIODES INC, BAS19-7-F
5	1	D2	DIODE, 58V TVS, SMA-DIODE	DIODES INC, SMAJ58A-13
6	1	J4	JACK, POWER, RJ45-JK0-0144BNL	PULSE, JK0-0144BNL
7	2	LED3, LED2	LED, GREEN, LED-ROHM, SML-010	ROHM, SML-010FTT86
8	1	L1	IND, PWR, 10000µH, L-COIL-DS1608C	COILCRAFT, DS1608C-106MLC
9	1	RPM	RES, CHIP 12.4k 1/16W 1%, 0805	VISHAY, CRCW080512K4FKEA
10	1	R1	RES, CHIP 2k 1/10W 5%, 0805	VISHAY, CRCW08052K00FKEA
11	1	R2	RES, CHIP 1k 1/16W 5%, 0603	YAGEO, RC0603FR-071KL
12	1	R3	RES, CHIP 10k 1/16W 5%, 0603	YAGEO, RC0603FR-0710KL
13	1	U1	IC, LTC4263CS, SO14	LINEAR TECHNOLOGY, LTC4263CS
Optional Circuit Components				
1	1	C2	CAP, X7R 1000PF 2kV, 1206	MURATA, GR431BR7LA102KW01L
2	4	C5, C8, C11, C13	CAP, X7R, 0.1µF 16V, 10%, 0603	MURATA, GRM188R71C104KA01D
3	1	C6	CAP, ELECT, 4.7µF 63V, C-PANA-EEVFK-C	PANASONIC, EEE-FK1J4R7R
4	2	C7, C12	CAP, X7R, 0.47µF 100V, 10%, 0805	MURATA, GRM21BR72A474KA73L
5	2	C9, C10	CAP, X7R 0.1µF 100V, 10%, 0603	MURATA, GRM188R72A104KA35D
6	2	D3, D5	DIODE, SHOTTKY, PICO MINI, SOT563	CENTRAL SEMI, CMLSH05-4
7	1	D4	DIODE, 58V TVS, SMA-DIODE	DIODES INC, SMAJ58A-13
8	1	D6	DIODE, RECTIFIER 3A, SMB-DIDOE	DIODES INC, S3BB-13-F
9	2	D8, D7	DIODE, 15V, ZENER, SOD323	CENTRAL SEMI, CMDZ15L
10	2	J6, J5	CONN, RJ-45 RIGHT ANGLE, RJ45	STEWART CONN SYS, SS-6488-NF-K1
11	1	LED1	LED, YELLOW, LED-ROHM, SML-010	ROHM, SML-010YTT86
12	2	R6, R8	RES, CHIP 1k 1/16W 5%, 0603	YAGEO, RC0603FR-071KL
13	1	R4	RES, CHIP 5.1k 1/16W 5%, 0603	AAC, CR16-512JM
14	2	R5, R7	RES, CHIP 510k 1/16W 5%, 0603	VISHAY, CRCW0603510KJNEA
15	1	SW1	SWITCH, PUSH BUTTON	WÜRTH, 434 123 050 816
16	1	J3	SOCKET, 1X6, 0.079", VERTICAL	SAMTEC, SQT-106-01-LM-S-004
17	1	U2	IC, LTC4263CDE, DFN14DE	LINEAR TECHNOLOGY, LTC4263CS
Hardware for Demo Board Only				
1	5	E1, E2, E9, E10, E11	TP, TURRET, 0.094"	MILL-MAX, 2501-2-00-80-00-00-07-0
2	6	E3, E4, E5, E6, E7, E8	TP, TURRET, 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
3	6	JP1, JP2, JP3, JP4, JP5, JP6	JMP, 1X3, 0.079"	SAMTEC, TMM-103-02-L-S
4	0	JP7	JMP, 2X3, 0.079"	OPT
5	6	FOR JP1 TO JP6 (1 and 2)	SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G
6	2	J1, J2	JACK, BANANA, KEY-575	KEYSTONE, 575-4
7	4	MH1 TO MH4	STANDOFF, SNAP ON, 1/2"	KEYSTONE, 8833

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC981B Required Circuit Components				
1	2	C2, C1	CAP, X7R, 0.1µF 16V, 10%, 0603	MURATA, GRM188R71C104KA01D
2	2	C3, C4	CAP, X7R 0.1µF 100V, 10%, 0603	MURATA, GRM188R72A104KA35D
3	1	C5	CAP, X7R, 0.47µF 100V, 10%, 0805	MURATA, GRM21BR72A474KA73L
4	1	D1	DIODE, 58V TVS, SMA-DIODE	DIODES INC, SMAJ58A
5	1	D2	DIODE, SCHOTTKY, PICO MINI, SOT563	CENTRAL SEMI, CMLSH05-4
6	1	J1	HEADER, 1X6, 0.079", SMT, HORIZONTAL	SAMTEC, MMT-106-02-S-SH-004
7	1	R1	RES, CHIP 510kΩ 1/16W 5%, 0603	AAC, CR16-514JM
8	1	R2	RES, CHIP 1kΩ 1/16W 5%, 0603	AAC, CR16-102JM
9	1	U1	I.C., LTC4263CDE, DFN14DE	LINEAR TECHNOLOGY, LTC4263CDE

SCHEMATIC DIAGRAM



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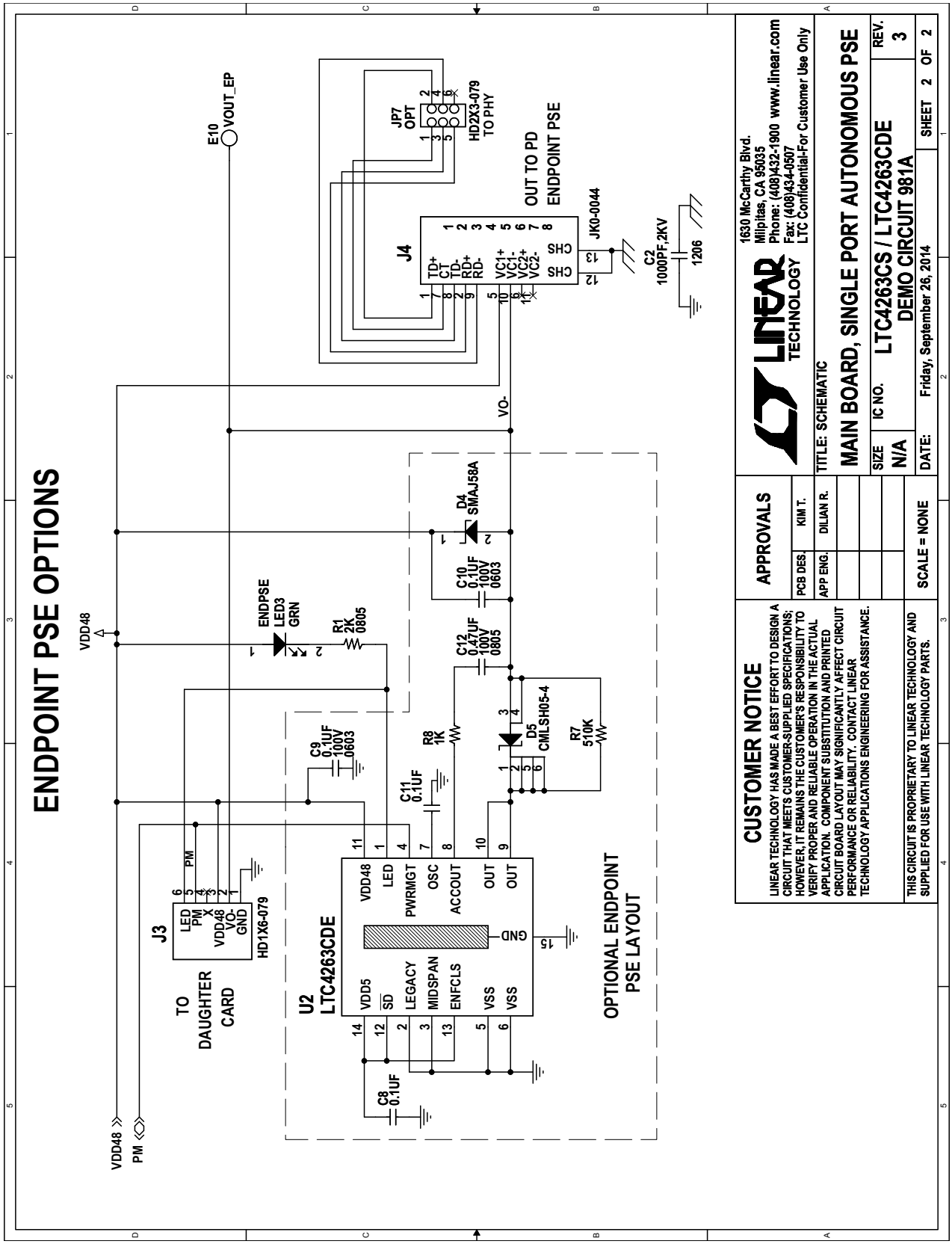
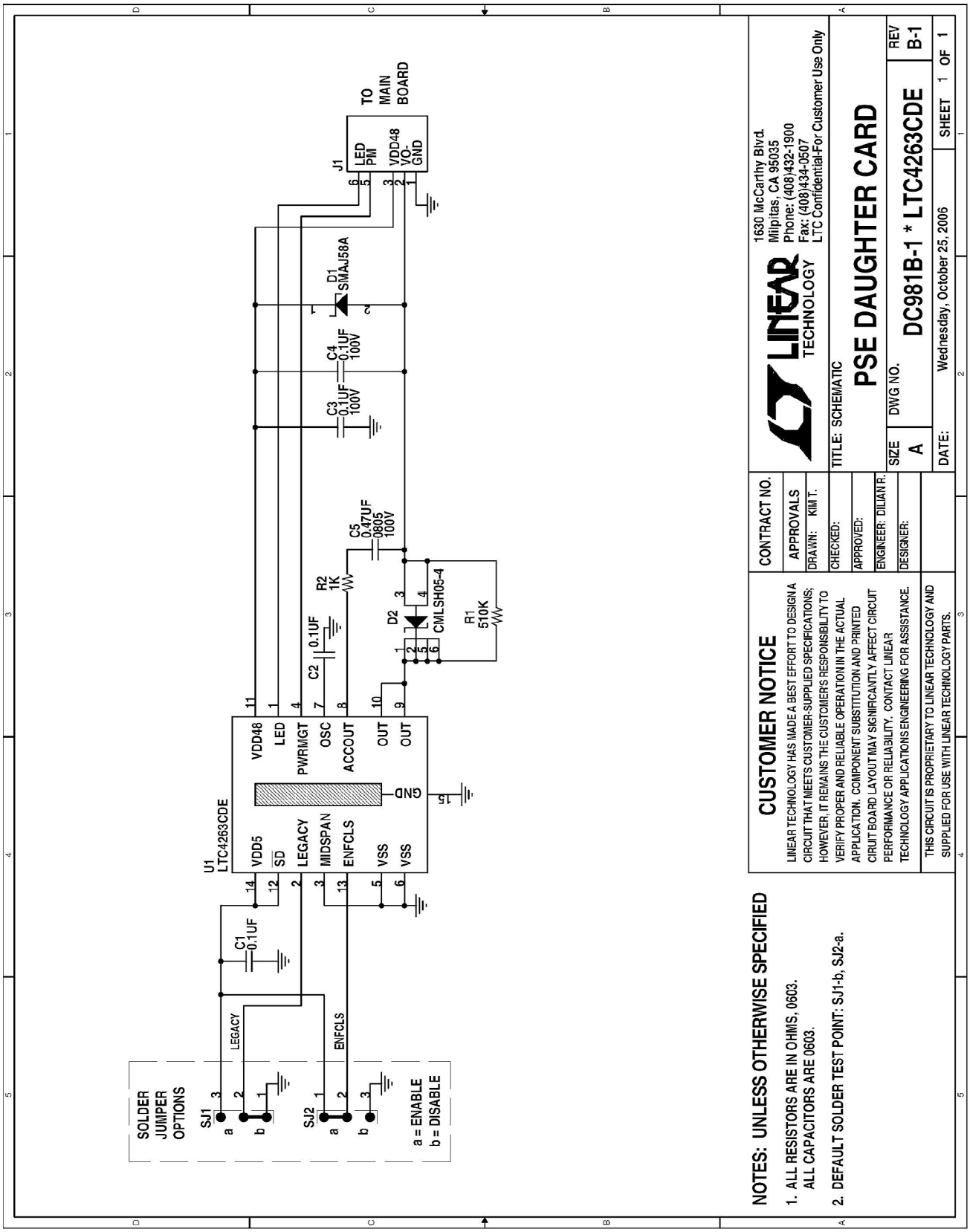
SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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