AN2840
Application note

EVLVIP17-5WCHG: 5 W low standby consumption battery charger demonstration board based on the VIPER17HN

Introduction

The EVLVIP17-5WCHG demonstration board is a 5 W SMPS for use as a travel battery charger for applications such as mobile phones, PDAs and electronic games. The purpose of the board is to demonstrate the performance of the VIPER17HN off-line high voltage converter. Thanks to its low consumption and other features, good electrical performance is achieved. To obtain constant output voltage and current regulation (CV/CC), the TSM1052 CV/CC controller is used on the secondary side. This TSM1052 is well-suited for this type of application, offering very low current consumption in a very small package (SOT23-6L). Another important feature of the SMPS is the elimination of the Y1 safety capacitor between the primary and the secondary side.

Figure 1. EVLVIP17-5WCHG demonstration board (top side)

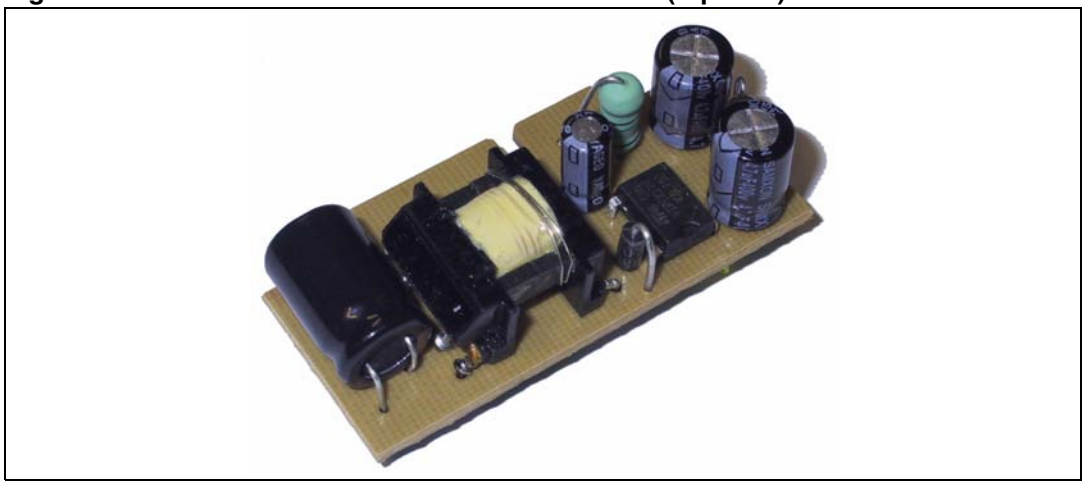
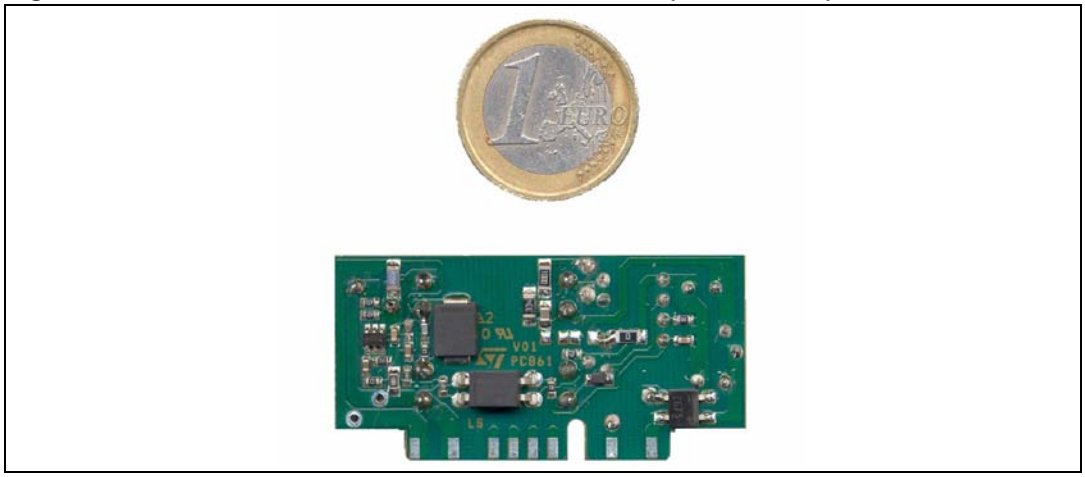


Figure 2. EVLVIP17-5WCHG demonstration board (bottom side)



Contents

1 Main characteristics and circuit description

The following is a list of the main characteristics of the EVLVIP17-5WCHG:

- Input mains range: 90 - 264 V_{RMS}, f: 45 - 66 Hz
- Output parameters: 5.1 V_{DC} ± 2%, 1 A ± 5%, cable drop compensation (0.2 V/A)
- No-load consumption: input power below 100 mW at high mains
- Short-circuit protected with auto-restart at short removal
- PCB type and size: CEM-1, single side 35 µm, 53 x 26 mm
- Safety: EN60065 compliant
- EMI: conforms to EN55022 - class B standards

The converter implements a flyback topology, which is ideal for low power, low cost isolated converters.

On the primary side, the VIPER17HN is used. This IC is a member of the VIPer+ family, and benefits from its additional features and protections.

This device, designed using a multi-chip approach, includes an advanced current mode PWM controller and an avalanche-rugged 800 V power MOSFET in a small DIP-7 package. The converter works in both continuous and discontinuous conduction mode depending on the input voltage (the circuit has a wide range input) and output load. The controller suffix “H” specifies that the switching frequency is 115 kHz, internally fixed, allowing the reduction of the power components. The application is designed to reduce overall component count and adapter cost.

The input section includes a fuse resistor for inrush current limiting and fault protection, a rectifier bridge, two electrolytic bulk capacitors and an inductor as front-end ac-dc converter and EMC filter. The transformer is a layer type, utilizing a standard EF12.6 ferrite core and is designed with approximately 75 V reflected voltage. The peculiarity of this transformer is the winding technique that eliminates the needs for the commonly-used Y1 safety capacitor between the primary and the secondary side. An RCD clamp network is used for leakage inductance demagnetization.

The startup of the circuit is managed by the internal high voltage startup generator of the VIPER17HN. This circuit sinks a typical current of 3 mA from the drain pin and charges the VDD capacitor. This current value is reduced to 0.6 mA when there is a protection intervention, in order to increase restart trial period and thus to reduce the stress on the power components in case of permanent fault. The power supply for the VIPER17HN is obtained by a self-supply winding from the transformer connected in a flyback configuration. This circuit provides a voltage that is, ideally, directly proportional to the output voltage. In practice, since this particular no Y-cap transformer has a high leakage inductance, the self-supply voltage increases as the peak primary current increases. In any case, thanks to the wide V_{DD} voltage range of the VIPER17HN (from 8.5 V to 23 V) the correct supply is always provided. The internal MOSFET current limit is decreased (from the nominal value of 0.4 A) by using resistor R16 connected to the CONT pin. With this function, the I_{Dlim} is fixed at about 280 mA, allowing the use of a small-sized transformer (EF12.6 for 5 W output) without risk of saturation.

The brownout voltage divider is not mounted (so this feature is disabled) to save power, especially for the no-load consumption.

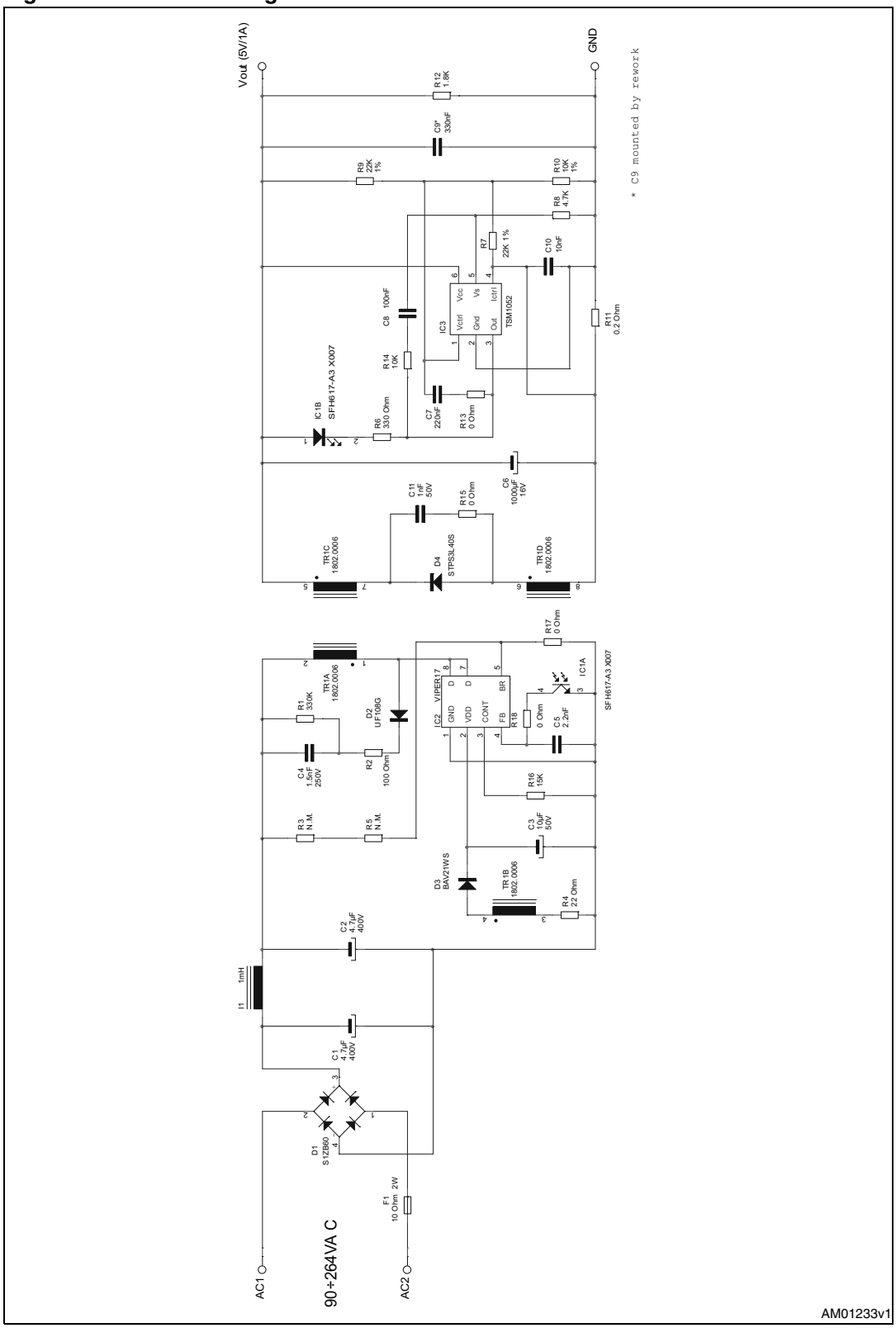
The VIPER17HN has several built-in features, such as a frequency jittering to reduce EMI problems, soft-start, and burst-mode operation for low power consumption during light load and no-load conditions. Over-current, overload and over-temperature protections are also implemented internally and guarantee safe operation of the board.

On the secondary side, the TSM1052 constant voltage constant current (CV/CC) controller is used. The TSM1052 and the photodiode of the optocoupler are supplied directly from the output voltage. The wide supply voltage range of the TSM1052 (1.7 V min) allows accurate constant current regulation even with output voltages down to 1.5 V-1.6 V. This range is usually enough for all battery charger applications. When the output voltage falls below this limit the circuit loses regulation, the OLP protection is invoked and the system starts working in HICCUP mode.

If, for some reason, current regulation is required down to the zero output voltage level (i.e. short-circuit), it is enough to supply the TSM1052 and the photodiode with a voltage equal to the sum of the output voltage and the voltage from TR1C winding rectified in a forward way. For more details on this specific schematic, please see application note AN2448 (Ultra small battery charger using TSM1052).

The R7 resistor is added to provide the cable drop compensation. The higher the output current, the higher the output voltage measured on the output terminals of the PCB. In this way, the voltage drop on the cable that connects the unit to the load is compensated and the voltage supplied to the load is essentially constant. More in detail, since R7 equals R9, the output voltage increase is 0.2 mV per mA of output current. This amount is chosen based on the typical cable resistance for these applications (typically around 0.2-0.3 Ω).

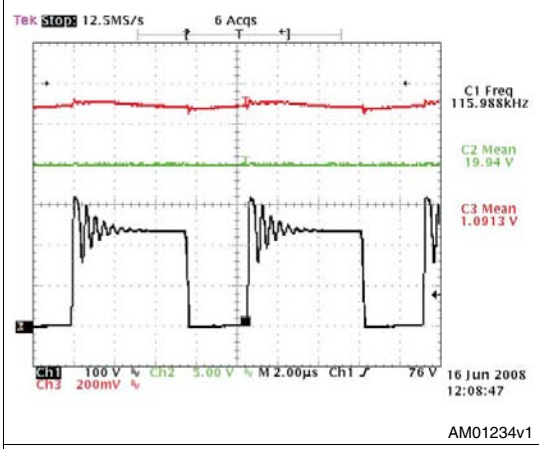
Figure 3. Electrical diagram



2 Operating waveforms

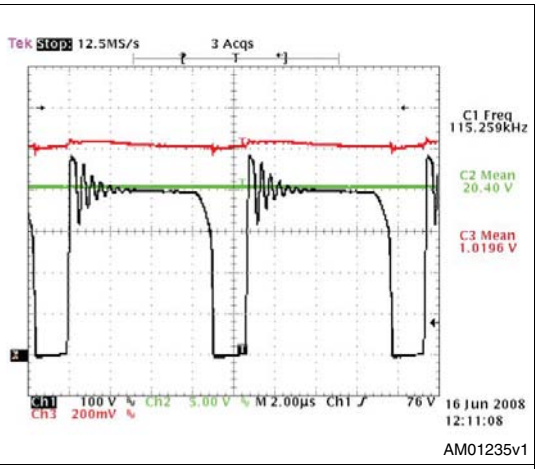
Figure 4 and *Figure 5* show some VIPER17HN waveforms during normal operation at full load (5 W). Note that at low mains (115 V_{RMS}) the converter operates in continuous conduction mode, while at 230 V_{RMS} it works in discontinuous conduction mode. This converter design takes advantage of both operating modes. In the illustrations below, the VDD voltage powering the device and the feedback pin voltage are also shown.

Figure 4. V_{IN} = 115 V_{AC} – 60 Hz, full load, normal operation



CH1: VIPER17HN drain pin (black trace)
CH2: VIPER17HN VDD pin (green trace)
CH3: VIPER17HN FB pin (red trace)

Figure 5. V_{IN} = 230 V_{AC} - 50 Hz, full load, normal operation

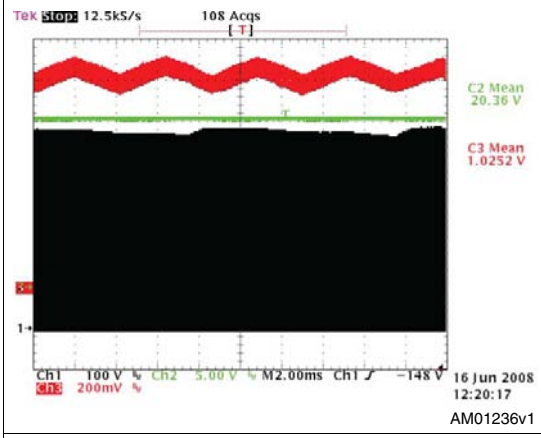


CH1: VIPER17HN drain pin (black trace)
CH2: VIPER17HN VDD pin (green trace)
CH3: VIPER17HN FB pin (red trace)

In *Figure 6* it is worth noting that once the circuit is working in DCM, the voltage on the FB pin has a triangular shape due to frequency jittering. The loop must adjust the FB pin voltage according to the actual switching frequency to keep the output voltage regulated. This happens because the transferred power in DCM is directly proportional to the switching frequency. Hence, the low frequency sawtooth superimposed on the FB pin has the same frequency as the modulating frequency (250 Hz typ.).

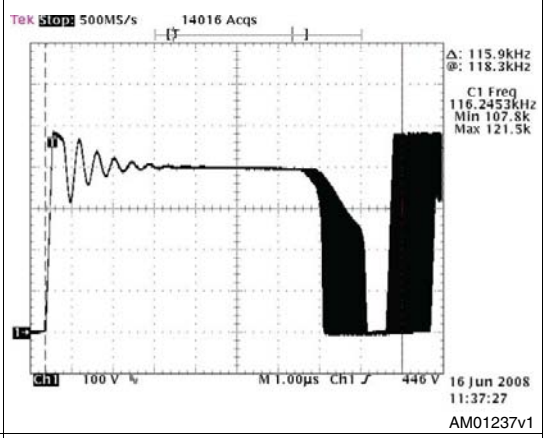
On the drain waveform in *Figure 7*, the modulation depth of the jittering function is visible. The waveform is captured while synchronizing the scope on the rising edge and using the Envelope acquisition. Thus the trailing edge of the following switching cycle shows frequency variation that is identical to the oscillator frequency with a variation depending on the jittering of the oscillator, in this case 115 kHz and +/- 8 kHz of modulation.

Figure 6. V_{IN} = 230 V_{AC} - 50 Hz, full load, FB pin behavior



CH1: VIPER17HN drain pin (black trace)
CH2: VIPER17HN VDD pin (green trace)
CH3: VIPER17HN FB pin (red trace)

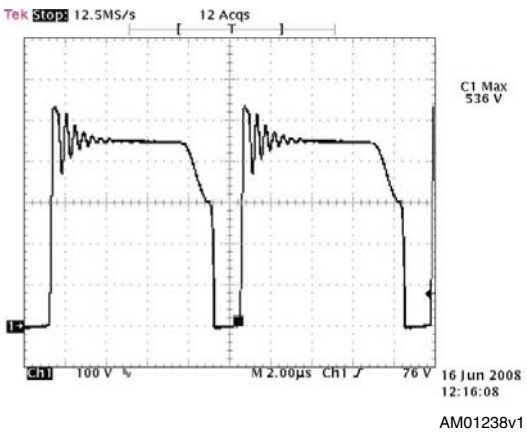
Figure 7. V_{IN} = 230 V_{AC} - 50 Hz, full load, frequency modulation



CH1: VIPER17HN drain pin (black trace)

In *Figure 8*, the drain voltage during full load operation at 265 V_{AC} is captured. As specified to the right of the illustration, the maximum peak voltage on the drain pin is 536 V, assuring good derating for reliable operation of the device.

Figure 8. V_{IN} = 265 V_{AC} - 50 Hz, full load, maximum drain peak voltage



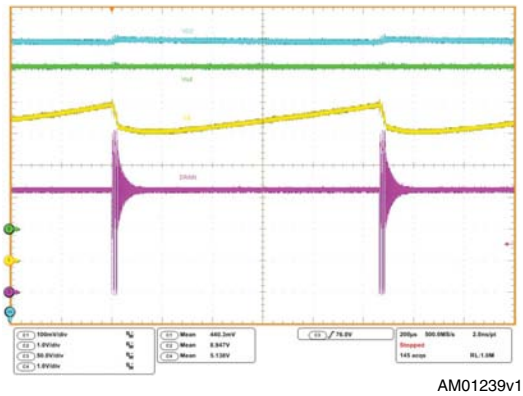
CH1: VIPER17HN drain pin (black trace)

2.1 No-load waveforms

During no-load conditions, the circuit operates in burst mode. Thanks to the VIPER17HN high voltage startup generator, low current consumption, low VDD voltage at no-load and the low consumption of the TSM1052, the input power is less than 100 mW over the entire input voltage range. *Figure 9* and *Figure 10* show the main waveforms in this condition.

During no-load operation, the burst frequency is around 1 kHz. However, due to the very low peak current, acoustic noise is not generated on the board.

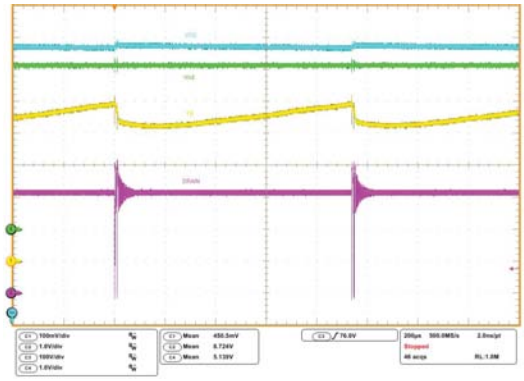
Figure 9. V_{IN} = 115 V_{AC} - 50 Hz in no-load condition



AM01239v1

CH1: VIPER17HN FB pin (yellow trace)
CH2: VIPER17HN VDD pin (cyan trace)
CH3: VIPER17HN drain pin (purple trace)
CH4: Output voltage (green)

Figure 10. V_{IN} = 230 V_{AC} - 50 Hz in no-load condition



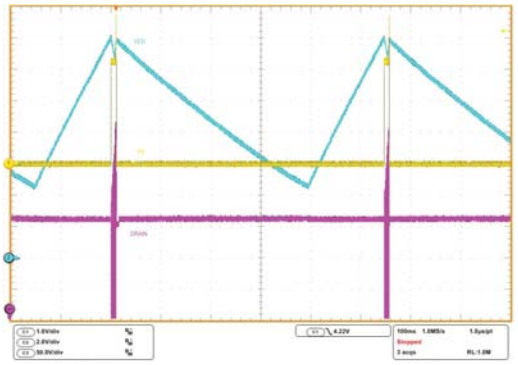
AM01240v1

CH1: VIPER17HN FB pin (yellow trace)
CH2: VIPER17HN VDD pin (cyan trace)
CH3: VIPER17HN drain pin (purple trace)
CH4: Output voltage (green)

3 Short-circuit operation

During output short-circuit conditions, the converter operates in hiccup mode (see *Figure 11*) due to the activation of the overload protection (OLP). Operation at both 115 V_{AC} and 230 V_{AC} is very similar, since neither the V_{DD} capacitor charge/discharge times nor the FB pin behavior depend on the bulk capacitor voltage. When a short-circuit is applied, the FB pin saturates high, and after about 8 ms the capacitors connected to that pin are charged up to 4.8 V (typ) and the OVL protection is triggered. Once the V_{DD} capacitor is discharged down to 4.5 V (typ.), the high voltage startup generator is turned on with reduced current (0.6 mA typ), then when the V_{DD} turn-on threshold is reached, the IC turns on and the cycle is repeated. Normal operation is restored after the short is removed (auto restart behavior).

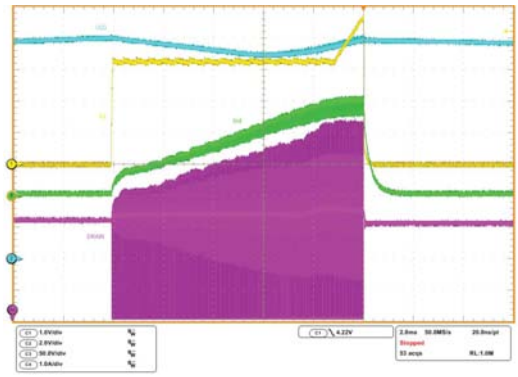
Figure 11. V_{IN} = 115 V_{AC} - 60 Hz short-circuit operation



AM01241v1

CH1: VIPER17HN FB pin (yellow trace)
CH2: VIPER17HN VDD pin (cyan trace)
CH3: VIPER17HN drain pin (purple trace)

Figure 12. V_{IN} = 230 V_{AC} - 50 Hz short-circuit operation detail

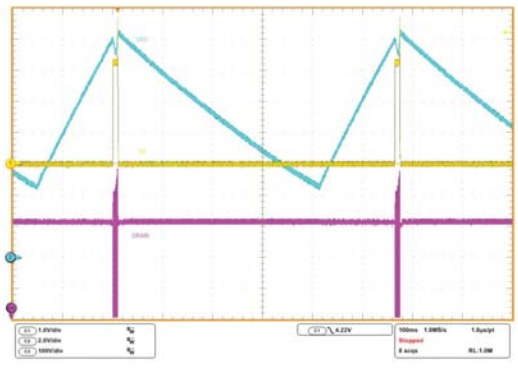


AM01242v1

CH1: VIPER17HN FB pin (yellow trace)
CH2: VIPER17HN VDD pin (cyan trace)
CH3: VIPER17HN drain pin (purple trace)
CH4: output current (green)

As illustrated in figures *13* and *14*, even at 230 V_{AC} the circuit behavior remains unchanged, and even at higher input voltage the working time in short-circuit condition is extremely short with respect to the off time. This permits limited dissipation for the power components and, since the components are not subject to excessive thermal stress, reliable operation of the circuit. Even the drain voltage peak during this condition is well below the VIPER17HN maximum rating for that pin.

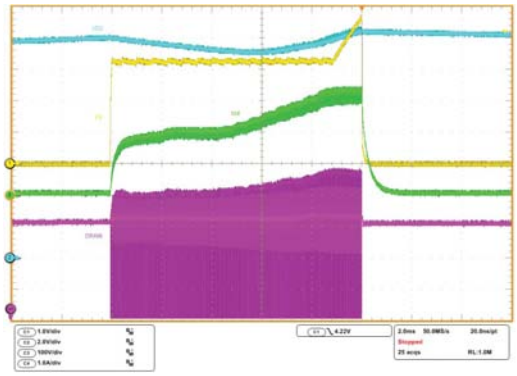
Figure 13. V_{IN} = 115 V_{AC} - 60 Hz short-circuit operation



AM01243v1

CH1: VIPER17HN FB pin (yellow trace)
CH2: VIPER17HN VDD pin (cyan trace)
CH3: VIPER17HN drain pin (purple trace)

Figure 14. V_{IN} = 230 V_{AC} - 50 Hz short-circuit operation detail



AM01244v1

CH1: VIPER17HN FB pin (yellow trace)
CH2: VIPER17HN VDD pin (cyan trace)
CH3: VIPER17HN drain pin (purple trace)
CH4: output current (green)

4 Electrical performance

4.1 Efficiency and no-load measurements

Tables *1* and *2* show board efficiency at the two nominal voltages.

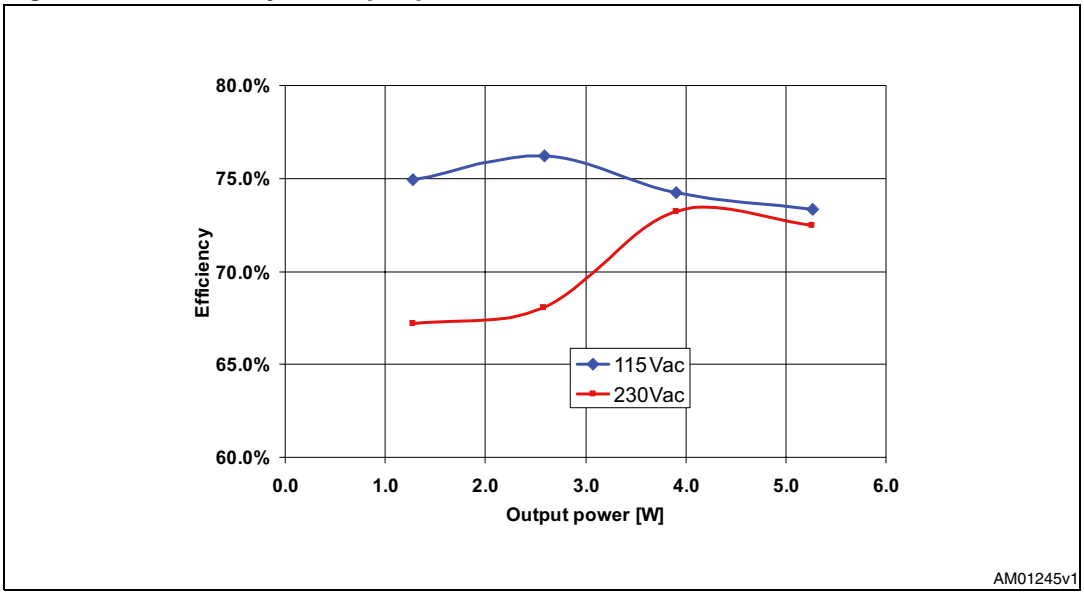
Table 1. Efficiency at 115 V_{AC}

% load	Io [A]	Vo [V]	Po [W]	Iin [mA]	Pin [W]	Efficiency
25%	0.2501	5.118	1.2800	32.5	1.708	74.9%
50%	0.5005	5.165	2.5851	57.0	3.391	76.2%
75%	0.7507	5.205	3.9074	82.0	5.263	74.2%
100%	0.9993	5.275	5.2713	106.6	7.19	73.3%
Average efficiency						74.7%

Table 2. Efficiency at 230 V_{AC}

% load	Io [A]	Vo [V]	Po [W]	Iin [mA]	Pin [W]	Efficiency
25%	0.2501	5.118	1.2800	22.5	1.905	67.2%
50%	0.5004	5.163	2.5836	39.8	3.795	68.1%
75%	0.7507	5.197	3.9014	52.4	5.328	73.2%
100%	0.9993	5.262	5.2583	67.4	7.256	72.5%
Average efficiency						70.2%

Figure 15. Efficiency vs output power



This adapter complies with the new EPA 2.0 standard for low voltage devices (V_{OUT} < 6, I_{OUT} > 0.55 A). The minimum required efficiency for a 5 W SMPS is 68.2%. This value has to be calculated as the average of the efficiency at 25%, 50%, 75% and 100% of rated load.

The input power without load has also been measured and as indicated in *Table 3*, the no-load consumption is always below 100 mW. Therefore, this adapter using the VIPER17HN meets the most restrictive worldwide standards regarding efficiency and power consumption at no-load (European Code of Conduct, adapter for mobile handheld battery-driven applications, starting from 1st January 2011: <150 mW).

Output voltage regulation during no-load operation is always good, and output voltage delivered is always within the specification. Neither output voltage drops nor abnormal turn-off and restarting cycles are present during no-load operation or load transients.

Table 3. No-load consumption

	$90V_{AC}$	$100V_{AC}$	$115V_{AC}$	$230V_{AC}$	$264V_{AC}$
V_{OUT} [V]	5.07	5.07	5.07	5.07	5.07
Pin [mW]	48	49.5	52	81.5	95

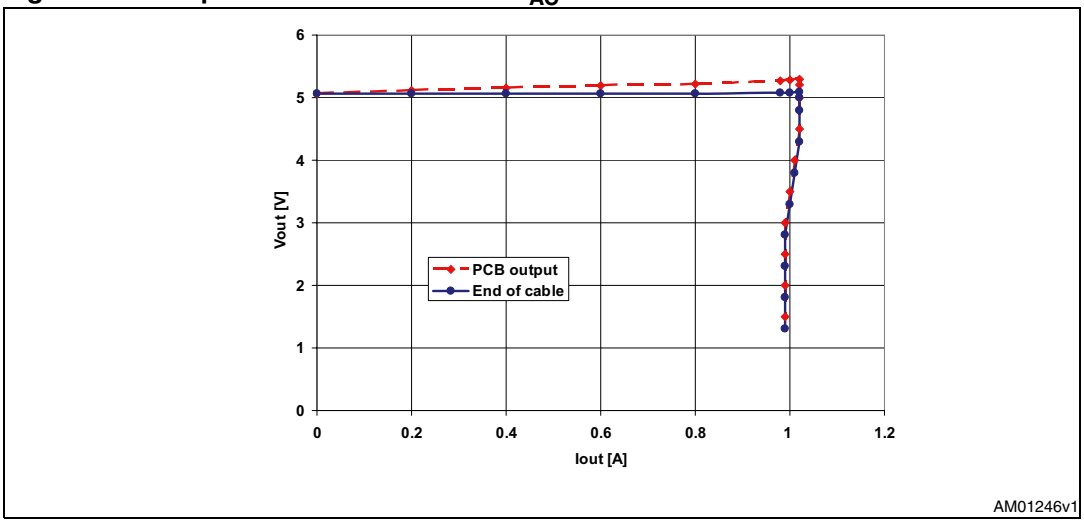
4.2 V-I output characteristics and cable drop compensation

Figure 16 shows the V-I output characteristics at the PCB output pads and at end of the output cable, measured at 115 V_{AC} mains input voltage. Values at 230 V_{AC} do not change significantly.

Due to the high performance of the TSM1052, in the constant current region the output voltage drops down to 1.5 V (1.3 V at the end of the output cable) while perfectly regulating the output current.

A further decrease in the output load impedance, as in the case of a short-circuit, causes an additional decrease in the output voltage that is insufficient to power the TSM1052. This results in a hiccup working mode with a very low average output current.

Figure 16. Output characteristic at 115 V_{AC}



This circuit behavior is present due to a design that uses the output voltage to power the TSM1052. Thanks to the very low V_{CC} of this device, the output current can be regulated even with a very small output voltage.

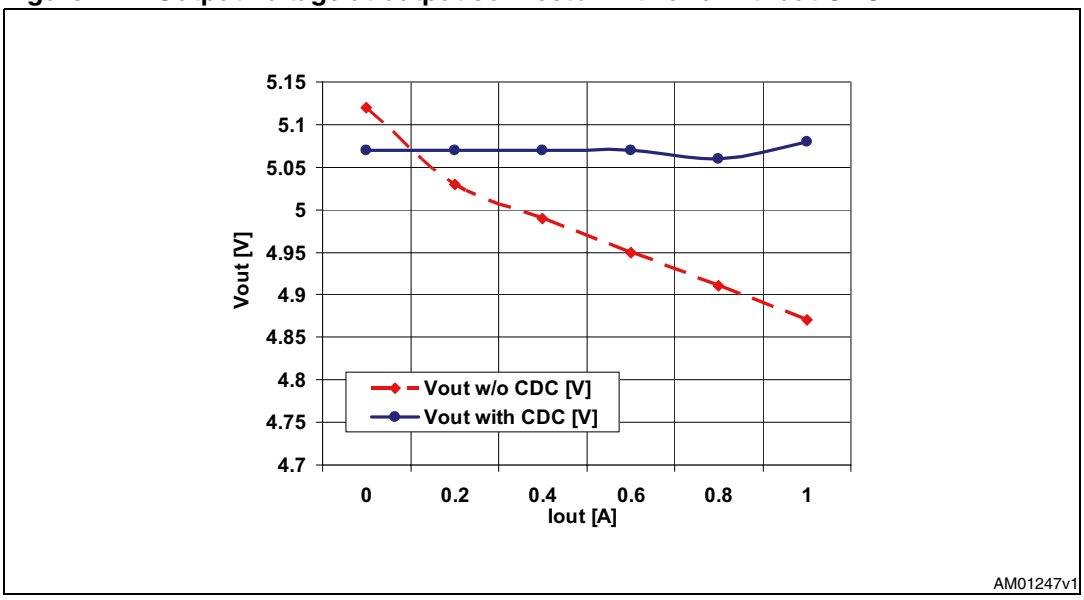
This application implements a simple circuit which compensates the voltage drop on the output cable. The effect can be noted in *Figure 16* and *Table 4*, which show the output voltage measured at the output connector, after the output cable in different load conditions. With the cable drop compensation (CDC) the output voltage is nearly constant, while without CDC the output voltage drops down to 4.87 V (about -3.9%) at maximum load.

The measurements are taken at 115 V_{AC}, but even at different input mains voltages deviations are negligible (a few millivolts).

Table 4. Output voltage at output connector

I_{OUT} [A]	0	0.2	0.4	0.6	0.8	1
V_{OUT} [V] with CDC	5.07	5.07	5.07	5.07	5.06	5.08
V_{OUT} [V] without CDC	5.12	5.03	4.99	4.95	4.91	4.87

Figure 17. Output voltage at output connector with and without CDC



5 Conducted noise measurements (pre-compliance test)

Figure 18 and *Figure 19* provide the results of the conducted emission pre-compliance measurements performed at maximum nominal voltage (230 V_{AC}) with quasi-peak and average detection. For conciseness, only the measurements of the worst line wire are reported. The measurements show a good margin with respect to the limits stated in the EN55022 CLASS-B specifications.

In comparing figures *18* and *19*, it is worth noting that the VIPER17HN frequency jittering feature makes it possible to spread the switching frequency harmonics spectrum and reduce the peak values. This is especially evident in the average measurement where a significant margin is achieved with respect to the limits.

Figure 18. V_{IN} = 230 V_{AC} – 50 Hz, full load CE QP measurement

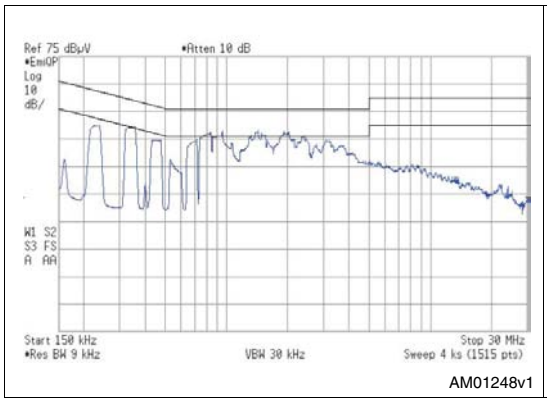
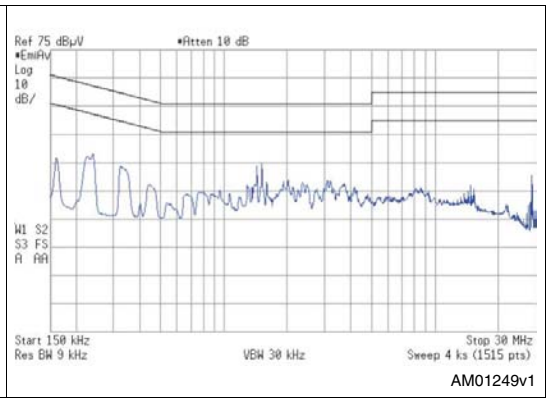
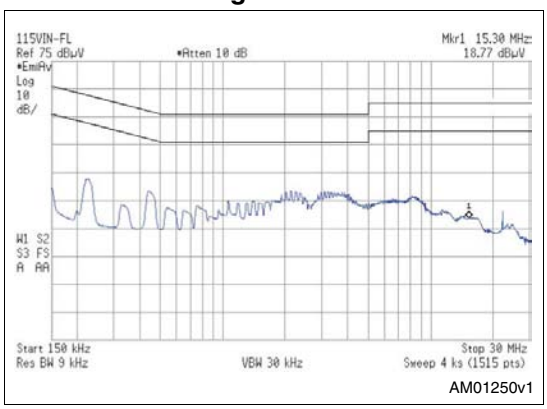


Figure 19. V_{IN} = 230 V_{AC} – 50 Hz full load CE average measurement



In *Figure 20*, the conducted emission in average mode is taken at 115 V_{AC}, full load. As the graph shows even in this condition the measured noise is well below the EN55022 Class-B limits.

Figure 20. V_{IN} = 115 V_{AC} - 60 Hz CE average measurement



6 Thermal measurements

A thermal analysis of the board is performed using an IR camera. The results are shown in *Figure 21* and *Figure 22* for 115 V_{AC} and 230 V_{AC} mains input. Both images refer to full load condition (P_{OUT} = 5 W).

- T_A = 26 °C for both figures
- Emissivity = 0.95 for all points

Figure 21. V_{IN} = 115 V_{AC}, full load, bottom and top sides

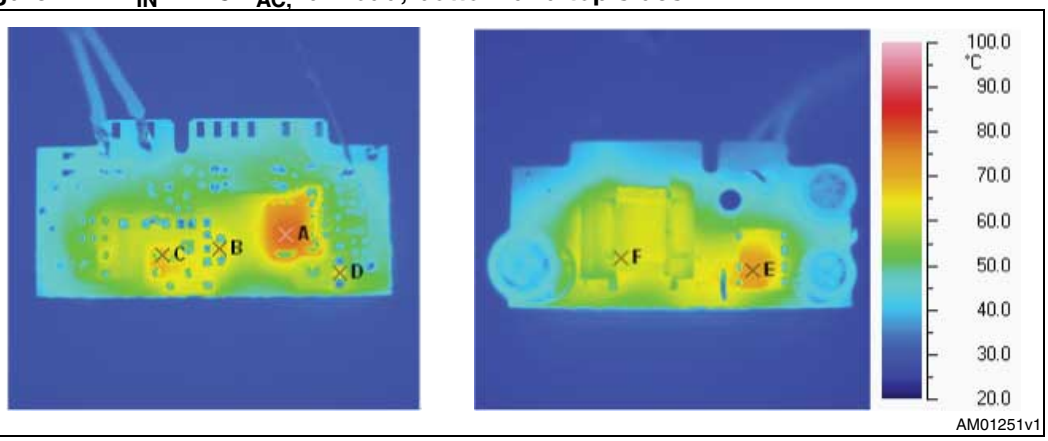


Figure 22. V_{IN} = 230 V_{AC}, full load, bottom and top sides

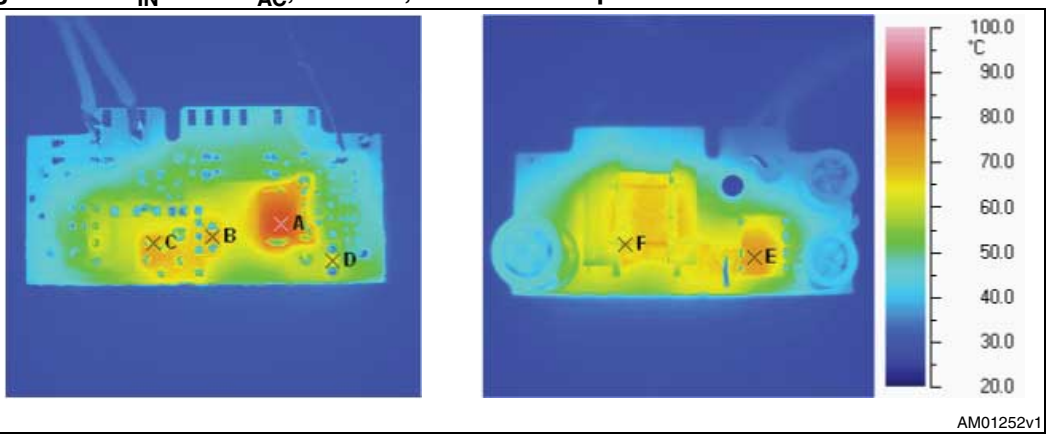


Table 5. Key component temperatures, full load

Point	Temperature [°C] at 115 V_{AC}	Temperature [°C] at 230 V_{AC}	Reference
A	78.4	80.6	D4 (output diode)
B	68.4	72.1	R1 (clamp)
C	69.5	71.8	Hot spot on PCB due to top side components
D	65.6	66.4	R11 (output current sense resistor)
E	73.7	74.1	IC2 (VIPER17HN)
F	69.7	72.8	TR1 (transformer)

7 Bill of materials

Table 6. EVLVIP17-5WCHG bill of materials

Ref	Description	Package	Manufacturer
C1, C2	Electr.cap. 4.7 µF 400 V 105 °C SEK	ø8x11 p3.5	Teapo/Yageo
C3	Electr.cap. 10 µF 50 V 105 °C	ø5x11 p2.5	
C4	Chip capacitor 1.5 nF/250 V X7R	0805	
C5	Chip capacitor 2.2 nF/25 V X7R	0603	
C6	Electr.cap. 1000 µF 16 V 105 °C SEK	Ø10x16 p5	Teapo/Yageo
C7	Chip capacitor 220 nF/16 V X7R	0603	
C8	Chip capacitor 100 nF/25 V X7R	0603	
C9	Chip capacitor 330 nF/25 V X7R	0805	
C10	Chip capacitor 10 nF/50 V X7R	0603	
C11	Chip capacitor 1 nF/50 V X7R	0603	
D1	Single phase bridge S1ZB60	MBS	
D2	Diode UF108G	D041	Panjit
D3	Diode BAV21WS	SOD323	
D4	Diode STPS3L40S	SMC	STMicroelectronics
F1	Fuse res. 10 Ω ±5% 2 W		
I1	Inductor 1 mH CECL-102K		Coils Electr.
IC1	OPTO SFH617-A3 X007	SMT	Vishay
IC2	I.C. VIPER17HN	DIP-7	STMicroelectronics
IC3	I.C. TSM1052CLT	SOT23-6L	STMicroelectronics
R1	Chip resistor 330 kΩ ±5%	1206	
R2	Chip resistor 100 Ω ±5%	1206	
R4	Chip resistor 22 Ω ±5%	0603	
R6	Chip resistor 330 Ω ±5%	0603	
R7	Chip resistor 22 kΩ ±1%	0603	
R8	Chip resistor 4.7 kΩ ±5%	0603	
R9	Chip resistor 22 kΩ ±1%	0603	
R10	Chip resistor 10 kΩ ±1%	0603	
R11	Chip resistor 0.2 Ω ±1% 200 ppm	1206	
R12	Chip resistor 1.8 kΩ ±5%	0805	
R13, R15, R18	Chip resistor 0 Ω	0603	
R14	Chip resistor 10 kΩ ±5%	0603	
R16	Chip resistor 15 kΩ ±1%	0603	
R17	Chip resistor 0 Ω	1206	
TR1	Transformer 1802.0006	EF12.6 LP	Magnetica

8 PCB layout

Figure 23. THT component layout (top side)

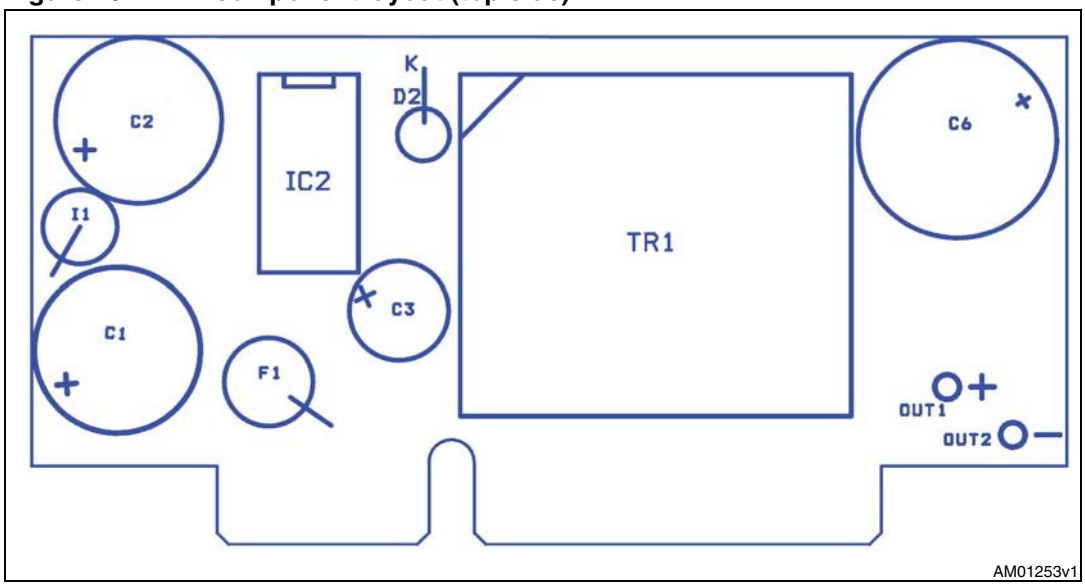
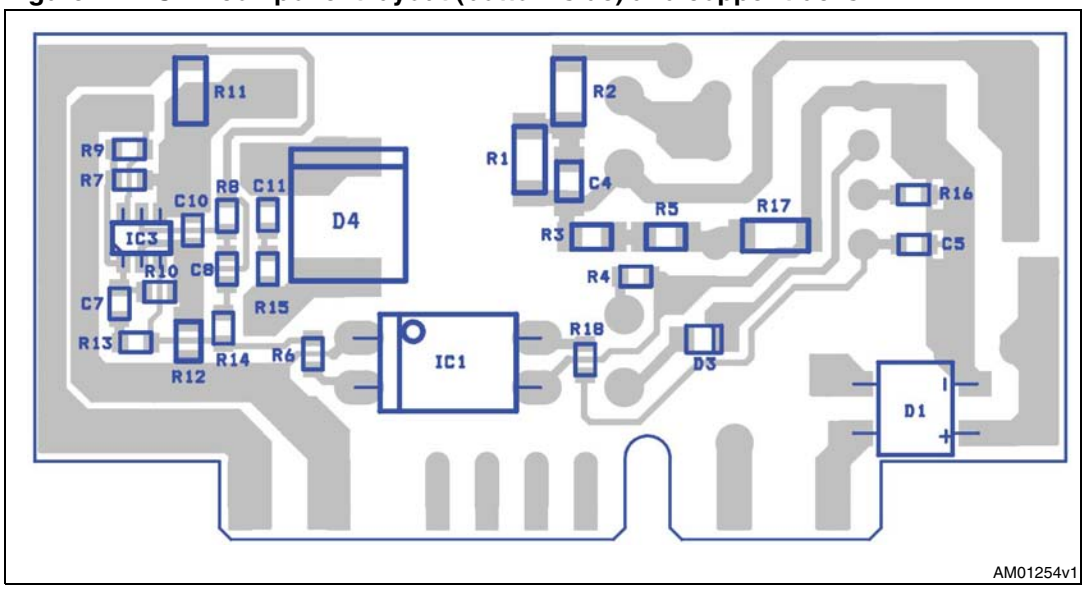


Figure 24. SMT component layout (bottom side) and copper tracks



9 Revision history

Table 7. Document revision history

Date	Revision	Changes
09-Dec-2008	1	Initial release