PIC16(L)F1777/8/9

PIC16(L)F1777/8/9 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F1777/8/9 family devices that you have received conform functionally to the current Device Data Sheet (DS40001819**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1777/8/9 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1777/8/9 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID Silicon Revision(2)
		A0
PIC16F1777	308Eh	2000h
PIC16LF1777	3091h	2000h
PIC16F1778	308Fh	2000h
PIC16LF1778	3092h	2000h
PIC16F1779	3090h	2000h
PIC16LF1779	3093h	2000h

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16(L)F177X Memory Programming Specification"* (DS40001792) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A0
Enhanced Universal Synchronous Receiver Transmitter (EUSART)	Transmit mode	1.1	Possible duplicate byte transmitted.	X
Master Synchronous Serial Port (MSSP)	SPI Slave mode	2.1	SPI master releasing Slave Select during Slave Sleep mode corrupts data.	X
Master Synchronous Serial Port (MSSP)	SPI Slave mode	2.2	SPI master enabling Slave Select too early could lose received data in Slave mode.	X
Master Synchronous Serial Port (MSSP)	SPI Slave mode	2.3	WCOL is erroneously set in SPI Slave mode during Sleep.	X
Programmable Ramp Generator (PRG)	Timing Sources	3.1	Configurable Logic Cell (CLC) timing sources not available.	X
ECCP	Compare mode	4.1	Compare Toggle mode yields unexpected results.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0**).

1. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

1.1 Transmit Mode

Under certain conditions, a byte written to the TXxREG register can be transmitted twice. This happens when a byte is written to TXxREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXxREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXxREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

When transmitting bytes, it is common practice to check the TXIF bit before writing to the TXxREG register. To avoid the issue of duplicate bytes being transmitted, a NOP should be placed before the write to the TXxREG register. This changes the timing so that the issue does not occur. The TRMT bit can also be checked in addition to or instead of the TXIF bit to determine if TXxREG can be written without causing a duplicate byte transmission. If the Transmit Interrupt is enabled, then inside the Interrupt Service Routine (ISR) testing, the TRMT bit will avoid transmission of a duplicate byte.

Affected Silicon Revisions

A0							
X							

2. Module: Master Synchronous Serial Port (MSSP)

2.1 SPI Slave Mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master releases the $\overline{SS}$ line ($\overline{SS}$ goes high) before the device wakes from Sleep and updates SSPxBUF, the received data will be lost.

Work around

Method 1: The SPI master must wait a minimum of parameter SP83 (1.5 T_{CY} + 40 ns) after the last SCK edge and the additional wake-up time from Sleep (device dependent) before releasing the $\overline{SS}$ line.

Method 2: If both the master and slave devices have an available pin, once the slave has completed the transaction and BF or SSPIF is set, the slave could toggle an output to inform the master that the transaction is complete and that it is safe to release the $\overline{SS}$ line.

Affected Silicon Revisions

A0							
X							

2.2 SPI Slave Mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master enables $\overline{SS}$ ($\overline{SS}$ goes low) within 1 T_{CY} before Sleep is executed, the data written into the SSPxBUF by the slave for transmission will remain in the SSPxBUF, and the byte received by the slave will be completely discarded. The MSb of the data byte that is currently loaded into SSPxBUF will be transmitted on each of the eight SCK clocks, resulting in either a 0x00 or 0xFF to be incorrectly transmitted. This issue typically occurs when the device wakes up from Sleep to process data and immediately goes back to Sleep during the next transmission.

Work around

The SPI slave must wait a minimum of 2.25 * T_{CY} from the time the $\overline{SS}$ line becomes active ($\overline{SS}$ goes low) before executing the Sleep command.

Affected Silicon Revisions

A0							
X							

2.3 SPI Slave Mode

When the MSSP module is configured with either of the Slave modes listed below and Sleep is executed during transmission, the WCOL bit is erroneously set. Although the WCOL bit is set, it does not cause a break in transmission or reception.

Mode 1: SPI Slave mode with $\overline{SS}$ disabled (SSPM = 0101) and CKE = 0.

Mode 2: SPI Slave mode with $\overline{SS}$ enabled (SSPM = 0100) and $\overline{SS}$ not set and then cleared before each consecutive transmission. This typically occurs during multiple byte transmissions in which the master does not release the $\overline{SS}$ line until all transmission has completed.

Work around

Method 1: The WCOL bit can be ignored since the issue does not interfere with MSSP hardware.

Method 2: Clear the SSPEN bit after each transaction, then set SSPEN before next transaction.

Affected Silicon Revisions

A0							
X							

3. Module: Programmable Ramp Generator (PRG)

3.1 Timing Sources

The Configurable Logic Cell (CLC) timing sources LC1_out, LC2_out, LC3_out, and LC4_out as defined in Table 30-5 of the data sheet are not available in the A0 revision. Use of these resources will result in unexpected operation.

Work around

None.

Affected Silicon Revisions

A0							
X							

4. Module: ECCP

4.1 Compare Mode

The ECCP Compare Toggle mode (CCP1M<3:0> bits = 0010) works properly as long as the Timer1 Prescaler value is configured to 1:1. When the Timer1 prescaler value is configured to any other value, the ECCP compare output yields unexpected results.

Work around

Only use the Compare Toggle mode when the Timer1 Prescaler value is set to 1:1.

Affected Silicon Revisions

A0							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001819**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Bank 6

Bank 6 was modified in Table 3-4 and 3-18, as follows:

TABLE 3-4: PIC16(L)F1777/9 MEMORY MAP (BANKS 0-7)

BANK 6	
300h 30Bh	Core Registers (Table 3-2)
30Ch	SLRCONA
30Dh	SLRCONB
30Eh	SLRCONC
30Fh	SLRCOND
310h	SLRCONE
311h	**CCPR8L**
312h	**CCPR8H**
313h	**CCP8CON**
314h	**CCP8CAP**
315h	MD1CON0
316h	MD1CON1
317h	MD1SRC
318h	MD1CARL
319h	MD1CARH
31Ah	—
31Bh	MD2CON0
31Ch	MD2CON1
31Dh	MD2SRC
31Eh	MD2CARL
31Fh	MD2CARH
320h General Purpose Register 80 Bytes 36Fh	
370h 37Fh	Accesses 70h – 7Fh

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 6											
30Ch	SLRCONA	SLRA7	SLRA6	SLRA5	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0	1111 1111	1111 1111
30Dh	SLRCONB	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0	1111 1111	1111 1111
30Eh	SLRCONC	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	1111 1111	1111 1111
30Fh	SLRCOND(3)	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	1111 1111	1111 1111
310h	SLRCONE(3)	—	—	—	—	—	SLRE2	SLRE1	SLRE0	---- -111	---- -111
311h	**CCPR8L**	Capture/Compare/PWM **Register 8** (LSB)								xxxx xxxx	uuuu uuuu
312h	**CCPR8H**	Capture/Compare/PWM **Register 8** (MSB)								xxxx xxxx	uuuu uuuu
313h	**CCP8CON**	EN	—	OUT	FMT	MODE<3:0>				0-00 0000	0-00 0000
314h	**CCP8CAP**	—	—	—	—	CTS<3:0>				---- 0000	---- 0000
315h	MD1CON0	EN	—	OUT	OPOL	—	—	—	BIT	0-00 ---0	0-00 ---0
316h	MD1CON1	—	—	CHPOL	CHSYNC	—	—	CLPOL	CLSYNC	--00 --00	--00 --00
317h	MD1SRC	—	—	—	MS<4:0>					---0 0000	---0 0000
318h	MD1CARL	—	—	—	CL<4:0>					---0 0000	---0 0000
319h	MD1CARH	—	—	—	CH<4:0>					---0 0000	---0 0000
31Ah	—	Unimplemented								—	—
31Bh	MD2CON0	EN	—	OUT	OPOL	—	—	—	BIT	0-00 ---0	0-00 ---0
31Ch	MD2CON1	—	—	CHPOL	CHSYNC	—	—	CLPOL	CLSYNC	--00 --00	--00 --00
31Dh	MD2SRC	—	—	—	MS<4:0>					---0 0000	---0 0000
31Eh	MD2CARL	—	—	—	CL<4:0>					---0 0000	---0 0000
31Fh	MD2CARH	—	—	—	CH<4:0>					---0 0000	---0 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

2. Module: Bank 12

Bank 12 was modified in Table 3-6, Table 3-7 and Table 3-18, as follows:

TABLE 3-6: PIC16(L)F1777 MEMORY MAP

BANK 12	
600h 60Bh	Core Registers (Table 3-2)
60Ch	DAC8CON0
60Dh	DAC8REFL
60Eh	**PRG4RTSS**
60Fh	**PRG4FTSS**
610h	**PRG4INS**
611h	**PRG4CON0**
612h	**PRG4CON1**
613h	**PRG4CON2**
614h	PWM3DCL
615h	PWM3DCH
616h	PWM3CON
617h	PWM4DCL
618h	PWM4DCH
619h	PWM4CON
61Ah	PWM9DCL
61Bh	PWM9DCH
61Ch	PWM9CON
61Dh	PWM10DCL
61Eh	PWM10DCH
61Fh	PWM10CON
620h 66Fh	General Purpose Register 80 Bytes
670h 67Fh	Accesses 70h – 7Fh

TABLE 3-7: PIC16(L)F1779 MEMORY MAP

BANK 12	
600h 60Bh	Core Registers (Table 3-2)
60Ch	DAC8CON0
60Dh	DAC8REFL
60Eh	**PRG4RTSS**
60Fh	**PRG4FTSS**
610h	**PRG4INS**
611h	**PRG4CON0**
612h	**PRG4CON1**
613h	**PRG4CON2**
614h	PWM3DCL
615h	PWM3DCH
616h	PWM3CON
617h	PWM4DCL
618h	PWM4DCH
619h	PWM4CON
61Ah	PWM9DCL
61Bh	PWM9DCH
61Ch	PWM9CON
61Dh	PWM10DCL
61Eh	PWM10DCH
61Fh	PWM10CON
620h 66Fh	General Purpose Register 80 Bytes
670h 67Fh	Accesses 70h – 7Fh

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 12											
60Ch to 613h	—	Unimplemented								—	—
60Ch	DAC8CON0(3)	EN	—	OE1	OE2	PSS<1:0>		NSS1	NSS0	0-00 0000	0-00 0000
60Dh	DAC8REF(3)	—	—	—	REF<4:0>					---0 0000	0000 0000
60Eh	**PRG4RTSS(3)**	—	—	—	—	RTSS<3:0>				---- 0000	---- 0000
60Fh	**PRG4FTSS(3)**	—	—	—	—	FTSS<3:0>				---- 0000	---- 0000
610h	**PRG4INS(3)**	—	—	—	—	INS<3:0>				---- 0000	---- 0000
611h	**PRG4CON0(3)**	EN	—	FEDG	REDG	MODE<1:0>		OS	GO	0-000 0000	0-00 0000
612h	**PRG4CON1(3)**	—	—	—	—	—	RDY	FPOL	RPOL	---- -000	---- -000
613h	**PRG4CON2(3)**	—	—	—	ISET<4:0>					---0 0000	---0 0000
614h	PWM3DCL	DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
615h	PWM3DCH	DC<9:2>								xxxx xxxx	uuuu uuuu
616h	PWM3CON	EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----
617h	PWM4DCL	DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
618h	PWM4DCH	DC<9:2>								xxxx xxxx	uuuu uuuu
619h	PWM4CON	EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----
61Ah	PWM9DCL	DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
61Bh	PWM9DCH	DC<9:2>								xxxx xxxx	uuuu uuuu
61Ch	PWM9CON	EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----
61Dh	PWM10DCL(3)	DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
61Eh	PWM10DCH(3)	DC<9:2>								xxxx xxxx	uuuu uuuu
61Fh	PWM10CON(3)	EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2015)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

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ISBN: 978-1-5224-0059-2

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