LTC2389
18-Bit/16-Bit, 2.5Msps Low Noise, SAR ADCs with Pin-Configurable Analog Input Range

DESCRIPTION

Demonstration circuit 1826A features the LTC®2389 low noise, high speed successive approximation register ADC which operates from a single 5V supply. The following text refers to the LTC2389-18, but also applies to the LTC2389-16, the only difference being the number of bits. The LTC2389-18 supports pin-configurable fully differential (±4.096V), pseudo-differential unipolar (0V to 4.096V), and pseudo-differential bipolar (±2.048V) analog input ranges, allowing it to interface with multiple signal chain formats. The LTC2389-18 achieves ±2.5LSB INL (maximum), with no missing codes at 18 bits.

The DC1826A demonstrates the performance of the LTC2389-18 in conjunction with the DC718 QuikEval™ II data collection board.

The demonstration circuit 1826A is intended to demonstrate recommended grounding, component placement and selection, routing and bypassing for this ADC. Several suggested driver circuits for the analog inputs will be presented.

Design files for this circuit board are available at http://www.linear.com/demo

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BOARD PHOTO

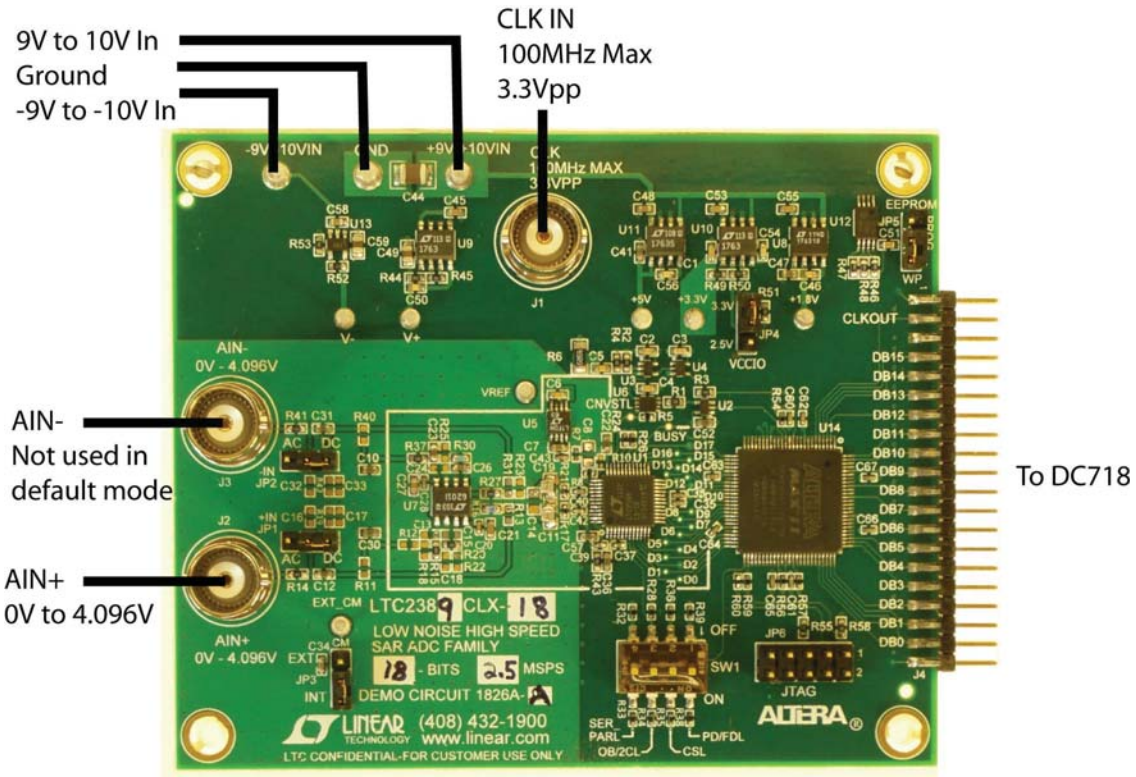

Figure 1. DC1826A Connection Diagram

DC1826A ASSEMBLY OPTIONS

ASSEMBLY VERSION	U1 PART NUMBER	MAX CONVERSION RATE	NUMBER OF BITS	SERIAL MAX CLKIN FREQUENCY
DC1826A-A	LTC2389CMS-18	2.5Msps	18	100MHz
DC1826A-E	LTC2389CMS-16	2.5Msps	16	100MHz

DC718 QUICK START PROCEDURE

Check to ensure that all switches and jumpers are set as shown in the connection diagram of Figure 1. The default connections configure the ADC to use the onboard reference and regulators to generate the required common mode voltages. The analog input is DC-coupled. Connect the DC1826A to a DC718 USB high speed data collection board using connector J4. Then, connect the DC718 to a host PC with a standard USB A/B cable. Apply ±9V to the indicated terminals. Then, apply a low jitter signal source to J2. The default setup uses a single-ended to differential converter so that it is only necessary to apply a single-ended input signal to J2. Connect a low jitter 2.5MHz (100MHz for serial) $3.3V_{P-P}$ sine wave or square wave to connector J1 for parallel operation. Note that J1 has a 49.9Ω termination resistor to ground.

Run the QuikEval II software (PScope.exe version K73 or later) supplied with the DC718 or download it from www.linear.com.

Complete software documentation is available from the help menu. Updates can be downloaded from the tools menu. Check for updates periodically as new features may be added.

The PScope™ software should recognize the DC1826A and configure itself automatically.

Click the collect button (see Figure 7) to begin acquiring data. The collect button then changes to pause, which can be clicked to stop data acquisition.

DC1826A SETUP

DC Power

The DC1826A requires $\pm 9V_{DC}$ and draws 100mA. Most of the supply current is consumed by the CPLD, opamps, regulators and discrete logic on the board. The $9V_{DC}$ input voltage powers the ADC through LT1763 regulators which provide protection against accidental reverse bias. Additional regulators provide power for the CPLD and opamps. See Figure 1 for connection details.

Clock Source

You must provide a low jitter $3.3V_{P-P}$ sine or square wave to J1. The clock input is AC-coupled so the DC level of the clock signal is not important. A generator like the HP8644 or the DC1216A-A is recommended. Even a good generator can start to produce noticeable jitter at low frequencies. Therefore, it is recommended for lower clock rates to divide down a higher frequency clock to the desired sample rate. For serial operation, the ratio of clock frequency to conversion rate is 50:1. The maximum serial conversion rate is 2Msps. If the clock input is to be driven with logic, it is recommended that

DC1826A SETUP

the 50Ω terminator (R6) be removed. Slow rising edges may compromise the SNR of the converter in the presence of high amplitude higher frequency input signals.

Data Output

Parallel data output from this board (0V to 3.3V default), if not connected to the DC718, can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use Pin 3 of J4 to latch the data. The data can be latched using either edge of this signal. The data output signal levels at J4 can also be reduced to 0V to 2.5V if the application circuit cannot tolerate the higher voltage. This is accomplished by moving JP4 to the 2.5V position.

Reference

The default reference is the LTC2389-18's internal 4.096V reference. If an external reference is desired use the on-board LTC6655-4.096 reference. It is enabled by stuffing 0Ω resistors R7, R9 and R10 and removing 0Ω resistor R8.

Analog Input

The default driver for the analog inputs of the LTC2389-18 on the DC1826A is shown in Figure 2. This circuit converts a single-ended 0V to 4.096V input signal applied at A_{IN}^+ into a differential signal with a swing of ±4.096V between the +IN and –IN inputs of the ADC. In addition, this circuit band limits the input frequencies to approximately 16MHz.

It is also possible to drive the LTC2389-18 pseudo differentially both with unipolar and bipolar outputs. The circuit of Figure 3 shows the pseudo-differential unipolar driver. This is connected on the DC1826A by removing R27 and placing 0Ω resistors in the R31 and R42 positions.

Figure 4 shows the pseudo-differential bipolar driver circuit. This is connected on the DC1826A by removing R29, R30, C25 and C26 and placing 0Ω in the R30 position.

Alternatively, if your application circuit produces a differential signal which can drive the ADC, the circuit shown in Figure 5 can be used. This is connected in the DC1826A by removing R29, R30, R37, C23, C25 and C26 and by adding a 0Ω resistor for R30 and R25. At this point it will be necessary to drive both A_{IN}^+ and A_{IN}^-.

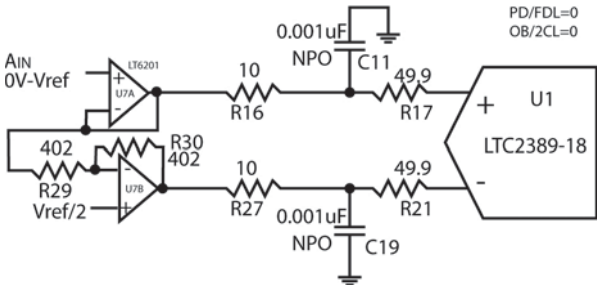

Figure 2. Default Driver Circuit

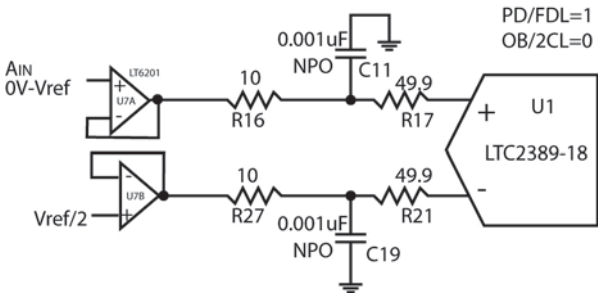

Figure 4. Pseudo-Differential Bipolar Driver

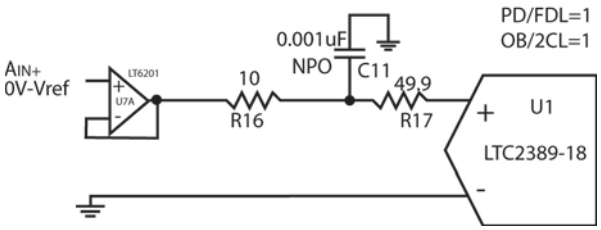

Figure 3. Pseudo-Differential Unipolar Driver

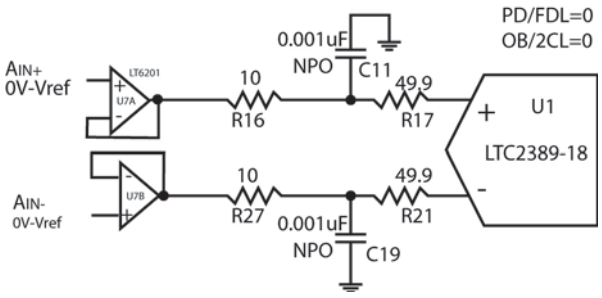

Figure 5. Fully Differential Driver

DC1826A SETUP

AC-Coupling the Inputs

The circuit in Figure 5 can be AC-coupled on the DC1826A by putting JP1 and JP2 in the AC position and adding a 1k resistor at the R11 and R40 locations. Using just JP1 and adding R11 allows a single-ended input signal to be AC-coupled. AC-coupling the inputs may degrade the distortion performance of the ADC due to nonlinearity of the coupling capacitors (C12 and C31).

Data Collection

For SINAD, THD or SNR testing, a low noise, low distortion generator such as the B&K Type 1051 or Stanford Research DS360 should be used. A low jitter RF oscillator such as the HP8644 or DC1216A-A is used as the clock source.

This demo board is tested in-house by attempting to duplicate the FFT plot shown in Figure 7a of the LTC2389-18 data sheet. This involves using a 2.5MHz clock source, along with a sinusoidal generator at a frequency of 2kHz. The input signal level is approximately –1dBfs. The input is level shifted and filtered with the circuit shown in Figure 6. A typical FFT obtained with DC1826A is shown in Figure 7. Note that to calculate the real SNR, the signal level (F1 amplitude = –0.998dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 7 this means that the actual SNR would be 98.50dB instead of the 97.52dB that PScope displays. Taking the RMS sum of the recalculated SNR and the THD yields a SINAD of 98dB which is fairly close to the typical number for this ADC.

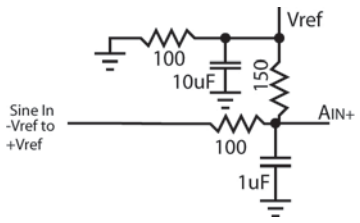

Figure 6. Level-Shift Circuit

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with a frequency that is a submultiple of the sample rate, and which will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and N/2. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a signal generator capable of ppm frequency accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the "leakage" or spreading of the fundamental, to get a close approximation of the ADC performance. If an amplifier or clock source with poor phase noise is used, the windowing will not improve the SNR.

Layout

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on the DC1826A should be used as a guideline for placement, and routing of the various components associated with the ADC. Here are some things to remember when laying out a board for the LTC2389-18. A ground plane is necessary to obtain maximum performance.

Keep bypass capacitors as close to supply pins as possible. Use individual low impedance returns for all bypass capacitors. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

Component Selection

When driving a low noise, low distortion ADC such as the LTC2389-18, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self heating. Because of their low voltage coefficients, to further reduce distortion NPO or silver mica capacitors should be used. Any buffer used to drive the LTC2389-18 should have low distortion, low noise and a fast settling time such as the LT6350.

DC1826A SETUP

Jumper and Switch Functions

JP1: Selects AC- or DC-coupling of A_{IN}^+. The default setting is DC.

JP2: Selects AC- or DC-coupling of A_{IN}^-. The default setting is DC.

JP3: V_{CM} sets the DC bias for A_{IN}^+ and A_{IN}^- when the inputs are AC-coupled. $V_{REF}/2$ is the default setting.

JP4: VCCIO sets the output levels at J2 to either 3.3V or 2.5V. Use 3.3V to interface to the DC718 which is the default setting.

JP5: EEPROM default position is WP. The position of this jumper should not be changed.

SW1

SER_PARL: Off enables serial operation. Sample rate is the CLKIN frequency divided by 50. On enables parallel operation. Sample rate is equal to the CLKIN frequency.

OB/2CL: Off enables offset binary output code in fully-differential mode and unipolar range with straight binary code in pseudo-differential mode. On enables 2's complement output code in fully-differential mode and bipolar range with 2's complement output code in pseudo-differential mode.

CSL: Off disables SDO and gates SCK off. On enables SDO and gates SCK on.

PD/FDL: Off enables pseudo-differential mode. On enables fully-differential mode.

The default position for all switches is on.

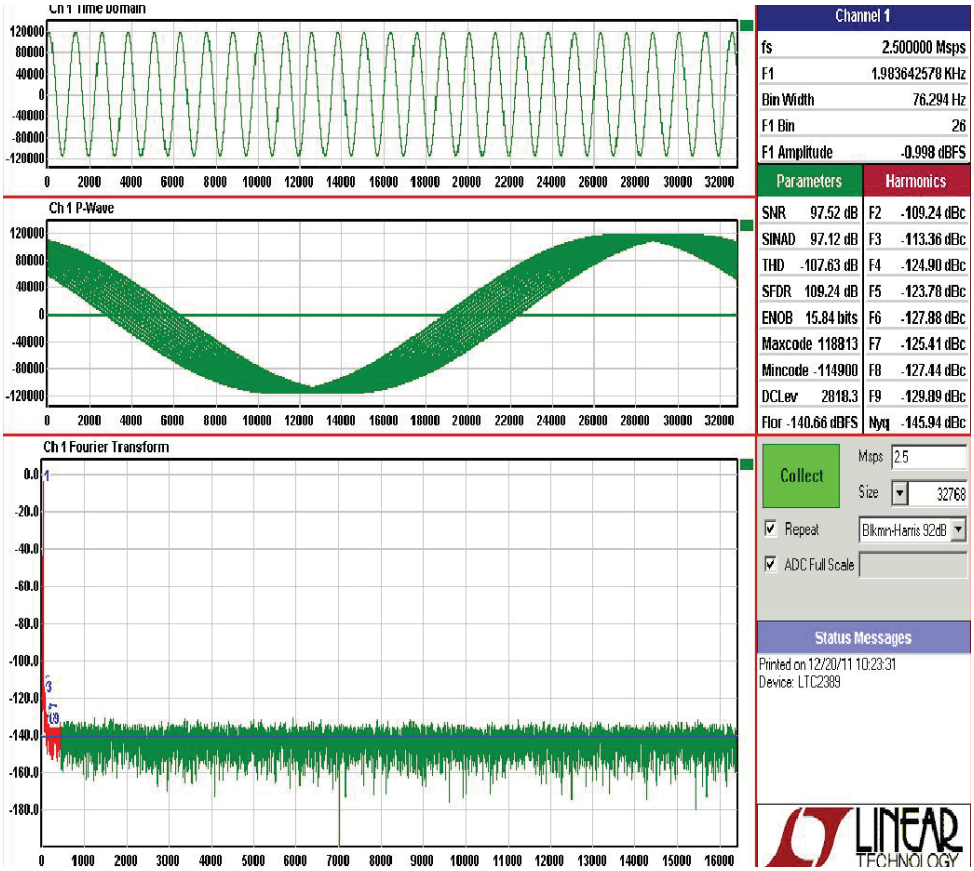

Figure 7. PScope Screenshot

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1826A Required Circuit Components				
1	7	C1, C2, C3, C4, C5, C6, C51	Cap., X7R, 0.1µF, 25V, 10%, 0603	AVX 06033C104KAT2A
2	5	C7, C21, C27, C29, C34	Cap., X5R, 1µF, 25V, 20%, 0603	AVX 06033D105MAT2A
3	0	C8, C14 (OPT)	Cap., 0805	
4	1	C9	Cap., X5R, 1µF, 25V, 10%, 0805	AVX 08053D105KAT2A
5	11	C10, C12, C22, C23, C30, C31, C36, C41, C47, C52, C57	Cap., X5R, 10µF, 6.3V, 20%, 0603	Taiyo Yuden JMK107BJ106MA-T
6	2	C11, C19	Cap., X7R, 1000pF, 50V, 10%, 0805	AVX 08055C102KAT1A
7	0	C13, C15, C16, C17, C18, C24, C32, C33 (OPT)	Cap., 0603	
8	17	C20, C28, C35, C37, C38, C39, C40, C42, C43, C60, C61, C62, C63, C64, C65, C66, C67	Cap., X5R, 0.1µF, 10V, 10%, 0402	AVX 0402ZD104KAT2A
9	2	C25, C26	Cap., NPO, 330pF, 25V, 5%, 0603	AVX 06033A331JAT1A
10	1	C44	Cap., X5R, 47µF, 16V, 20%, 1210	Taiyo Yuden EMK325BJ476MM
11	5	C45, C48, C53, C55, C58	Cap., X7R, 1µF, 16V, 20%, 0603	AVX 06033C105MAT2A
12	4	C46, C50, C54, C56	Cap., X7R, 0.01µF, 100V, 10%, 0603	AVX 06031C103KAT2A
13	2	C49, C59	Cap., X5R, 10µF, 10V, 20%, 0805	Taiyo Yuden LMK212BJ106MG
14	7	E1, E2, E4, E5, E7, E8, E10	Turret, Testpoint	Mill Max 2308-2-00-80-00-00-07-0
15	3	E3, E6, E9	Turret, Testpoint	Mill Max 2501-2-00-80-00-00-07-0
16	5	JP1, JP2, JP3, JP4, JP5	Headers, 3 Pins, 100mil Ctrs.	Samtec TSW-103-07-L-S
17	1	JP6	Headers, Dbl. Row, 2 x 5, 100mil Ctrs.	Samtec TSW-105-07-L-D
18	3	J1, J2, J3	BNC Connector	Connex 112404
19	1	J4	Box Conn, 0.1 Ctr, 40 Pin	Samtec TSW-120-07-L-D
20	4	MH1, MH2, MH3, MH4	Stacking Spacers, Snap-On, 0.25" Tall	Keystone 8831
21	2	R1, R3	Res., Chip, 33, 0.06W, 5%, 0603	Vishay CRCW060333R0JNEA
22	3	R2, R4, R58	Res., Chip, 1k, 0.06W, 5%, 0603	Vishay CRCW06031k,00JNEA
23	1	R5	Res., Chip, 33, 0.06W, 5%, 0402	Vishay CRCW040233R0JNED
24	1	R6	Res., Chip, 49.9, 0.25W, 1%, 1206	Vishay CRCW120649R9FKEA
25	0	R7, R9, R10 (OPT)	Res., 0402	
26	1	R8	Res./Jumper, Chip, 0Ω, 1/16W, 1A, 0402	Vishay CRCW04020000Z0ED
27	0	R11, R12, R13, R18, R19, R22, R23, R25, R31, R40, R42 (OPT)	Res., 0603	
28	4	R14, R15, R20, R41	Res./Jumper, Chip, 0Ω, 1/16W, 1A, 0603	Vishay CRCW06030000Z0EA
29	2	R16, R27	Res., Chip, 10, 0.06W, 5%, 0603	Vishay CRCW060310R0JNEA
30	2	R17, R21	Res., Chip, 49.9, 0.06W, 1%, 0402	Vishay CRCW040249R9FKED

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
31	5	R24, R26, R54, R56, R57	Res., Chip, 1k, 0.06W, 5%, 0402	Vishay CRCW04021k,00JNED
32	5	R28, R32, R36, R39, R59	Res., Chip, 10k, 0.06W, 5%, 0402	Vishay CRCW040210k,0JNED
33	2	R29, R30	Res., Chip, 402, 0.06W, 1%, 0402	Vishay CRCW0402402RFKED
34	4	R33, R34, R35, R38	Res., Chip, 300, 0.06W, 5%, 0402	Vishay CRCW0402300RJNED
35	1	R37	Res., Chip, 75, 0.06W, 5%, 0603	Vishay CRCW060375R0JNEA
36	1	R43	Res., Chip, 0Ω, 0.06W, 1A, 0603	Vishay CRCW06030000Z0EA
37	1	R44	Res., Chip, 3.92k, 0.06W, 1%, 0603	Vishay CRCW06033K92FKEA
38	2	R45, R53	Res., Chip, 1.00k, 0.06W, 1%, 0603	Vishay CRCW06031k,00FKEA
39	3	R46, R47, R48	Res., Chip, 4.99k, 0.06W, 1%, 0603	Vishay CRCW06034K99FKEA
40	1	R49	Res., Chip, 1.69k, 0.06W, 1%, 0603	Vishay CRCW06031k,69FKEA
41	1	R50	Res., Chip, 1.54k, 0.06W, 1%, 0603	Vishay CRCW06031k,54FKEA
42	1	R51	Res., Chip, 2.80k, 0.06W, 1%, 0603	Vishay CRCW06032K80FKEA
43	1	R52	Res., Chip, 665, 0.06W, 1%, 0603	Vishay CRCW0603665RFKEA
44	1	R55	Res., Chip, 10k, 0.06W, 5%, 0603	Vishay CRCW060310k,0JNEA
45	0	R60 (**OPT)	Res., Chip, 301, 0.06W, 1%, 0402	Vishay CRCW0402301RFKED
46	1	SW1	Switch, Slide, SW-219-4M	CTS Electronic Components 219-4MST
47	0	TP1, TP2 (OPT)	Testpoint, Test Pad	Component Corp. TP-107-02
48	2	U2, U4	I.C., Inverter, SC70-5	Fairchild Semi. NC7SV,U04P5X
49	1	U3	I.C., Inverter, SC70-5	Fairchild Semi. NC7SZ04P5X
50	1	U5	I.C., Precision Buff., Ref., MSOP(08)-MS8	Linear Technology Corp., LTC6655BHMS8-4.096
51	1	U6	I.C., Single D, Flip Flop, US8	ON Semi. NL17SZ74USG PbF
52	1	U7	I.C., Op Amp, SO(08) (Narrow-150mil)	Linear Technology Corp., LT6201IS8
53	1	U8	I.C., mPower Regulator, SO(08) (Narrow-150mil)	Linear Technology Corp., LT1763CS8-1.8
54	2	U9, U10	I.C., mPower Regulator, SO(08) (Narrow-150mil)	Linear Technology Corp., LT1763CS8
55	1	U11	I.C., mPower Regulator, SO(08) (Narrow-150mil)	Linear Technology Corp., LT1763CS8-5
56	1	U12	I.C., Serial EEPROM, TSSOP-8	Microchip, 24LC024-I/ST
57	1	U13	I.C., mPower Regulator, TSOT23-S5	Linear Technology Corp., LT1964ES5-SD
58	1	U14	I.C., Max II Family, EPM240T	Altera EPM240GT100C5N
59	5	XJP1, XJP2, XJP3, XJP4, XJP5	Shunt, 0.1" Ctrs.	Samtec SNT-100-BK-G

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1826A-A Required Circuit Components				
1	1	DC1826A	General BOM	
2	1	R60	Res., Chip, 301, 0.06W, 1%, 0402	Vishay CRCW0402301RFKED
3	1	U1	IC, LTC2389CLX-18	Linear Technology Corp., LTC2389CLX-18
4	1		Fab, Printed Circuit Board	Demo Circuit DC1826A
DC1826A-E Required Circuit Components				
1	1	DC1826A	General BOM	
2	1	U1	IC, LTC2389CLX-16	Linear Technology Corp., LTC2389CLX-16
3	1		Fab, Printed Circuit Board	Demo Circuit DC1826A

SCHEMATIC DIAGRAMS

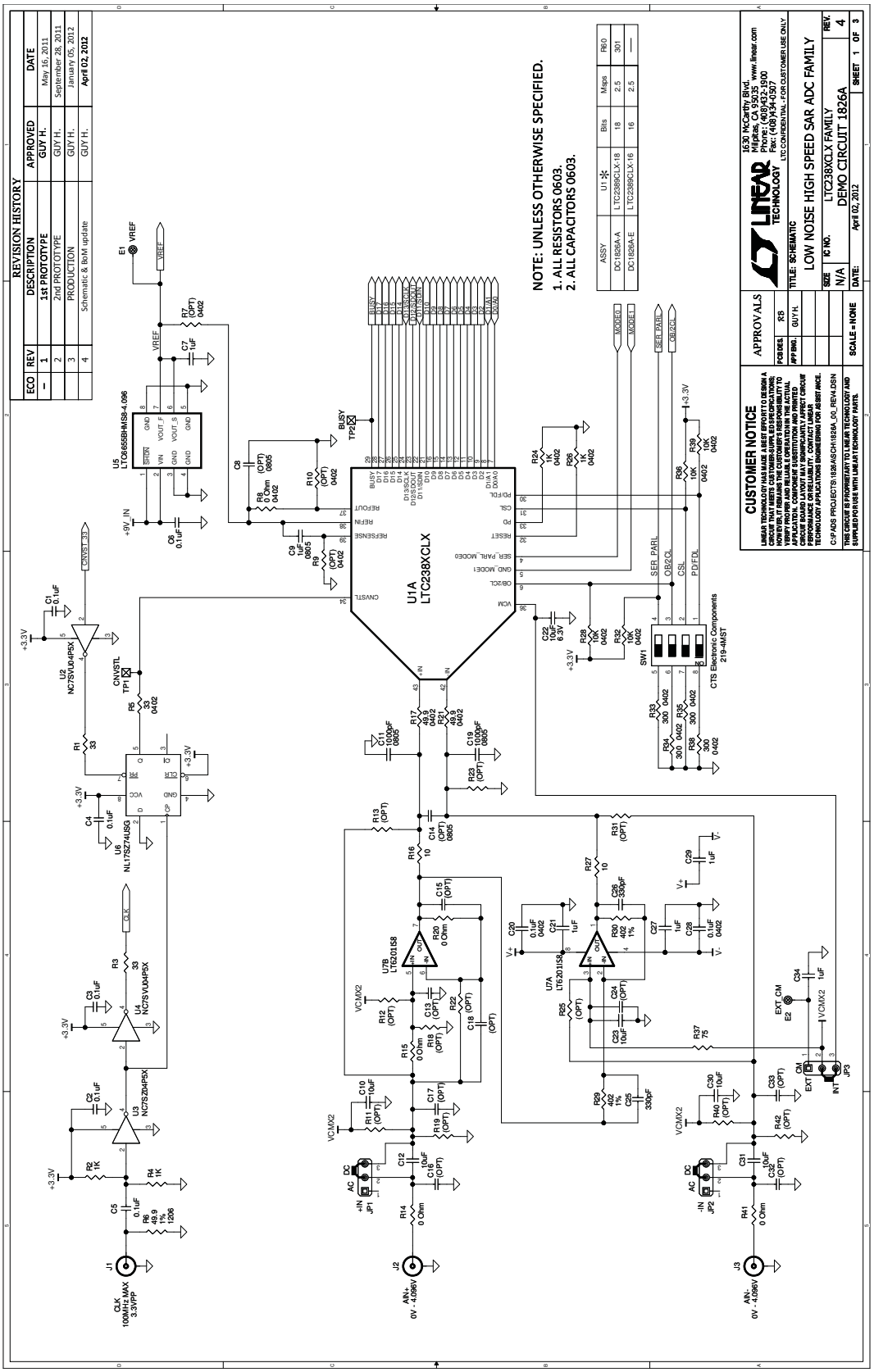

Figure 8. DC1826A Low Noise, High Speed SAR ADC Family

SCHEMATIC DIAGRAMS

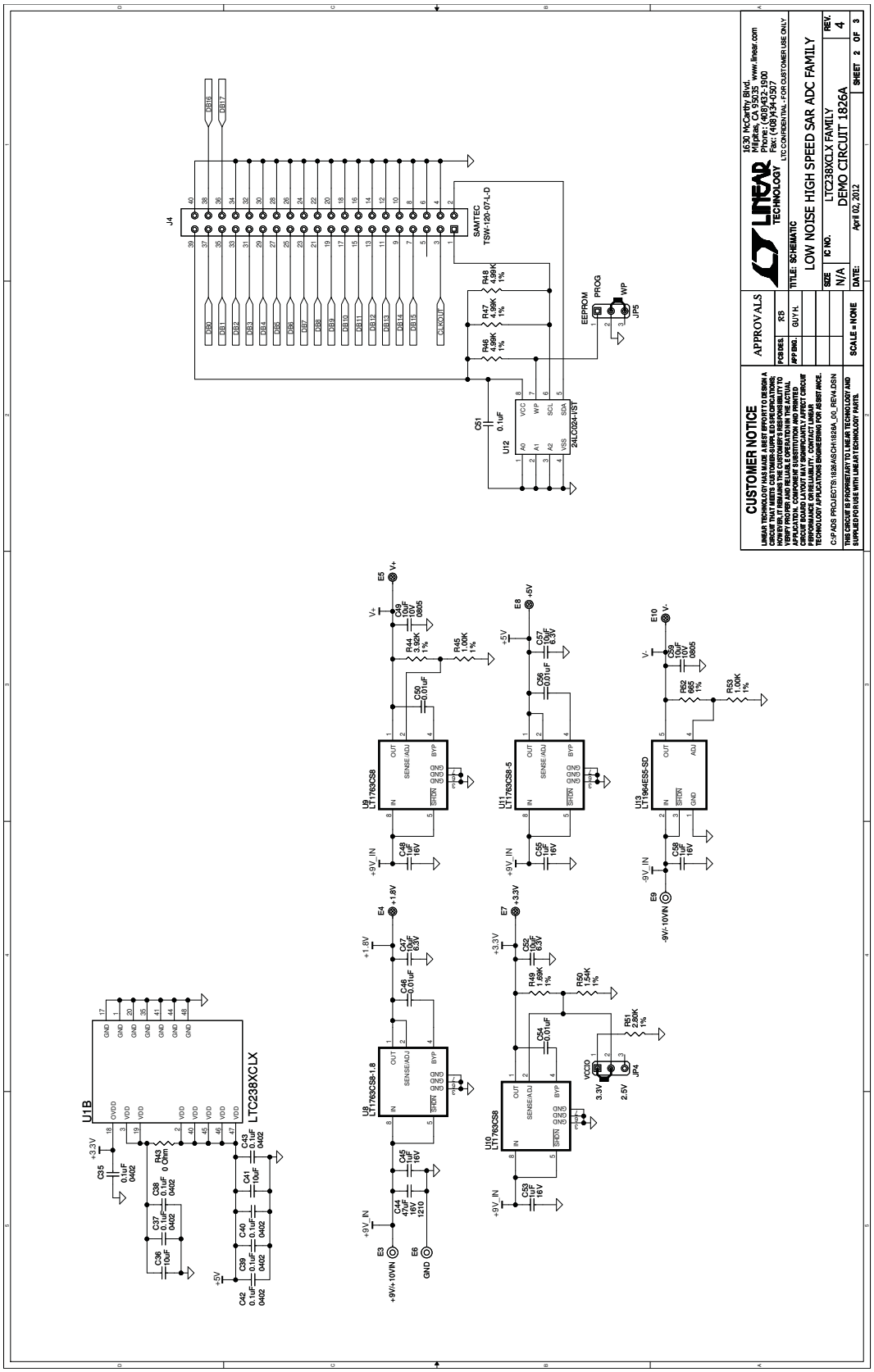

Figure 9. DC1826A Low Noise, High Speed SAR ADC Family

SCHEMATIC DIAGRAMS

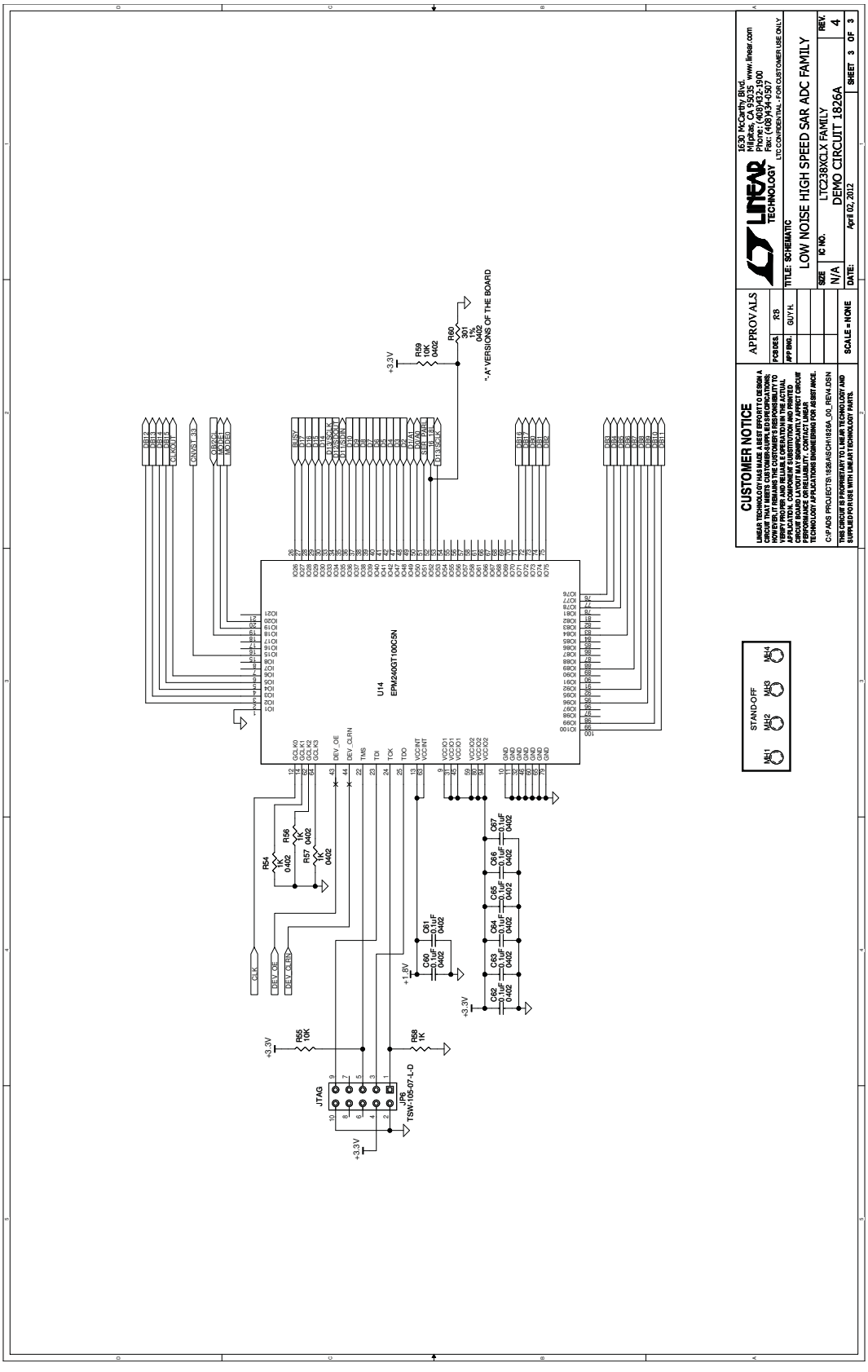

Figure 10. DC1826A Low Noise, High Speed SAR ADC Family

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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