

**NPN Silicon Digital Transistor**

- Built in bias resistor ( $R_1 = 1\text{ k}\Omega$ ,  $R_2 = 1\text{ k}\Omega$ )
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101



Type	Marking	Pin Configuration			Package
		1=B	2=E	3=C	
BCR521	XVs	1=B	2=E	3=C	SOT23

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Collector-emitter voltage	$V_{CEO}$	50	V
Collector-base voltage	$V_{CBO}$	50	
Input forward voltage	$V_{i(fwd)}$	12	
Input reverse voltage	$V_{i(rev)}$	10	
Collector current	$I_C$	500	mA
Total power dissipation- $T_S \leq 79\text{ }^\circ\text{C}$	$P_{tot}$	330	mW
Junction temperature	$T_j$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-65 ... 150	

**Thermal Resistance**

Parameter	Symbol	Value	Unit
Junction - soldering point <sup>1)</sup>	$R_{thJS}$	$\leq 215$	K/W

<sup>1)</sup>For calculation of  $R_{thJA}$  please refer to Application Note AN077 (Thermal Resistance Calculation)

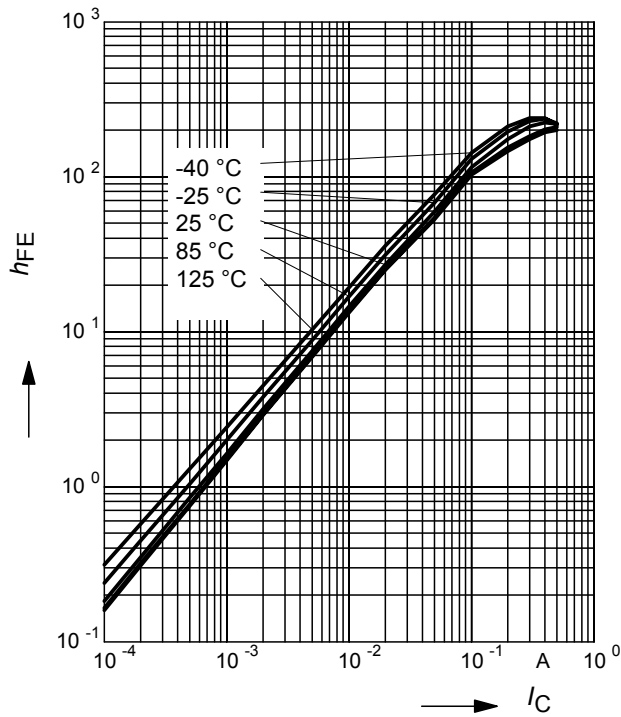
**Electrical Characteristics** at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>DC Characteristics</b>					
Collector-emitter breakdown voltage $I_C = 100 \mu\text{A}, I_B = 0$	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10 \mu\text{A}, I_E = 0$	$V_{(BR)CBO}$	50	-	-	
Collector-base cutoff current $V_{CB} = 50 \text{ V}, I_E = 0$	$I_{CBO}$	-	-	100	nA
Emitter-base cutoff current $V_{EB} = 10 \text{ V}, I_C = 0$	$I_{EBO}$	-	-	7.5	mA
DC current gain- $I_C = 50 \text{ mA}, V_{CE} = 5 \text{ V}$	$h_{FE}$	20	-	-	-
Collector-emitter saturation voltage <sup>1)</sup> $I_C = 50 \text{ mA}, I_B = 2.5 \text{ mA}$	$V_{CEsat}$	-	-	0.3	V
Input off voltage $I_C = 100 \mu\text{A}, V_{CE} = 5 \text{ V}$	$V_{i(off)}$	0.6	-	1.5	
Input on voltage $I_C = 10 \text{ mA}, V_{CE} = 0.3 \text{ V}$	$V_{i(on)}$	1	-	1.8	
Input resistor	$R_1$	0.7	1	1.3	k $\Omega$
Resistor ratio	$R_1/R_2$	0.9	1	1.1	-
<b>AC Characteristics</b>					
Transition frequency $I_C = 50 \text{ mA}, V_{CE} = 5 \text{ V}, f = 100 \text{ MHz}$	$f_T$	-	100	-	MHz

<sup>1</sup>Pulse test:  $t < 300 \mu\text{s}$ ;  $D < 2\%$

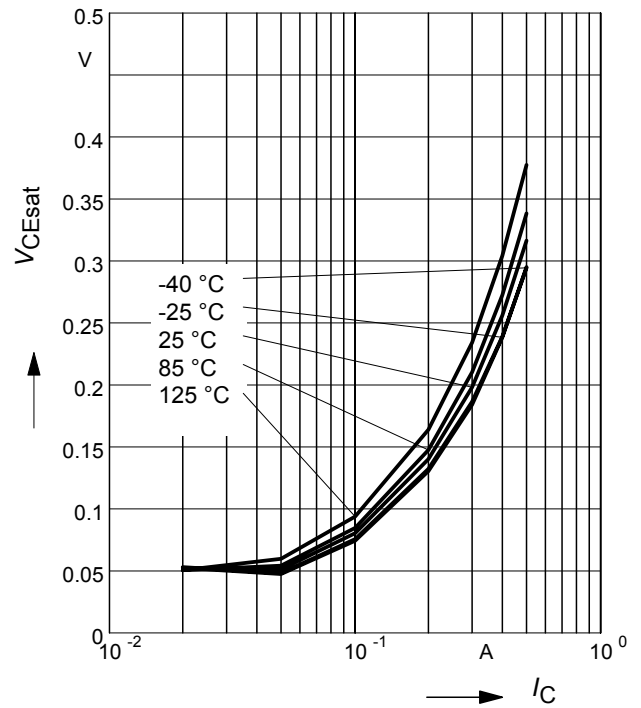
**DC current gain  $h_{FE} = f(I_C)$**

$V_{CE} = 5\text{ V}$  (common emitter configuration)



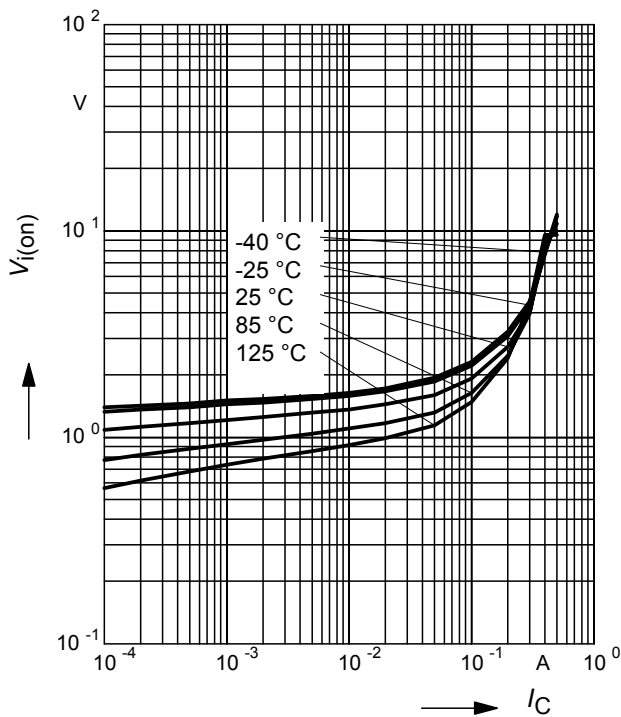
**Collector-emitter saturation voltage**

$V_{CEsat} = f(I_C), I_C/I_B = 20$



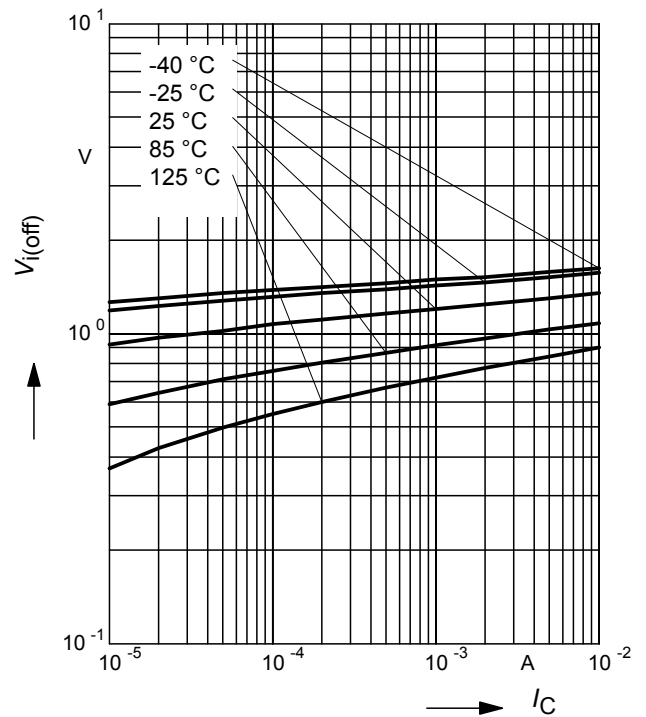
**Input on Voltage  $V_{i(on)} = f(I_C)$**

$V_{CE} = 0.3\text{ V}$  (common emitter configuration)



**Input off voltage  $V_{i(off)} = f(I_C)$**

$V_{CE} = 5\text{ V}$  (common emitter configuration)



**Total power dissipation  $P_{tot} = f(T_S)$**



**Permissible Pulse Load  $R_{thJS} = f(t_p)$**



**Permissible Pulse Load**

$P_{totmax}/P_{totDC} = f(t_p)$



Package Outline



1) Lead width can be 0.6 max. in dambar area

Foot Print



Marking Layout (Example)



Standard Packing

Reel  $\varnothing$ 180 mm = 3.000 Pieces/Reel  
 Reel  $\varnothing$ 330 mm = 10.000 Pieces/Reel



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