
PIC16F872 Rev. A2 Silicon Errata Sheet

The PIC16F872 Rev. A2 parts you have received conform functionally to the Device Data Sheet (DS30221A), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16F872 silicon.

1. Module: Electrical Specifications

The supply voltage specification has not yet met the design target (data sheet specification). The specification for these devices is shown in Table 1.

2. Programming Issues

Problems may be experienced when programming devices with date codes earlier than and including 0034NNN. These devices are shipped with Low Voltage In-Circuit Serial Programming™ (ICSP) (LVP) enabled. In this mode, the I/O pin, RB3, is used to place the device in Programming mode. Most programmers will leave this pin floating, which may cause the device to enter Programming mode before MCLR has been released from ground. This sequence of events prevents the device from entering Programming mode properly.

Work around

Connect a 10 kΩ resistor from pin RB3 to ground. This resistor can be placed in the programming socket when the device is programmed in a programmer.

When programming, using ICSP with the device mounted on the target board, pin RB3 must be pulled or driven low during programming.

If Low Voltage ICSP Programming is not required in the application, it should be disabled. All future programming cycles will not require pin RB3 to be pulled, or driven low after LVP is disabled.

3. Module: Timer1

When Timer1 is running in Asynchronous mode and then disabled, data in the Timer1 register (TMR1) may become corrupted. Corruption occurs when the timer enable is turned off at the same instant that a ripple carry occurs in the timer module.

This issue only occurs in asynchronous operation. In synchronous operation, the relevant signals are latched with the CPU clock and the problem condition does not arise.

Work around

When Timer1 is configured to operate as an asynchronous counter, care must be taken that there is no incoming pulse while the module is being turned off. If an incoming pulse arrives while Timer1 is being turned off, the value of register TMR1 may become corrupted.

If an application requires that Timer1 be turned off, and if it is possible that Timer1 may receive an incoming pulse while being turned off, synchronize the external clock first by clearing the T1SYNC bit of register T1CON (T1CON<2>). Please note, however, that this may cause Timer1 to miss up to one count.

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

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Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30221A), the following clarifications and corrections should be noted.

1. The supply voltage specification (parameter D001) has changed. The new value is shown in Table 1.

TABLE 1: DC SPECIFICATION CHANGES FROM DATA SHEET

Param. No.	Symbol	Characteristic	Tested Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D001	VDD	Supply Voltage	2.2	—	5.5	2.0	—	5.5	V

2. Configuration Word: Code Protection

The function of the Code Protect bits has changed since engineering samples were provided. Code protection now functions to protect all, or none of the FLASH program memory. Partial program memory code protection is no longer supported in production marked devices. Current code protection support is shown in Table 2.

TABLE 2: CONFIGURATION WORD CHANGES FROM DATA SHEET

Bits Affected	Function	Bit State CP<1:0>	FLASH Program Memory Range Protected		
			Data Sheet DS30221A	Engineering Samples Marked "ES"	Production Marked Devices
CP<1:0>	Code Protection	11	Code Protection Off	Code Protection Off	Code Protection Off
		10	0000h to 06FFh	07F0h to 07FFh	Not Supported
		01	0000h to 03FFh	0400h to 07FFh	Not Supported
		00	0000h to 07FFh	0000h to 07FFh	0000h to 07FFh

REVISION HISTORY

Rev A Document (6/2000)

Original errata document.

Issues 1 (Electrical Specifications) and 2 (Programming Issues), page 1.

Clarification of supply voltage (page 2).

Correction of configuration word and code protection (page 2).

Rev B Document (2/01)

Issue 3 (Timer1), page 1.

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NOTES:

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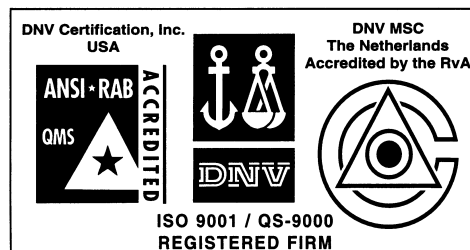
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