Errata Note

SX1272/73 – 860 to 1020 MHz
Low Power Long Range Transceiver

Revision 1 - July 2013

Table of Contents

1 Chip Identification

SX1272/73 is Production Released, with silicon Version V2b, identified as follows:

***RegVersion* at address 0x42 returns value 0x22**

This note describes the behavior of silicon Version V2b only.

Should you have any questions regarding the content of this document, or any other questions, please contact your Semtech sales representative.

Note:
Previous silicon revisions (V1a and V2a) are engineering samples which do not offer full functionality. They should not be used in a production device.

2 LoRa Modem

2.1 Frequency Offset Tolerance with 500 kHz Bandwidth

Description
With LoRa bandwidth set to 500 kHz, and with the largest spreading factors (SF=10,11,12), the tolerance to frequency offset is limited to +/-60 kHz

Workaround
No workaround identified.

2.2 Receiver Spurious Reception

Description
The SX1272/73 receiver shows spurious reception at a specific frequency offset. This may happen if a very high level LoRa signal is received at a specific offset, with the same bandwidth and spreading characteristic as the current modem settings:

Table 1: Default Spurious Rx Response

	LoRa BW Setting		
	125 kHz	250 kHz	500 kHz
Offset of Spurious Response	+/-1MHz	+/-2MHz	No response
Approximate max. level causing spurious reception (LoRa signal with same BW/SF)	-60dBm		

Workaround
The phenomenon can be mitigated by ~25dB by setting bit 7 at address 0x31 to 0.
This bit is defaulted to 1 at POR or after a Manual Reset sequence, and should be set back to 0 after any of these events occur (during the radio initialization). The following performance is resulting:

Table 2: Optimized Rx Spurious Response

	LoRa BW Setting		
	125 kHz	250 kHz	500 kHz
Offset of Spurious Response	+/-1 MHz	+/-2 MHz	No response
Approximate max. level causing spurious reception (LoRa signal with same BW/SF)	-35dBm		

2.3 Valid Packet Counter Offset

Description

The valid packet counter (used for debug, and counting only packets whose CRC is correct) presents the following issue:

- In Rx Single mode, it does not increment
- In Rx Continuous mode, it does not count the first valid packet received

Workaround

- In Rx Single mode, do not use this counter, but instead increment a counter variable if *PayloadCrcError=0* on a *RxDone* interrupt.
- In Rx Continuous mode, the same method can apply.

3 FSK Modem

3.1 PayloadReady Set for 31.25ns if FIFO is Empty

Description
When receiving in Packet mode with the SX1272/73, the microcontroller can be instructed to service the FIFO and read the bytes it contains before the *PayloadReady* flag is set, thanks to the *FifoLevel* gauge. On the SX1272/73, the duration of *PayloadReady* is very short (31.25ns) if the FIFO is already emptied at packet end, when this interrupt fires.

This situation can happen if *FifoThreshold* and the corresponding *FifoLevel* interrupts are used to monitor the FIFO content and offload it on-the-go, *FifoThreshold* being equal to the number of bytes stored in the FIFO.

Workaround
When *FifoLevel* interrupt is used to offload the FIFO, the microcontroller should monitor both PayloadReady and *FifoLevel* interrupts, and read only (*FifoThrehold*-1) bytes off the FIFO when *FifoLevel* fires.

3.2 Erroneous IBM Data Whitening/De-Whitening

Description
On the SX1272/73, the implementation of the IBM-compatible whitening/de-whitening algorithm is erroneous, which makes it incompatible with the standard implementation.

Conditions:
- ✓ *CrcWhiteningType* = 1
- ✓ *DcFree* = 10

Workaround
The workaround is to use “unlimited Length Packet Format”, and process whitening/de-whitening in the host microcontroller. Semtech is providing software implementations of this algorithm. Please contact your Semtech representative for assistance.

4 Revision History

Revision	Date	Silicon Revision	Description/Changes
1	July 2013	V2b	First FINAL Revision

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