dsPIC33FJ16GP101/102 and dsPIC33FJ16MC101/102

dsPIC33FJ16GP101/102 and dsPIC33FJ16MC101/102 Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ16GP101/102 and dsPIC33FJ16MC101/102 family devices that you have received conform functionally to the current Device Data Sheet (DS70652**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ16GP101/102 and dsPIC33FJ16MC101/102 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various dsPIC33FJ16GP101/102 and dsPIC33FJ16MC101/102 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A1
dsPIC33FJ16GP101	0x0200	0x3001
dsPIC33FJ16GP102	0x0201	
dsPIC33FJ16MC101	0x0202	
dsPIC33FJ16MC102	0x0203	

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33F Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70659) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1] A1
SPI	Frame Sync Pulse	1.	Frame sync pulse is not generated in Master mode when FRMPOL = 0.	X
SPI	Frame Sync Pulse	2.	When in SPI Slave mode, with the frame sync pulse set as an input, FRMDLY must be set to '0'.	X
UART	TX Interrupt	3.	A TX Interrupt may occur before the data transmission is complete.	X
UART	UARTEN	4.	The transmitter write pointer does not get cleared when the UART is disabled (UARTEN = 0), it requires TXEN to be set in order to clear the write pointer.	X
CPU	`div.sd` Instruction	5.	When using the `div.sd` instruction, the overflow bit is not getting set when an overflow occurs.	X
CPU	Interrupt Disable	6.	When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: SPI

When using the frame sync pulse output feature (FRMEN bit (SPIxCON2<15>) = 1) in Master Mode (SPIFSD bit (SPIxCON2<14>) = 0), the frame sync pulse is not being generated with an active low pulse (FRMPOL bit (SPIxCON2<13>) = 0).

Work around

The Slave Select pin is used as the frame sync pulse when the frame sync pulse output feature is used. Mapping the $\overline{SSx}$ input function and output function to the same pad using the PPS feature resolves this issue.

The code in Example 1 assigns SPI1 Slave Select input and SPI1 Slave Select output to RP15.

EXAMPLE 1:

```
/* Assign SPI1 Slave Select Input to RP15 */
RPINR21bits.SS1R  = 15;

/* Assign peripheral output function SPI1
   to RP15 */
RPOR7bits.RP15R = 0b01001;
```

Affected Silicon Revisions

A1							
X							

2. Module: SPI

When in SPI Slave mode (MSTEN bit (SPIxCON1<5>) = 0) and using the frame sync pulse output feature (FRMEN bit (SPIxCON2<15>) = 1) in Slave Mode (SPIFSD bit (SPIxCON2<14>) = 0), the Frame Sync Pulse Edge Select bit must be set to '0' (FRMDLY bit (SPIxCON2 <1>) = 0)

Work around

There is no workaround. The Frame Sync Pulse Edge Select bit cannot be set to produce a Frame sync pulse that coincides with the first bit clock.

Affected Silicon Revisions

A1							
X							

3. Module: UART

When using UTXISEL = 01 (Interrupt when last character is shifted out of the Transmit Shift Register), and the final character is being shifted out through the Transmit Shift Register, the TX interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occurs only when all transmit operations are complete, after which the following work around can be implemented:

Hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the transmit shift register empty bit, as shown in Example 2.

EXAMPLE 2:

```
// in UART1 initialization code
...
// Set to generate TX interrupt when all
// transmit operations are complete.
U1STAbits.UTXISEL0  = 1;
U1STAbits.UTXISEL1  = 0;
...

U1TXInterrupt(void)
{
    // wait for the transmit buffer to be
    // empty and then process interrupt.
    while(U1STAbits.TRMT==0);
    ...
```

Affected Silicon Revisions

A1							
X							

4. Module: UART

The transmitter write pointer does not get cleared when the UART module is disabled (UARTEN = 0), and it requires the TXEN bit to be set in order to clear the write pointer.

Work around

Do not load data into the TX FIFO (register) before setting the TXEN bit.

Affected Silicon Revisions

A1							
X							

5. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A1							
X							

6. Module: CPU

When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.

Work around

Avoid updating the DISICNT register manually. Instead, use the `DISI #n` instruction with the required value for 'n'.

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70652**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None to report at this time.

APPENDIX A: REVISION HISTORY

Rev A Document (6/2011)

Initial release of this document; issued for revision A1 silicon.

Includes silicon issues 1 and 2 (SPI), 3 and 4 (UART), and 5 (CPU).

Rev B Document (12/2011)

Added silicon issue 6 (CPU).

NOTES:

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