TERIDIAN SEMICONDUCTOR CORP.

Simplifying System Integration™

73S1215F
Evaluation Board User Guide

August 17, 2009
Rev. 1.8
UG_1215F_039

Teridian Semiconductor Corp., 6440 Oak Canyon, Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.teridian.com

Table of Contents

1 Introduction 5
1.1 Evaluation Kit Contents 6
1.2 Evaluation Board Features 6
1.3 Recommended Equipment and Test Tools 6
2 Evaluation Board Basic Setup 7
2.1 Connecting the Evaluation Board with an Emulation Tool 8
2.2 Loading User Code into the Evaluation Board 9
3 Using the USB CCID Application 11
3.1 Driver and Host Demonstration Software Installation 11
3.1.1 Installation on Windows XP 11
3.1.2 Driver and Software Installation on a Linux System 12
3.2 Frequently Asked Questions 12
4 Evaluation Board Hardware Description 14
4.1 Jumpers, Switches and Modules 14
4.2 Test Points 20
4.3 Schematic 21
4.4 PCB Layouts 22
4.5 Bill of Materials 28
4.6 Schematic Information 31
4.6.1 Reset Circuit 31
4.6.2 Oscillators 31
4.6.3 LCD 32
4.6.4 USB Interface 32
4.6.5 Smart Card Interface 33
5 Ordering Information 34
6 Related Documentation 34
7 Contact Information 34
Revision History 35

Figures

Figure 1: 73S1215F Evaluation Board 5
Figure 2: 73S1215F Evaluation Board Basic Connections 7
Figure 3: 73S1215F Evaluation Board Basic Connections with ADM-51 ICE 8
Figure 4: Emulator Window Showing RESET and ERASE Buttons 10
Figure 5: Emulator Window Showing Erased Flash Memory and File Load Menu 10
Figure 6: Board Setup for the USB-CCID Application 12
Figure 7: 73S1215F Evaluation Board Jumper, Switch and Module Locations 19
Figure 8: 73S1215F Evaluation Board Electrical Schematic 21
Figure 9: 73S1215F Evaluation Board Top View (Silkscreen) 22
Figure 10: 73S1215F Evaluation Board Bottom View (Silkscreen) 23
Figure 11: 73S1215F Evaluation Board Top Signal Layer 24
Figure 12: 73S1215F Evaluation Board Middle Layer 1 – Ground Plane 25
Figure 13: 73S1215F Evaluation Board Middle Layer 2 – Supply Plane 26
Figure 14: 73S1215F Evaluation Board Bottom Signal Layer 27
Figure 15: External Components for RESET 31
Figure 16: Oscillator Circuit 31
Figure 17: LCD Connections 32
Figure 18: USB Connections 32
Figure 19: Smart Card Connections 33

Tables

Table 1: Flash Programming Interface Signals 9
Table 2: Evaluation Board Jumper, Switch and Module Description 14
Table 3: Evaluation Board Test Point Description 20
Table 4: 73S1215F Evaluation Board Bill of Materials 28

1 Introduction

The Teridian Semiconductor Corporation (TSC) 73S1215F Evaluation Board is used to demonstrate the capabilities of the 73S1215F Smart Card Controller device. It has been designed to operate either as a standalone or a development platform.

The 73S1215F Evaluation Board can be programmed to run any of the Teridian turnkey applications or a user-developed custom application. Teridian provides its USB CCID application preloaded on the board and an EMV testing application on the CD.

Applications can be downloaded through the In-Circuit-Emulator (ICE) or through the TSC Flash Programmer Model TFP2. As a development tool, the evaluation board has been designed to operate in conjunction with an ICE to develop and debug 73S1215F based embedded applications.

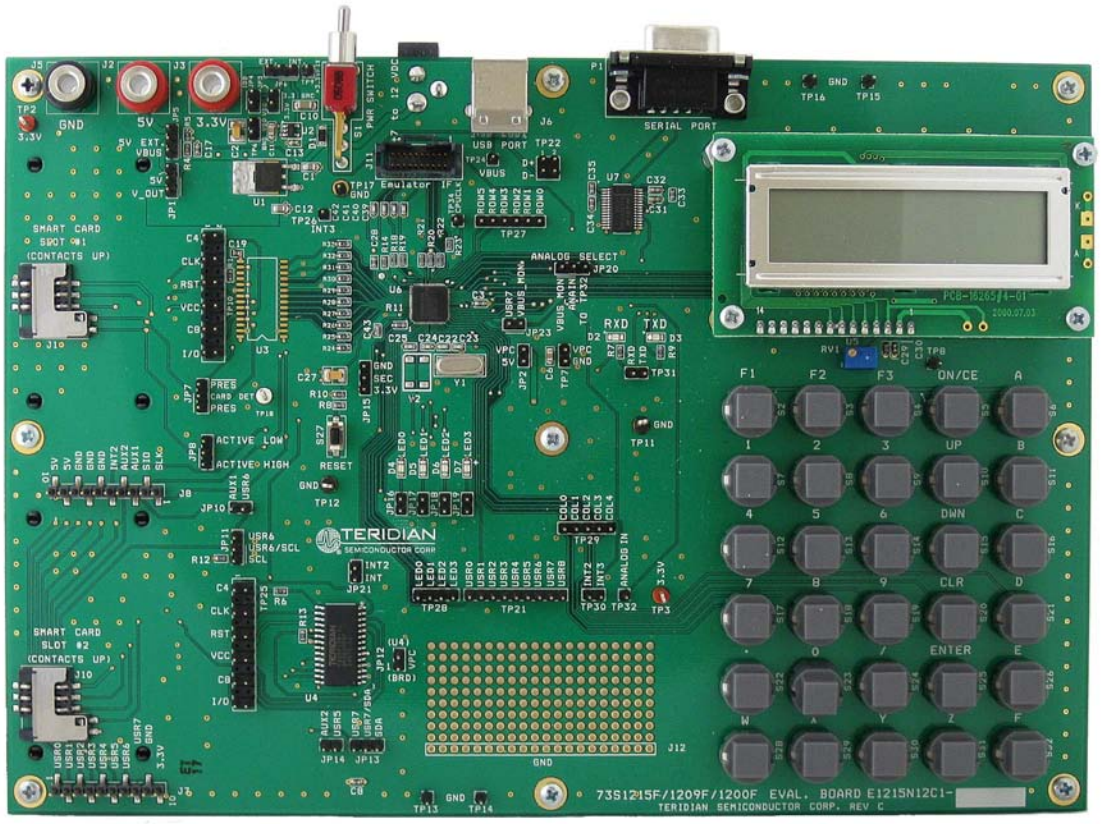

Figure 1: 73S1215F Evaluation Board

1.1 Evaluation Kit Contents

The 73S1215F Evaluation Kit contains the following:

- 73S1215F Evaluation Board: 4-layer, rectangular PWB as shown in Figure 1 (identification number E1215N12C1 Rev C), containing the 73S1215F with the preloaded turnkey program USB CCID.
- 12 VDC/1,000 mA universal wall transformer with 2.1 mm plug ID (CUI Inc. – EPAS-101W-12).
- USB cable, A-B, male/male, 2 meters (Digi-Key AE9932-ND)
- CD containing documentation (data sheet, and user guides), software API libraries, evaluation code, and utilities.

1.2 Evaluation Board Features

The 73S1215F Evaluation Board (see Figure 1) includes the following:

- USB 2.0 full speed interface
- RS-232 interface
- Dual smart card interface
- ICE/Programmer interface
- 2 line x 16 character LCD module
- 6 x 5 keypad
- Real Time Clock (RTC) capability
- 4 LEDs

1.3 Recommended Equipment and Test Tools

The following equipment and tools (not provided) are recommended for use with the 73S1215F Evaluation Kit:

- For functional evaluation: PC with Microsoft® Windows® XP or Vista®, or a workstation running Linux® equipped with an USB port.
- For software development (MPU code)
  - Signum™ ICE (In Circuit Emulator): ADM-51. Refer to http://signum.temp.veriohosting.com/Signum.htm.
  - Keil™ 8051 C Compiler Kit: CA51. Refer to http://www.keil.com/c51/ca51kit.htm and http://www.keil.com/product/sales.htm.

2 Evaluation Board Basic Setup

Figure 2 shows the basic connections of the evaluation board with the external equipment.

The power supply can come from three sources:

- A regulated lab power supply connected to the banana plugs J2, J3 and J5. In this case, the board main switch S1 has no effect.
- Any AC-DC converter block (default), able to generate a DC power supply of 7 V min / 12 V max / 400 mA. In this case, the board main switch S1 connects or disconnects the supply to the board.
- The +5 V from the USB bus when connected to a computer or hub able to support USB-powered devices. In this case, the board main switch S1 has no effect. When the board is powered from the USB bus, the application is bus-powered and the embedded application must be designed for this.

The USB VBUS specification allows the VBUS voltage to be as low as 4.4 V. This will violate the minimum VPC voltage for smart card operation which is specified as 4.75 V. As a result, this power configuration is not recommended.

The communication with an external host can be accommodated by either:

- A standard USB 2.0 Full Speed Interface or
- A standard RS-232 serial interface (TX/RX only).

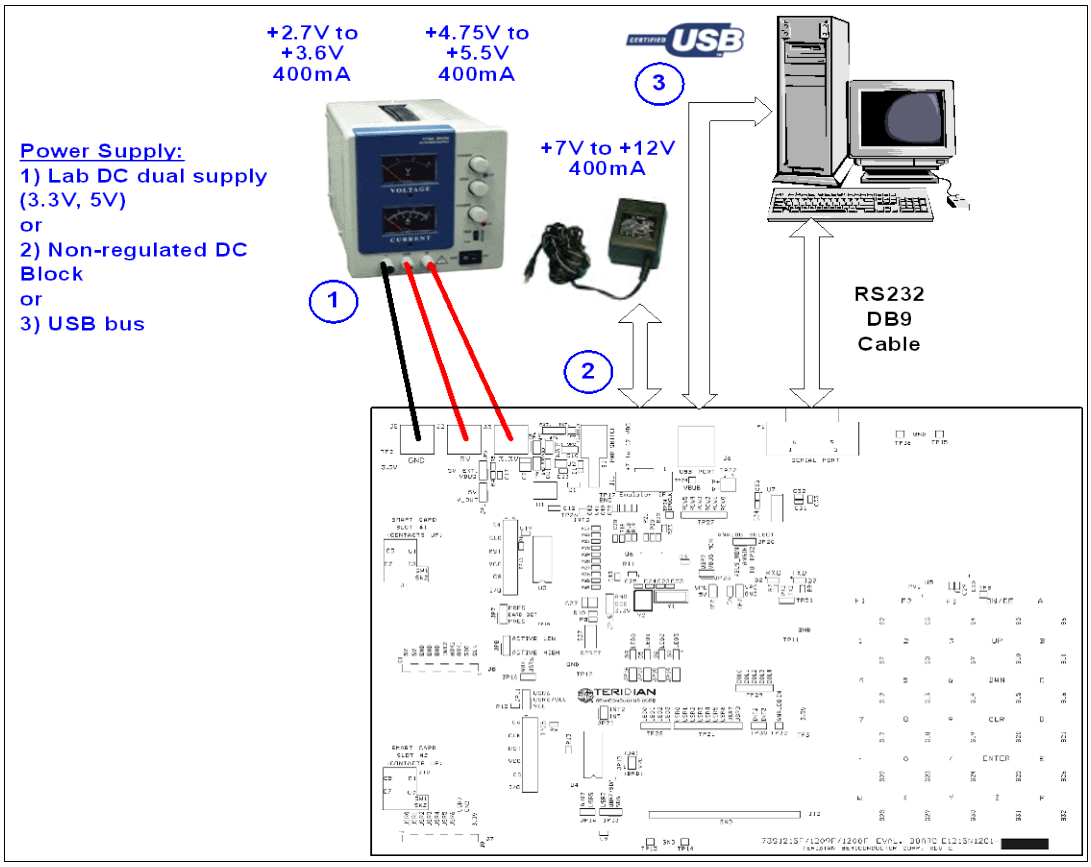

Figure 2: 73S1215F Evaluation Board Basic Connections

The board provides by default the USB CCID application. Refer to Section 3 for information on setting up and running the USB CCID application.

2.1 Connecting the Evaluation Board with an Emulation Tool

The 73S1215F Evaluation Board can operate with an In-Circuit-Emulator (ICE) from Signum Systems (model ADM-51). Figure 3 shows the connections between the ICE and the evaluation board. The Signum System pod has a ribbon cable that must be directly attached to connector J11.

Signum Systems offers different pod options depending on user needs. The standard pod allows users to perform typical emulator functions such as symbolic debugging, in-line breakpoints, memory examination and/or modification, etc. Other pod options enable code trace capability and/or complex breakpoints at an additional cost.

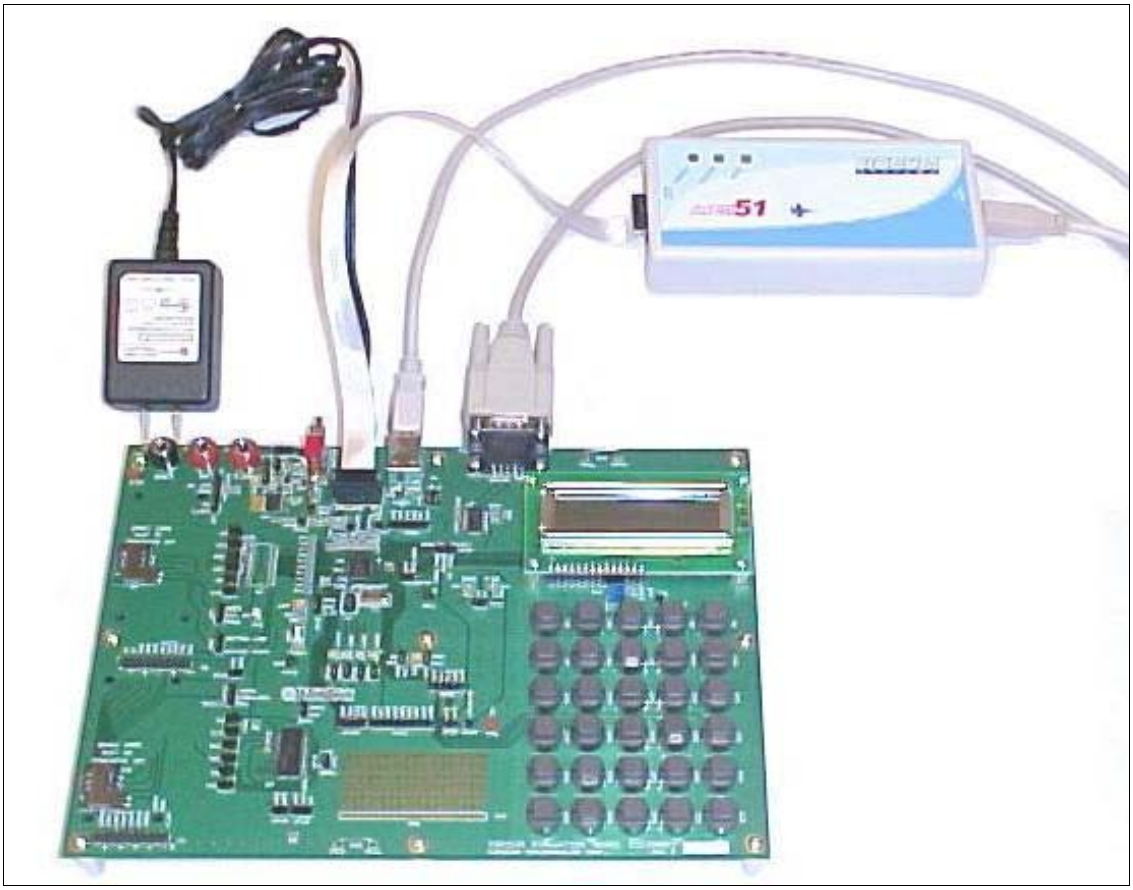

Figure 3: 73S1215F Evaluation Board Basic Connections with ADM-51 ICE

2.2 Loading User Code into the Evaluation Board

Hardware Interface for Programming

The signals listed in Table 1 are necessary for communication between the TFP2 or ICE and the 73S1215F.

Table 1: Flash Programming Interface Signals

Signal	Direction	Function
E_TCLK	Output from 73S1215F	Data clock
E_RXTX	Bi-directional	Data input/output
E_RST[1]	Bi-directional	Flash Downloader Reset (active low)
[1] The E_RST signal should only be driven by the TFP2 when enabling these interface signals. The TFP2 must release E_RST at all other times.		

The signals in Table 1, along with 3.3 V and GND, are available on the emulator header J11. Production modules may be equipped with much simpler programming connectors, e.g. a 5x1 header.

Programming of the flash memory requires either the Signum Systems ADM51 in-circuit emulator or the TSC Flash Programmer Model TFP2 provided by Teridian.

Loading Code with the In-Circuit Emulator

If firmware exists in the 73S1215F flash memory, the memory must be erased before loading a new file into memory. In order to erase the flash memory, the RESET button in the emulator software must be clicked followed by the ERASE button (see Figure 4).

Once the flash memory is erased, a new file can be loaded using the Load command in the File menu. The dialog box shown in Figure 5 makes it possible to select the file to be loaded by clicking the Browse button. Once the file is selected, pressing the OK button loads the file into the flash memory of the IC.

At this point, the emulator probe (cable) can be removed. Once the 73S1215F device is reset using the reset button on the evaluation board, the new code starts executing.

Loading Code with the TSC Flash Programmer Model TFP2

Follow the instructions given in the *TSC Flash Programmer Model TFP2 User's Manual*.

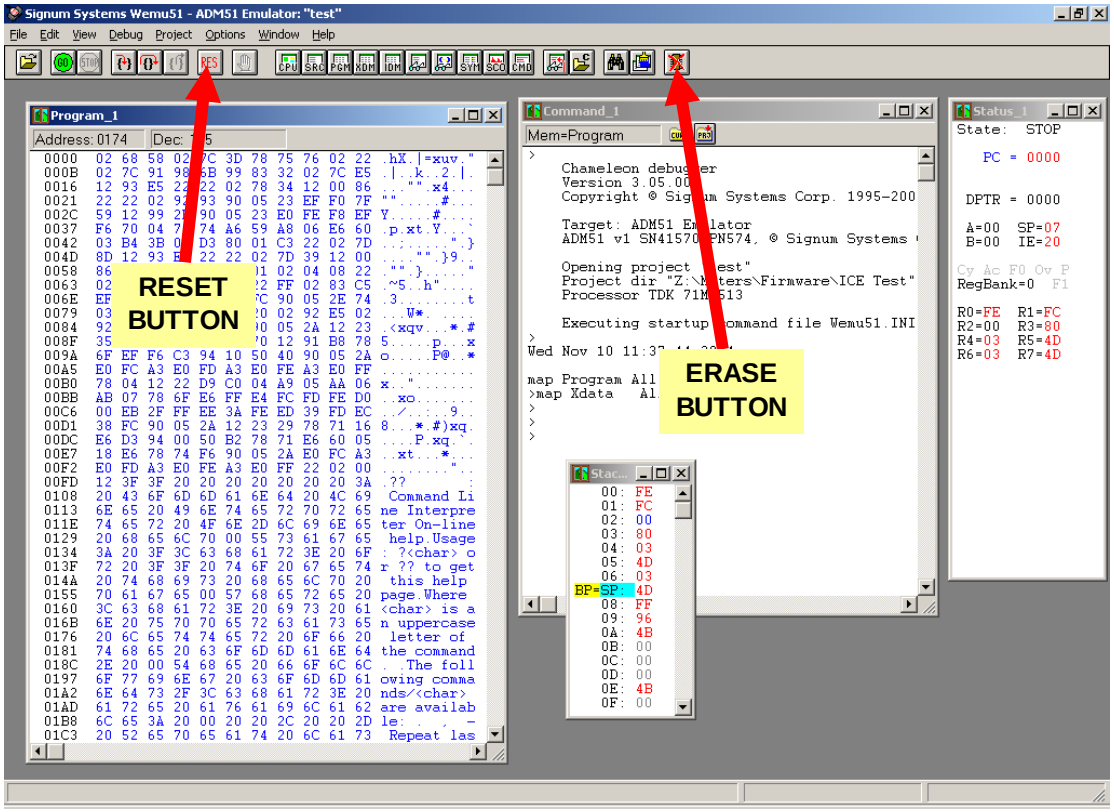

Figure 4: Emulator Window Showing RESET and ERASE Buttons

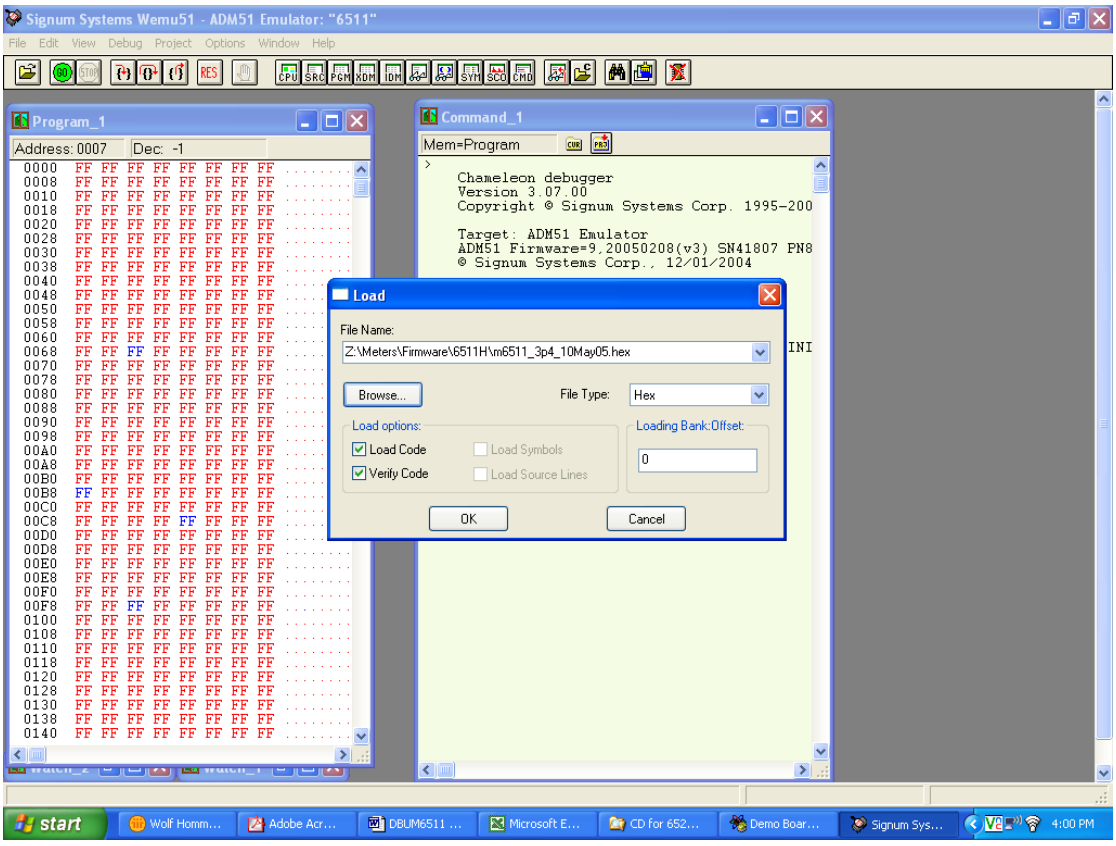

Figure 5: Emulator Window Showing Erased Flash Memory and File Load Menu

3 Using the USB CCID Application

The USB CCID firmware is pre-installed on the 73S1215F Evaluation Board. To operate correctly, it requires a PC with the appropriate driver to be connected through its USB port. When powered-up, the board is able to run the CCID-USB demonstration host application which allows:

- Smart card activation and deactivation, in ISO or EMV mode.
- Smart card APDU commands to be exchanged with the smart card inserted in the board.
- Starting a test sequence in order to test and evaluate the board performance against an EMV test environment.

3.1 Driver and Host Demonstration Software Installation

3.1.1 Installation on Windows XP

Two drivers are available for use with Windows XP:

- The standard Microsoft Windows XP driver and
- The Teridian provided driver that adds additional features beyond the capabilities of the Microsoft driver.

See the *73S1215F, 73S1217F CCID Application Note* further details on the differences between the two drivers.

When using the 73S1215F transparent reader – dual slot with keypad and LCD evaluation board, the Microsoft provided driver should not be used as this driver does not support the second slot nor the LCD display and keypad.

The Microsoft CCID driver included on the CD is used by Teridian for testing. Check with Microsoft for the latest driver upgrades.

Follow these steps to install the software on a PC running Windows XP:

- Extract “12xxF CCID+DFU V***y.yy*** Release.zip” (where ***y.yy*** is the latest version of the firmware release).
  - Create an install directory. For example: “C:\TSC\”.
  - Unzip “12xxF CCID+DFU V***y.yy*** Release.zip” to the just created folder. All applications and documentation needed to run the board with a Windows PC will be loaded to this folder.
- Plug the supplied adapter into the 12V DC jack and a wall outlet.
- Flip the ON/OFF switch to ON.
- Connect the USB cable between the host system and the 73S1215F Evaluation Board.
- The host system should recognize the board and start the Add New Hardware Installation Wizard. When the wizard prompts, select the Teridian provided driver file.
  - To use the Teridian supplied driver, select the ccidtsc-xp.inf file located in the “C:\TSC\12xxF CCID+DFU V***y.yy*** Release\USB-CCID Firmware\CCID USB\CCID+DFU USB Drivers\XP 32 - CCID” subdirectory. The ccistsc-xp.inf and ccidtsc-xp.sys files must be in the same directory on the host.
- Follow the prompts until the process is completed.
- Run “CCID-DFU_USB_v***y.yy***.exe” (located in the path - C:\TSC\12xxF CCID+DFU C:\TSC\12xxF CCID+DFU V2.00 Release\Host Applications\Windows App\Bin\Release Release\Host Applications\Windows App\Bin\Release) on the host system to execute the host demonstration application.

At this point the application window should appear. For additional information regarding the use of the Teridian Host application, refer to the *73S12xxF USB-CCID Host GUI Users Guide* (UG_12xxF_037).

To use the Windows standard driver, select the usbccid.inf file located in the "C:\TSC\12xxF CCID+DFU V***y.yy*** Release\USB-CCID Firmware\CCID USB\CCID+DFU USB Drivers\MS Generic" subdirectory. The usccid.inf and usbccid.sys files must be in the same directory on the host.

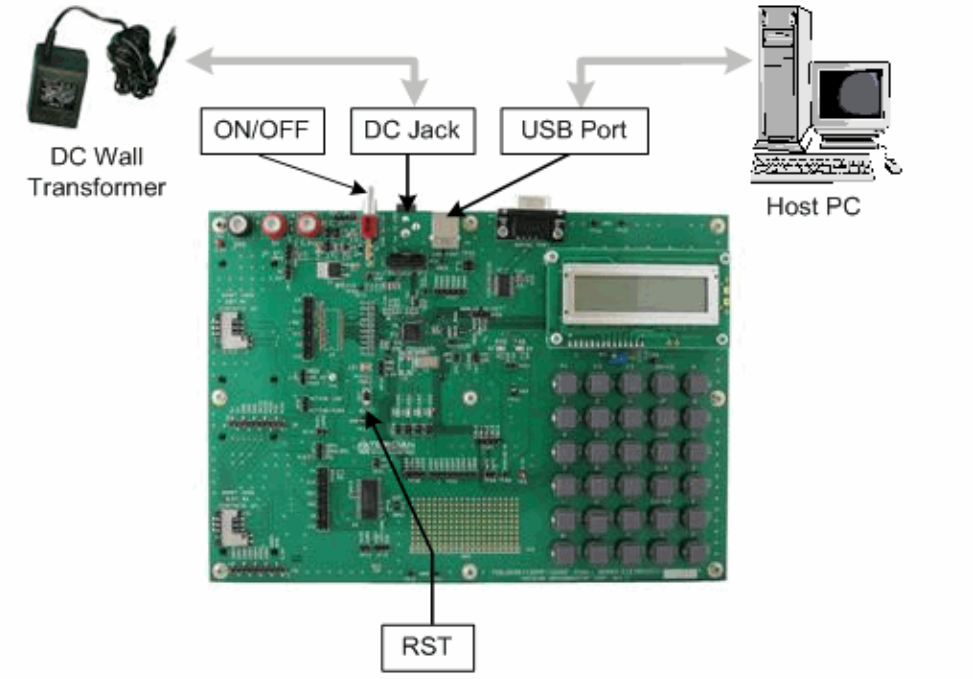

Figure 6: Board Setup for the USB-CCID Application

3.1.2 Driver and Software Installation on a Linux System

Teridian has tested this board with CCID driver v1.3.2 and PCSC-Lite v.1.4.4 (middleware) on two distributions of Linux: Slackware® 6 with kernel 2.4.16, and Fedora® 7 with kernel 2.6.23. Please refer to the *73S1215F, 73S1217F CCID USB Linux Driver Installation Guide* (UG_12xxF_041) for details on installation and usage on Linux.

3.2 Frequently Asked Questions

Windows

Q: The PC/SC application starts but it shows a "No Reader Found" message.

A: Follow these steps to make sure:

1. The board has powered up properly (USB is securely connected and there is power applied to the board).
2. Control Panel – System – Hardware – Device Manager – Smart Card Readers shows: "Teridian Semiconductors USB CCID Smart Card Reader..." And there is no yellow "!" or red "X".
3. Smart Card Service has started by going to "Control Panel – Administrative Tools – Services – Smart Card". Look under the "status" column and if it shows "stopped", hit the restart or start button to start it.
4. If all of the above look ok, hit the refresh button on the CCIDUSB.exe application.

Q: There is a yellow "!" on the Teridian driver shown on the Device Manager menu.

A: This usually means the driver did not complete the driver enumeration process. Push the reset button on the evaluation board a few times. If the board is connected to the host via a USB HUB, remove the HUB and try connecting the board directly to the PC USB port to make sure the driver and the board can enumerate with the USB host. If the problem persists, check the driver on the PC to make sure it is at least version 6.0.0.2. Contact your Teridian Sales Representative for the latest version of the driver. Sometimes, rebooting the PC Host to clear up any previous USB problem will help.

Q: There is a red "X" on the Teridian driver shown on the Device Manager menu.

A: This usually means the smart card driver has been disabled. Highlight and right click on the driver to re-enable.

Q: The Teridian Smart Reader is nowhere to be found on the Device Manager menu and there is an "unknown USB device" found where the Teridian evaluation board should be.

A: This usually means the evaluation board is properly powered up but there is no enumeration taking place. If the board is connected to a USB HUB, remove the HUB and connect the board directly to the PC USB port. Or move it to a different USB port on the system. If the problem persists and it is absolutely sure that the board is properly powered up, it is possible that there is no firmware in the part. Contact a Sales Representative for reprogramming of the Flash.

Q: The Teridian driver is loaded. What to do to replace it with the Microsoft Generic USB CCID driver?

A: Right click on the Teridian Driver in the Device Manager Menu, select "Update Driver.." Select "No, Not this time" on the next menu, "Install from a list or specific location", "Don't Search, I will choose the driver to install". If the next menu does not show the Microsoft Generic USB CCID driver, select "Have Disk" and browse to where the driver file resides (usually in the "CCID USB XPDriver" folder) and select the file. Follow through with the installation wizard.

Linux

Q: How can I see debug messages from PCSC-Lite when I run pcscd from the command line?

A: Before invoking pcscd, open the file /usr/local/pcsc/drivers/ifd-ccid.bundle/Contents/Info.plist in an editor, and set ifdLogLevel to 7. Save the change. Then run the command "pcscd –f –d" in a console. Now pcscd runs in foreground and should display many messages in the console. These messages show information about the smart card readers that have been detected, and whether or not a smart card is present in the reader. Also shown in the messages are the data exchanges between the host (Linux) and the smart card reader. The most important messages are the error messages that pcscd displays when a critical error has occurred. If fewer messages are desired, set IfdLogLevel to 3 or 1.

Q: When I run command "pcscd –f –d", I get an error message that says "file /var/run/pcscd.pub already exists. Another pcscd seems to be running".

A: Only one instance of pcscd (PCSC-Lite Daemon) should be running at any time. If you receive this error message when invoking the pcscd program, pcscd is probably running already. If your intention is to restart pcscd, first terminate the pcscd that is currently running. Run the command "ps aux | grep pcscd" to obtain the PID (Process ID) of the currently running pcscd. For example, you may see output similar to the following:

```
[root@localhost ~]# ps aux | grep pcscd
root 3380  0.1  0.0    74588   1752    pts/2     Sl+       16:06    0:02 pcscd –f –d
[root@localhost ~]#
```

The PID of the currently running pcscd in this case is 3380. Next run the command "kill 3380" to stop pcscd. Now start pcscd again by entering the command "pcscd –f –d".

Q: When I start the program pcsc_scan, I receive an error message saying "PCSC Not Running".

A: The pcsc_scan program requires the services provided by pcscd. Hence the PCSC-Lite daemon pcscd should be already running before pcsc_scan can start. Run pcscd first, and then invoke pcsc_scan.

4 Evaluation Board Hardware Description

4.1 Jumpers, Switches and Modules

Table 2 describes the 73S1215F Evaluation Board jumpers, switches and modules. The Item # in Table 2 references Figure 7. The default setting refers to setup for running USB-CCID application.

Table 2: Evaluation Board Jumper, Switch and Module Description

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
1	J2, J3, J5	No Connect	Banana plugs for external regulated power supply	Must be used to connect an external regulated power supply. These inputs are intended to allow control of the input supply voltage of the board (e.g. different than 5.0 V and 3.3 V on-board regulators). JP5 must be in position "5V EXT" and JP1 must be in position "5V "when using this 5 V power supply input. JP6 must be in position "EXT" "when using this 3.3 V power supply input.
	The evaluation board is sensitive to the polarity: One red plug is +3.3 V nominal and the other red plug is +5.0 V. The black plug is ground. The voltage supply input should be in the range +2.7 V to +3.6 V and 4.75 V to 5.5 V respectively.			
2	JP4	Inserted	VDD jumper	In normal use, a jumper must be inserted in this header, to connect the +3.3 V power supply of the board to the VDD pins of the 73S1215F. This jumper can be replaced by a μA / mA-meter to measure the actual current drawn by the 73S1215F.
3	JP3	Inserted	3.3 V jumper	In normal use, a jumper must be inserted in this header, to connect the +3.3 V power supply of the RS-232 transceiver and the 73S8010R. This jumper can be removed to minimize power consumption if these devices are not used.
4	JP6	'INT'	Jumper: power supply selection (#1)	A jumper must be inserted to select one of the following settings: • In position "EXT", the evaluation board 3.3 V is supplied from the external power supply inputs (banana plug J3). In this case, the voltage must be externally regulated. The power supply line is directly applied to the board power supply. This external power supply must not exceed 3.6 V. • In position "INT", the evaluation board is powered from the 3.3 V voltage regulator U1. The regulator can be powered either from the USB bus power supply (USB-powered application), or from an external non-regulated power supply (connector PJ1).
5	S1		Main switch	This switch turns the power On / Off to the evaluation board, when the jumper JP1 is in position "VOUT". When using a lab regulated power supply connected to the banana plugs J2 and J3, this switch has no effect.

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
6	PJ1	Connect	DC jack	Plug to connect an external DC block. Must be used in conjunction with appropriate settings of S1, JP1 and JP6 (see details above). Power supply features are: Voltage: 7 V min; 12 V max Current: 400 mA
7	J11	No Connect	In-Circuit Emulator connector	This connector must be used when using an external In-Circuit Emulator (SIGNUM 8052 ADM51 ICE). Refer to the Electrical Schematic for pin assignment.
8	J6	Connect	USB connector	Standard USB socket. Requires a standard USB 1.1 or 2.0 device cable to connect to a computer.
9	JP23	Inserted	USB interrupt jumper	Jumper allows the VBUS (after level conversion) to connect to USR7 (configured for interrupt). Remove this jumper if not needed and USR7 can be used for another purpose.
10	JP20	Not Inserted	Jumper: analog in	Jumper will select between the VBUS or analog in test point for the analog input. Using VBUS on the analog input will free up the USR7 interrupt for other uses. The analog input can be set up to use the compare to detect when the USB cable is inserted/removed.
11	P1	No Connect	DB9 RS232 female socket	This socket allows connection of an RS232 cable to a computer. Use a crossed wires (RX/TX) cable. The evaluation board has an on-board level shifter (U7) to allow direct connection to a computer. Connection of a RS232 link is required when using the pre-downloaded application.
12	D2, D3, D4, D5, D6, D7		LEDs: Serial link activity and four dedicated LED pins.	These LEDs (D2, D3) reflect the activity on the serial link (RS232 or serial), and the others are used for general purpose indicators without the need for current limiting resistors. • D2 reflects the activity on the RX line (Data going TO the 73S1215F) • D3 reflects the activity on the TX line (Data coming FROM the 73S1215F) • D4 to D7 are the LED0-LED3 output pins .
13	U5		LCD Module	On-board LCD module: • 2 lines of 16 characters, each character dot matrix is 5x7. • Includes an embedded Hitachi HD44780 LCD driver, controlled from the on-board 73S1215F USR interface.
14	RV1		Adjustable resistor to adjust LCD brightness	Can be used to adjust the brightness of the on-board LCD module.

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
15	S2 to S31		On-board keypad	5x6 keyboard directly connected to the on-board 73S1215F IC. The assignment of the keys, as silk-printed on the PCB is the one supported by the TSC Application Programming Interface.
16	–		Board reference and serial number	Should be mentioned in any communication with TSC Application Engineers when requesting support.
17	JP2	Inserted	Jumper VPC	In normal use, a jumper must be inserted in this header to connect the +5.0 V power supply of the board to the VPC pins of the 73S1215F. This jumper can be replaced by a μA / mA-meter to measure the actual current drawn by the 73S1215F.
18	–		Breadboard area	This breadboard area allows engineers to add their own circuitry / connection of peripherals, when prototyping and developing a 73S1215F based application. User I/Os, GPIOs, interrupt pins and power supply pins are located close to this area to allow easy connection.
19	JP16, JP17, JP18, JP19	Inserted	Jumper: LED pins	In normal use, a jumper must be inserted in this header, to connect the LEDs to the LED pins of the 73S1215F. This jumper can be replaced by a μA / mA-meter to measure the actual current drawn by the LED outputs of the 73S1215F.
20	JP12	Inserted	Jumper: 73S8010R VPC connect	Insertion of the jumper will provide 5.0 V to the 73S8010R VPC pin. If the 73S8010R is not used, the jumper can be removed.
21	JP13	Not Inserted	Jumper: USR7/SDA select	This jumper selects which signal is connected to the daughter board connector pin USR7: • In position “USR7”, the 73S1215F USR7 signal is connected to the daughter card pin USR7. • In position “SDA”, the I2C SDA signal is connected to the daughter card pin USR7. This allows the SDA line to connect to an SDA pin on a 73S8010R daughter card.
22	JP14	Not Inserted	Jumper: USR5/AUX2 select	This jumper allows the on board 73S8010 AUX2 pin to be connected to USR5 if needed. If not needed the jumper should be removed.
23	U4		On board 73S8010R	The board contains a built-in 73S8010R that is connected to the external smart card interface of the 73S1215F. If not used, this device can be disconnected from the 73S1215F by removing jumpers JP12 and JP21.
24	JP21	Inserted	Jumper: 73S8010R interrupt	This jumper will allow the on-board 73S8010 interrupt output to connect to INT2 on the 73S1215F. Remove this jumper if the on-board 73S8010 is not used.

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
25	J7,J8	Not Inserted	Optional 73S80xxX Daughter Board interface	When developing applications that require more than 2 smart card interfaces, an optional daughter board can be populated to use the 73S1215F external smart card interface (lines SCIO and SCK), in conjunction with the USR(0:7) port and the INT2 interrupt input of the 73S1215F). Refer to the Electrical Schematic for pin assignment.
26	J9, J10		SIM / SAM and Smart Card connectors – external interface (#2)	Allows the evaluation board to communicate with a smart card using either the standard (credit card size) or SIM/SAM format. This slot is connected to the 73S1215F external card interface # 2. Note that J10 is wired is parallel to the smart card connector J9 (underneath the PCB). Both connectors cannot be populated at the same time.
27	JP11	Not Inserted	Jumper: USR6/SCL select	This jumper selects which signal is connected to the daughter board connector pin USR6: • In position “USR6”, the 73S1215F USR6 signal is connected to the daughter card pin USR6. • In position “SCL”, the I2C SCL signal is connected to the daughter card pin USR6. This allows the SCL line to connect to an SCL pin on a 73S8010R daughter card.
28	JP10	Not Inserted	Jumper: USR6/AUX1 select	This jumper allows the on board 73S8010 AUX1 pin to be connected to USR6 if needed. If not needed the jumper should be removed.
29	JP8	‘Active High’	Jumper: Selection of the polarity of the card detection switches of internal smart card connector	On-board smart card connectors and SIM/SAM connectors are equipped with card presence switches, normally open when no card is inserted. When the switches are closed (card inserted), the polarity must be selected by a jumper on JP8: • In position “ACTIVE HIGH”, the card detection switches connect +3.3 V to the card detection inputs of the 73S1215F. • In position “ACTIVE LOW”, the card detection switches connect ground to the card detection inputs of the 73S1215F. The 73S1215F firmware can handle both polarities for card detection. Therefore, this setting is firmware dependent. The default firmware settings are JP8 = ACTIVE HIGH and JP7 = PRES.
30	S27		Reset button	Evaluation board main reset: Asserts a hardware reset to the on-board 73S1215F IC.
31	JP7	‘PRES’	Jumper: Selection of the PRES and PRESB inputs	Selects the card detect input PRES or PRESB. PRES is the active high input and PRESB is the active low input. See item 29 for more detail.

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
32	JP15	'GND'	Jumper: security fuse control	This jumper should be removed at all times. Connecting the jumper will allow the security fuses to be blown under firmware control. Refer to the *73S1215F Data Sheet* for further information about the security fuse.
33	J1, J4		SIM / SAM and Smart Card connectors – internal interface (#1)	Allows the evaluation board to communicate with a smart card using either the standard (credit card size) or SIM/SAM format: This slot is connected to the 73S1215F built-in card interface # 1. J1 is wired in parallel to the smart card connector J4 (underneath the PCB). Both connectors cannot be used at the same time.
34	R24 - R33		Jumper resistors	These jumper resistors will configure the board for a 73S1215F device. U3 should not be populated.
35	U3		73S8009	See item 34.
36	JP1	'VOUT'	Jumper: power supply selection (#2)	This jumper selects the 5.0 V power supply. It selects either the power supply connected to the on-board 5.0 V regulator (U1) or the 5.0 V from the external regulated supply/USB VBUS (see item 39): • In position "VOUT", the evaluation board 5.0 V is powered from the on-board +5 V regulator. • In position "5V", the evaluation board, is powered from the voltage applied on the plug J2.
37	JP5	'VBUS'	Jumper: power supply selection (#3)	This jumper selects the 5.0V power supply. It selects either the power supply connected to plug J2 or the USB VBUS 5.0V: • In position "VBUS", the evaluation board +5 V going to JP1 is connected to the +5 V coming from the USB. • In position "5VEXT", the evaluation board is powered from the voltage applied on the plug J2.

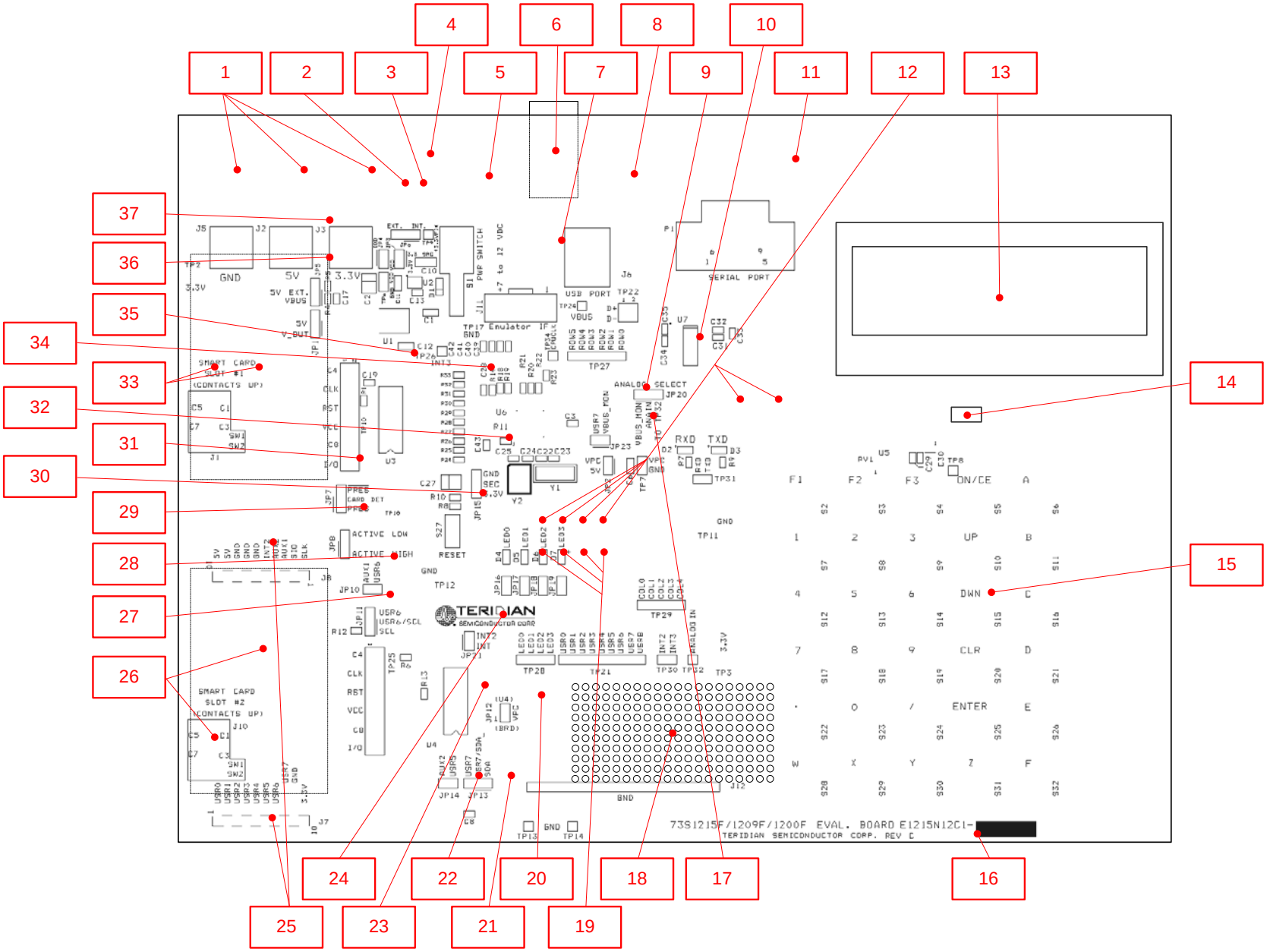

Figure 7: 73S1215F Evaluation Board Jumper, Switch and Module Locations

4.2 Test Points

The test point numbers listed in Table 3 refer to the test point numbers shown in the electrical schematic and in the silkscreen of the PCB.

Table 3: Evaluation Board Test Point Description

Test Point #	Name	Use
TP2, TP3	+3.3V	+3.3 V main board power supply, coming from the internal or external source, as defined from the jumpers JP3 and JP6. TP3 and TP4 are close to the breadboard area for easy wiring of the power supply.
TP6	VDD	2-pin test point, with one ground and one VDD signal directly connected to the 73S1215F and its decoupling capacitors. Can be used to measure the integrity of the digital power supply of the 73S1215F, or to add a decoupling capacitor.
TP7	VPC	2-pin test point, with one ground and one VPC signal directly connected to the 73S1215F and its decoupling capacitors. Can be used to measure the integrity of the power supply of the DC-DC converters of the 73S1215F, or to add a decoupling capacitor.
TP8	+5V	+5 V coming from either the USB bus or from the external DC block (connected to JP5), as selected with jumper on JP1. Can be used to test voltage presence.
TP9	+3.3VFIX	+3.3 V coming from the on-board regulator (powered from either the USB bus or the external DC block). Can be used to test voltage presence.
TP10	Smart Card Contacts – Interface #1	Header for measurement of the card signals, close to the card connectors. Contains the card signals VCC1, RST1, CLK1, C81 and C41. Each contact has its own ground pin on the header.
TP11 to TP17	GND	Ground test points. Can be used for grounding of lab equipment probes.
TP18	Card Detect – Interface #1	Card detect signal coming directly from the card connectors.
TP21	USR(8:0)	Standard 9/8-bit user I/O port of the 73S1215F.  Some of the user I/Os are shared by the LCD interface and the extension 73S80xx daughter board when using additional external smart card interfaces. Only one should be used at a time.
TP22	USB	TP22 has 4 pins, connected to the USB D+ and D- wires, as well as 2 grounds.
TP24	VBUS	+5V USB bus. Can be used as a test point for USB voltage presence.
TP25	Smart Card Contacts – Interface #2	Header for measurement of the card signals, close to the card connectors. Contains the card signals VCC2, RST2, CLK2, C42 and C82. Each contact has its own ground pin on the header.
TP26	INT3	Interrupt input #3 secondary test points.
TP27	ROW[0:5]	The row pins used for the keypad interface.
TP28	LED0-4	The LED outputs from the 73S1215F.
TP29	COL[0:4]	The column pins used for the keypad interface.
TP30	INT2-3	Interrupt input #2 and #3 of the 73S1215F. This header is close to the breadboard area for easy wiring.
TP31	RX, TX	The TX and RX serial UART I/O signals (3.3 V digital logic level).
TP32	ANALOG IN	Analog input test point. Analog voltage can be connected to this test point for voltage comparison.
TP34	CPUCLK	This pin outputs the oscillator clock of the 73S1215F device. Can be used as a clock source for any purpose.

4.3 Schematic

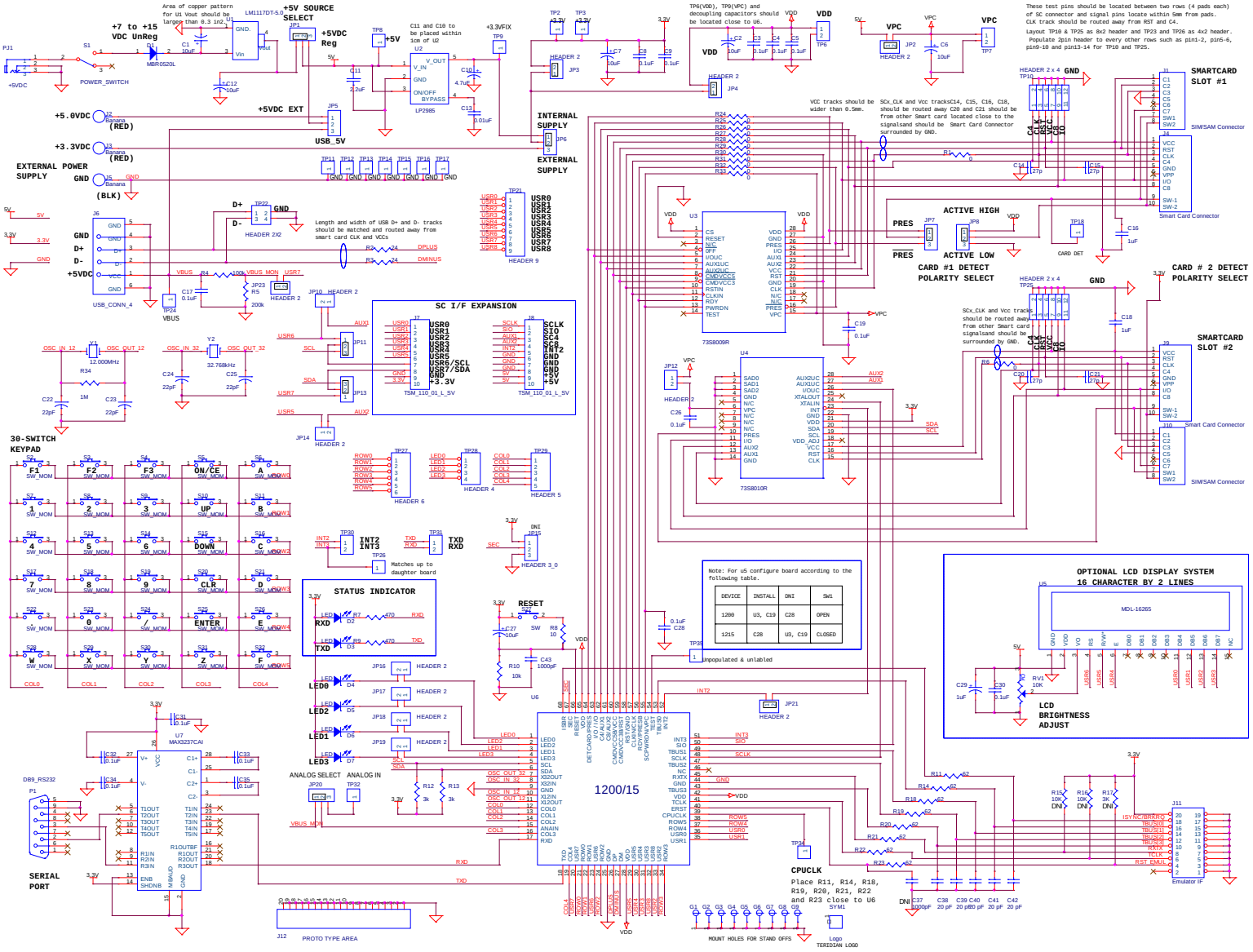

Figure 8: 73S1215F Evaluation Board Electrical Schematic

4.4 PCB Layouts

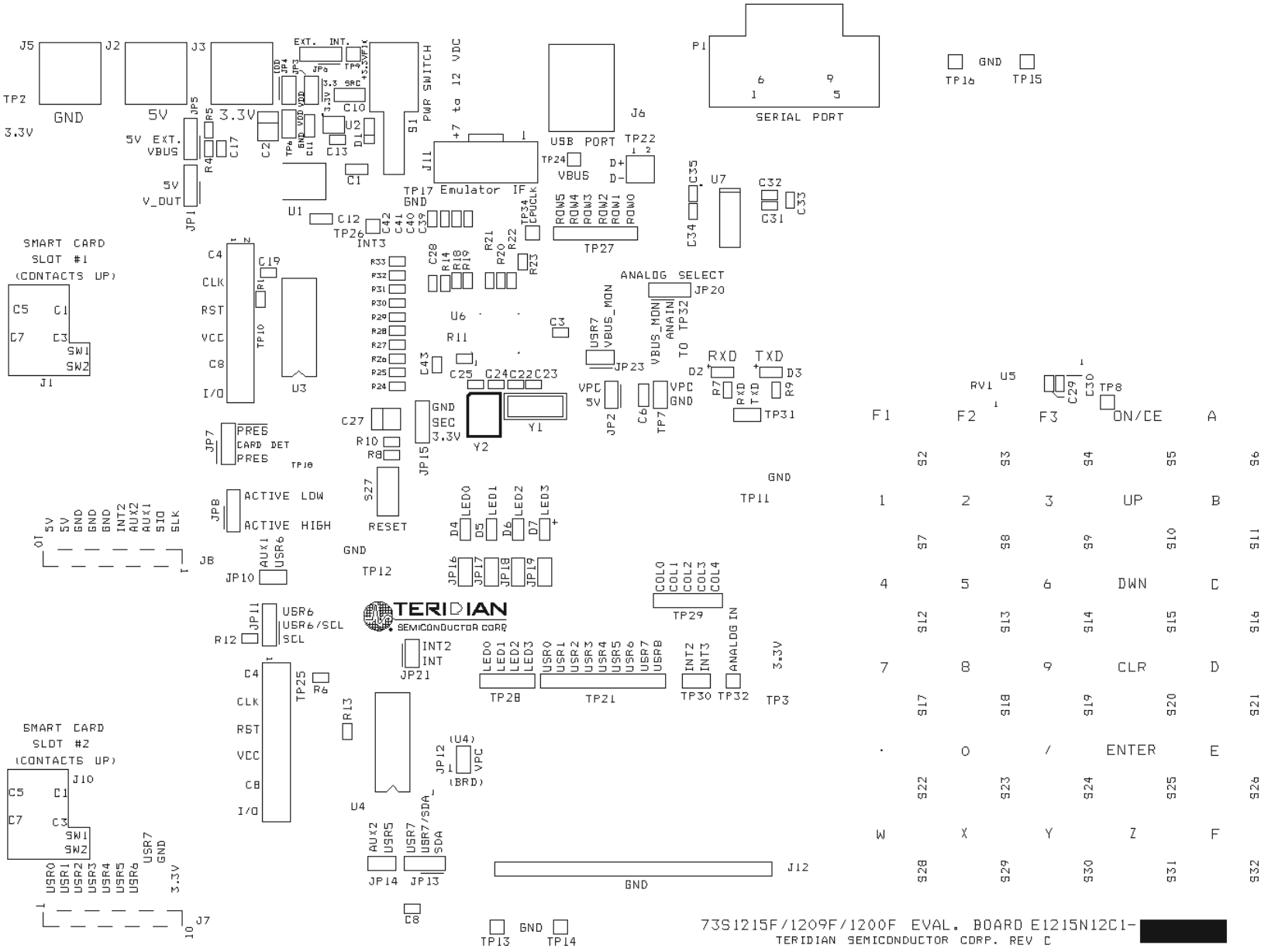

Figure 9: 73S1215F Evaluation Board Top View (Silkscreen)

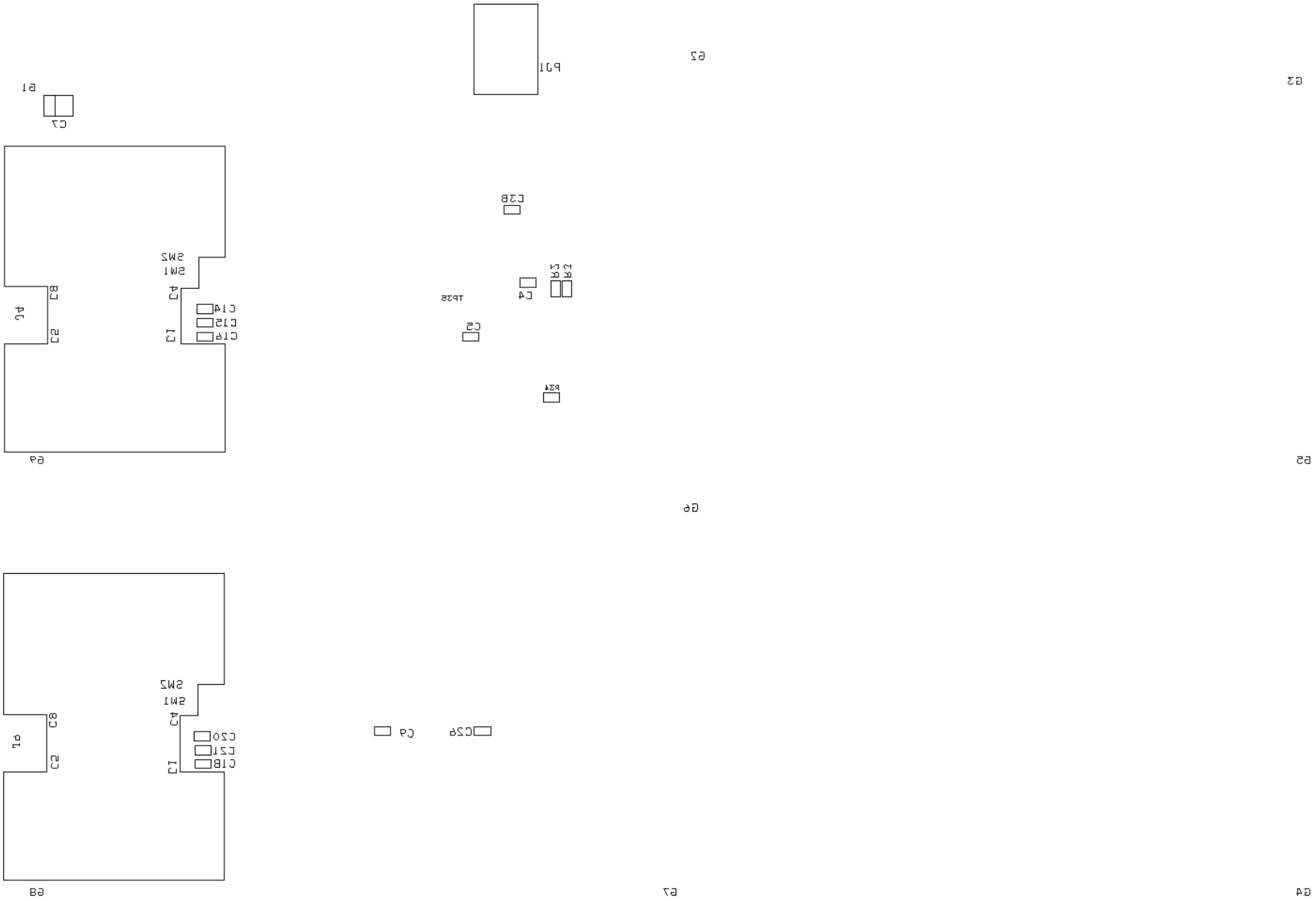

Figure 10: 73S1215F Evaluation Board Bottom View (Silkscreen)

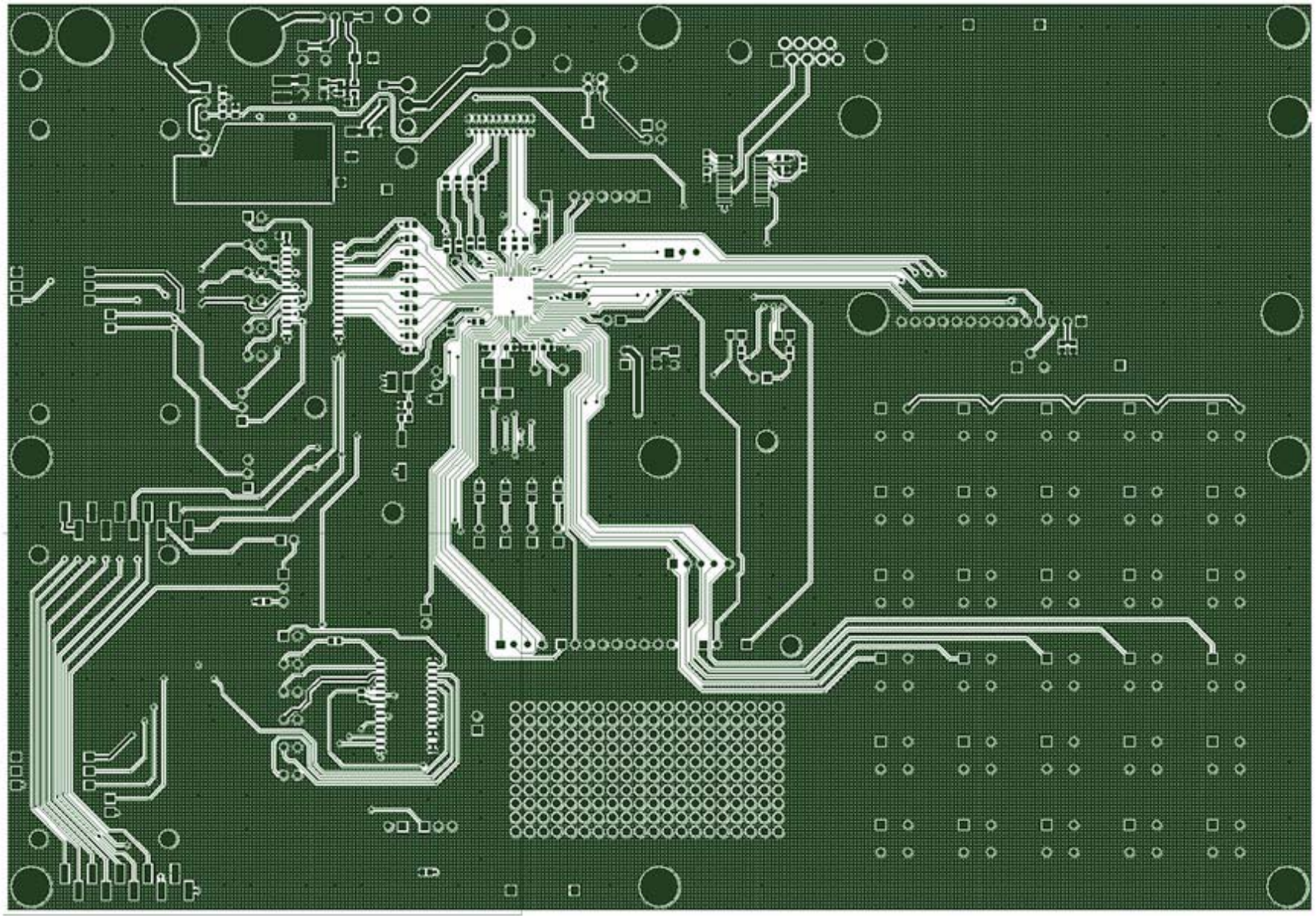

Figure 11: 73S1215F Evaluation Board Top Signal Layer

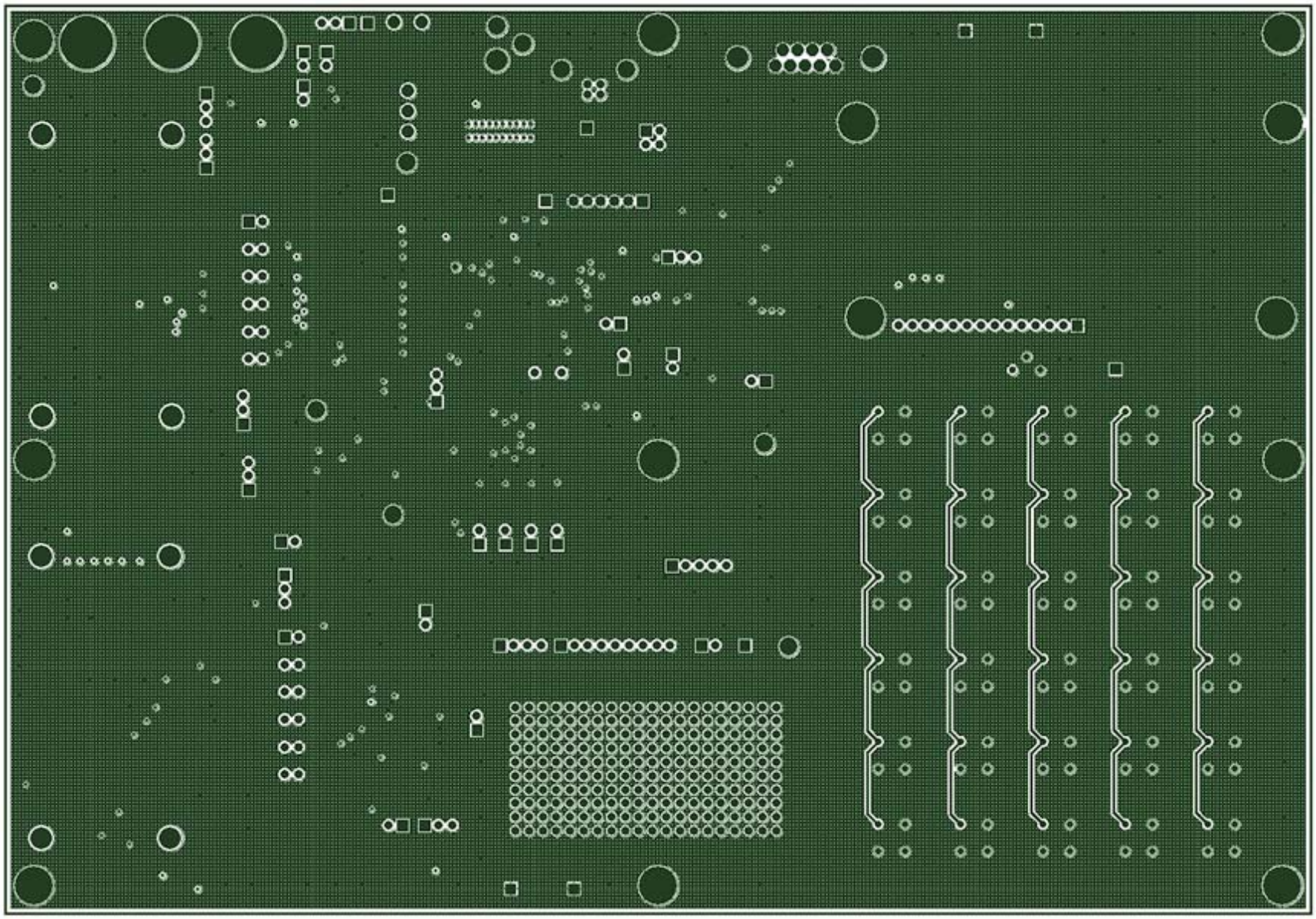

Figure 12: 73S1215F Evaluation Board Middle Layer 1 – Ground Plane

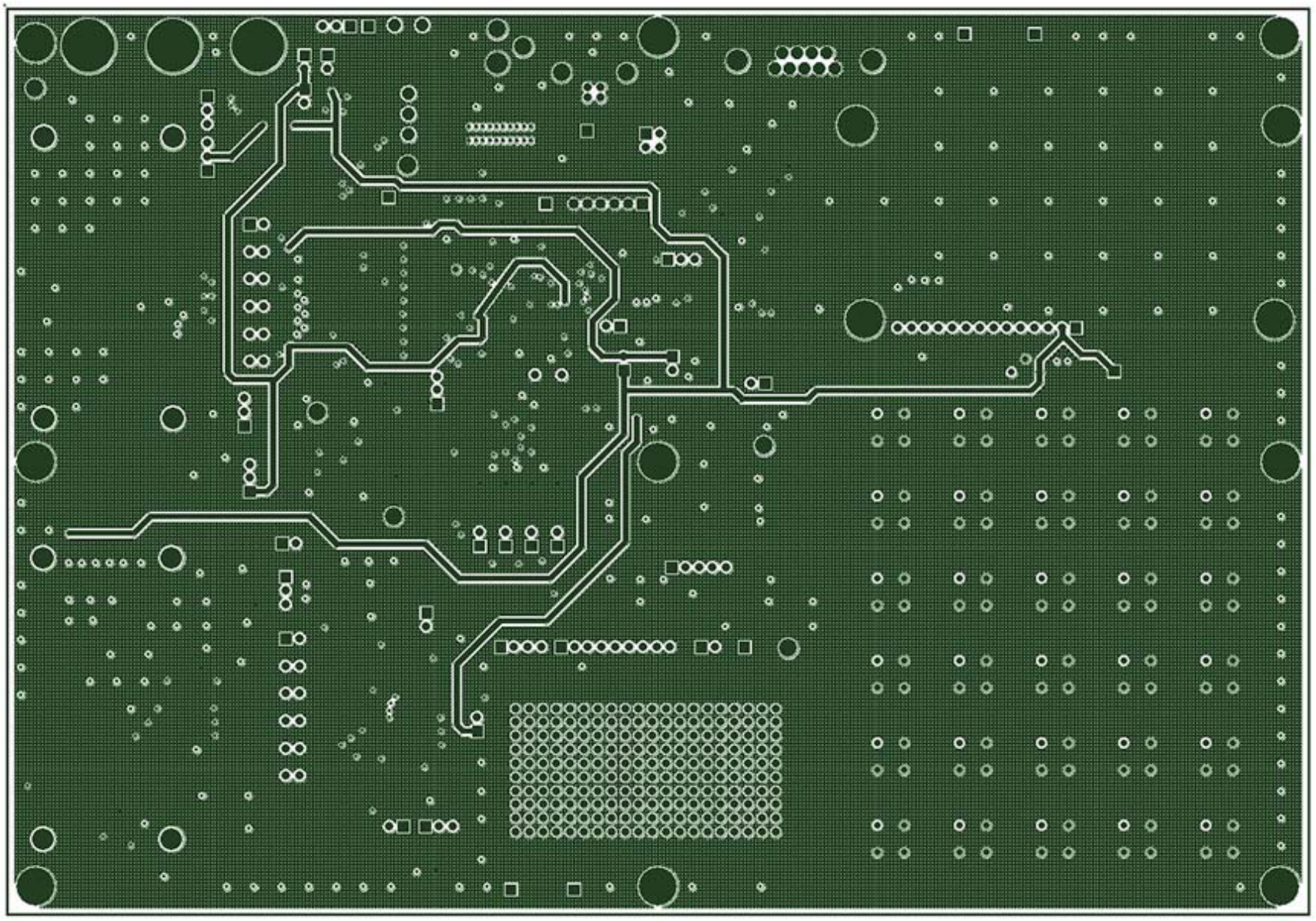

Figure 13: 73S1215F Evaluation Board Middle Layer 2 – Supply Plane

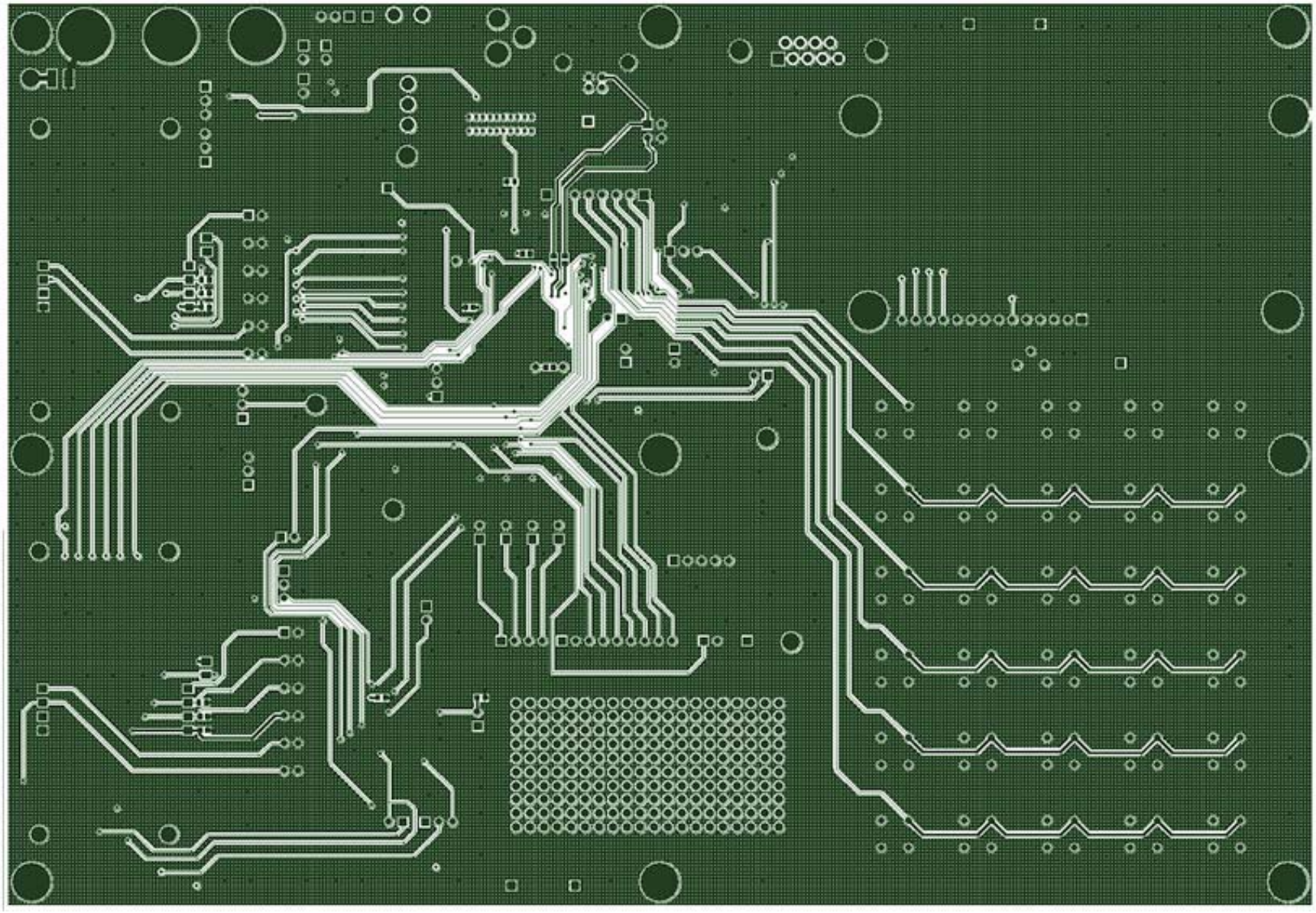

Figure 14: 73S1215F Evaluation Board Bottom Signal Layer

4.5 Bill of Materials

Table 4 provides the bill of materials for the 73S1215F Evaluation Board schematic provided in Figure 8.

Table 4: 73S1215F Evaluation Board Bill of Materials

Item	Qty.	Reference	Part	PCB Footprint	Digi-key Part Number	Part Number	Manufacturer
1	3	C2,C7,C27	10 µF	3528-21 (EIA)	478-1672-1-ND	TAJB106K010R	AVX Corporation
2	3	C1,C6,C12	10 µF	805	PCC2225CT-ND	ECJ-2FB0J106M	Panasonic
3	15	C3,C4,C5,C8,C9,C17,C19 C26,C28,C30,C31,C32, C33, C34,C35	0.1 µF	603	PCC1762CT-ND	ECJ-1VB1C104K	WALISN
4	1	C10	4.7 µF	1206	PCC2177CT-ND	ECJ-3YB1A475M	Panasonic
5	1	C11	2.2 µF	805	PCC1923CT-ND	ECJ-2YB0J225K	Panasonic
6	1	C13	0.01 µF	603	445-1311-1-ND	C1608X7R1H103K	TDK Corporation
7	4	C14,C15,C20,C21	27 pF	603	PCC270ACVCT-ND	ECJ-1VC1H270J	Panasonic
8	3	C16,C18,C29	1 µF	603	PCC2174CT-ND	C1608X5R1A105K	TDK Corporation
9	9	C22,C23,C24,C25,C38, C39, C40, C41, C42	22 pF	603	PCC220ACVCT-ND	ECJ-1VC1H220J	Panasonic
10	1	C43	1000 pF	603	PCC2151CT-ND	ECJ-1VC1H102J	Panasonic
11	1	D1	MBR0520L	SOD-123	MBR0520LCT-ND	MBR0520L	Fairchild
12	6	D2,D3,D4,D5,D6,D7	LED	805	160-1414-1-ND	LTST-C170FKT	LITE-ON INC
13	9	JP1,JP5,JP6,JP7,JP8, JP11, JP13,JP15, JP20	HEADER 3	1 x 3 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
14	12	JP2,JP3,JP4,JP10,JP12, JP14,JP16,JP17,JP18, JP19,JP21, JP23	HEADER 2	1 x 2 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
15	2	J1,J10	SIM/SAM Connector	ITT_CCM003_3754	CCM03-3754CT-ND	CCM03-3754CT-ND	C&K
16	2	J2,J3	Banana (red)	Banana		16BJ381	Mouser
17	1	J5	Banana (black)	Banana		16BJ382	Mouser
18	2	J9,J4	Smart Card Connector	ITT_CCM002-2504	401-1715-ND	CCM02-2504LFT	C&K
19	1	J6	USB_CONN_4	USB_AU_Y1007	ED90064-ND	897-43-004-90-000000	Mill-Max
20	2	J8,J7	TSM_110_01_L_SV	TSM_110_01_L_SV		TSM_110_01_L_SV	Samtec
21	1	J11	Emulator IF	10 X 2 pin	A3210-ND	5-104068-1	AMP/Tyco Electronics

Item	Qty.	Reference	Part	PCB Footprint	Digi-key Part Number	Part Number	Manufacturer
22	1	PJ1	+12 VDC	RAPC722	SC1153-ND	RAPC722-X	Switchcraft
23	1	P1	DB9_RS232	AMP_745781	A2100-ND	745781-4	AMP/Tyco Electronics
24	1	RV1	10 kΩ	3266W	3266W-103-ND	3266W-1-103	Bourns
25	12	R1,R6,R24-R33	0 Ω	603	P0.0GCT-ND	ERJ-3GEY0R00V	Panasonic
26	2	R2,R3	24 Ω	603	P24GCT-ND	ERJ-3GEYJ240V	Panasonic
27	1	R4	100 kΩ	603	P100KGCT-ND	ERJ-3GEYJ104V	Panasonic
28	1	R5	200 kΩ	603	P200KGCT-ND	ERJ-3GEYJ204V	Panasonic
29	2	R7,R9	470 Ω	603	P470GCT-ND	ERJ-3GEYJ471V	Panasonic
30	1	R8	10 Ω	603	P10GCT-ND	ERJ-3GEYJ100V	Panasonic
31	1	R10	10 kΩ	603	P10KGCT-ND	ERJ-3GEYJ103V	Panasonic
32	8	R11,R14,R18,R19,R20, R21, R22,R23	62 Ω	603	P62GCT-ND	ERJ-3GEYJ620V	Panasonic
33	2	R12,R13	3 kΩ	603	P3.0KGCT-ND	ERJ-3GEYJ302V	Panasonic
34	1	R34	1 MΩ	603	P1.0MGCT-ND	ERJ-3GEYJ106V	Panasonic
35	1	S1	POWER_SWITCH	POW_SW	EG2363-ND	100SP1T2B4M6RE	E-Switch
36	30	S2,S3,S4,S5,S6,S7,S8, S9,S10,S11,S12,S13,S14 S15,S16,S17,S18,S19, S20,S21,S22,S23,S24, S25,S26,S28,S29,S30, S31,S32	SW_MOM	Pushbutton SW	401-1005-ND	D6 C 10	ITT Industries
37	1	S27	SW	Panasonic EVQ	P8051SCT	SKQBB010	Panasonic
38	12	TP8,TP9,TP13,TP14,TP15, TP16,TP17,TP24,TP26, TP32, TP34, TP35	TP	1 Pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
39	1	TP18		1 pin White	5012K-ND	5012	Keystone Electronics
40	2	TP2,TP3		1 pin Red	5010K-ND	5010	Keystone Electronics
41	2	TP11,TP12	TP	1 pin Black	5011K-ND	5011	Keystone Electronics
42	4	TP6,TP7,TP30,TP31	TP2	1 x 2 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
43	2	TP10,TP25	HEADER 2 x 4	6 x 2 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
44	1	TP21	HEADER 9	1 x 9 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics

Item	Qty.	Reference	Part	PCB Footprint	Digi-key Part Number	Part Number	Manufacturer
45	1	TP22	HEADER 2X2	2 x 2 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
46	1	TP27	HEADER 6	6 x 1 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
47	1	TP28	HEADER 4	4 x 1 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
48	1	TP29	HEADER 5	5 x 1 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
49	1	U1	LM1117DT-5.0	TO-252-3	LM1117DT-5.0-ND	LM1117DT-5.0	National Semiconductor
50	1	U2	LP2985		LP2985IM5-3.3CT-ND	LP2985IM5-3.3	National Semiconductor
51	1	U4	73S8010R		73S8010R		Teridian Semiconductor
52	1	U5	MDL-16265		153-1078-ND	MDL-16265-SS-LV	Varitronix
53	1	U6	73S1215F	68 QFN		73S1215F	Teridian Semiconductor
54	1	U7	MAX3237CAI		MAX3237CAI-ND	MAX3237CAI	Maxim
55	1	Y1	12.000 MHz		X1116-ND	ECS-120-20-4XDN	ECS
56	1	Y2	32.768 kHz		XC1195CT-ND	ECS-.327-12.5-17X-TR	ECS

4.6 Schematic Information

This section provides recommendations on proper schematic design that will help in designing circuits that are functional and compatible with the software library APIs provided by Teridian.

4.6.1 Reset Circuit

The 73S1215F Evaluation Board provides a reset pushbutton that can be used when prototyping and debugging software. The RESET pin should be supported by the external components shown in Figure 15. R8 should be around 10 Ω. The capacitor C27 should be 10 µF. R8 and C27 should be mounted as close as possible to the IC.

C43 (1000 pF) is shown for EFT protection and is optional.

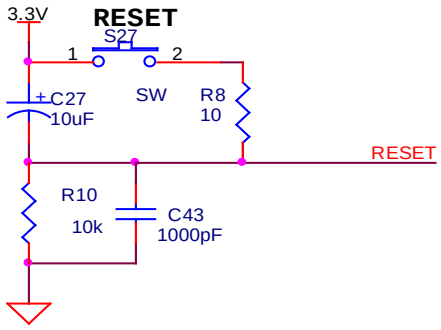

Figure 15: External Components for RESET

4.6.2 Oscillators

The 73S1215F offers two oscillators (see Figure 16); one for the primary system clock and the other for an RTC (32 KHz). The system clock should use a 12 MHz crystal to provide the proper system clock rates for the USB, serial and smart card interfaces. The system oscillator requires a 1 MΩ parallel resistor to insure proper oscillator startup.

The RTC oscillator drives a standard 32.768 kHz watch crystal. Crystals of this type are accurate and do not require a high current oscillator circuit. The oscillator in the 73S1215F has been designed specifically to handle watch crystals and is compatible with their high impedance and limited power handling capability.

The 32 KHz oscillator does not require a parallel startup resistor.

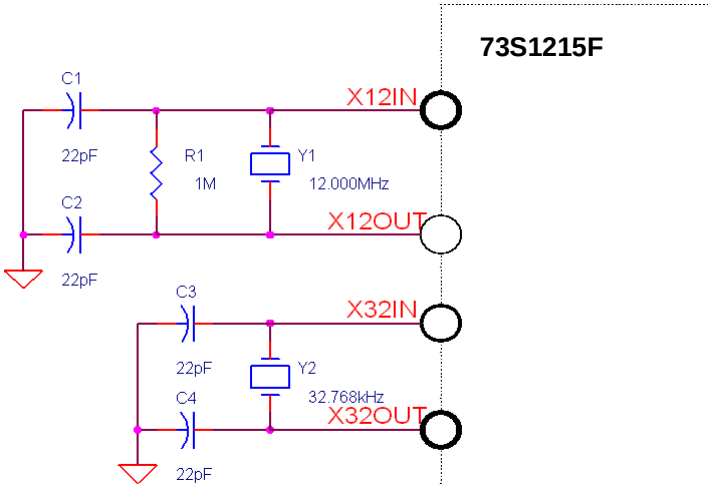

Figure 16: Oscillator Circuit

4.6.3 LCD

The 73S1215F does not contain an on-chip LCD controller. However, an LCD module (with built-in controller) can be used with the 73S1215F via use of specific USR (GPIO) pins. The LCD API libraries support up to a 2 line/16 character display. Figure 17 shows the basic connection for this type of LCD. The LCD module must connect to the USR pins as shown and it requires an external brightness adjust circuit.

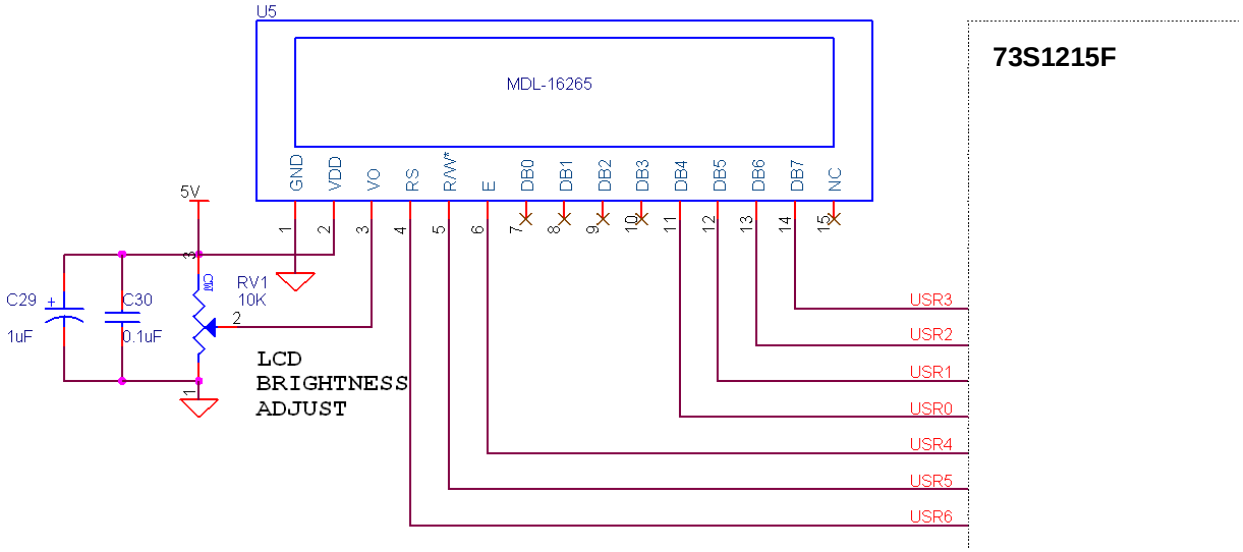

Figure 17: LCD Connections

4.6.4 USB Interface

The USB interface on the 73S1215F requires few external components for proper operation. Two serial resistors of 24 Ω ± 1% are needed to provide proper impedance matching for the USB data signals D+ and D-.

For self-powered USB applications, a connection must be made between the VBUS power input and USR7 for proper operation with the provided API libraries. A direct connection can not be made as the VBUS voltage exceeds the digital power supply running at 3.3 V. As a result, a resistor divider is required to scale the VBUS voltage down to 3.3 V. Figure 18 shows the basic USB connections.

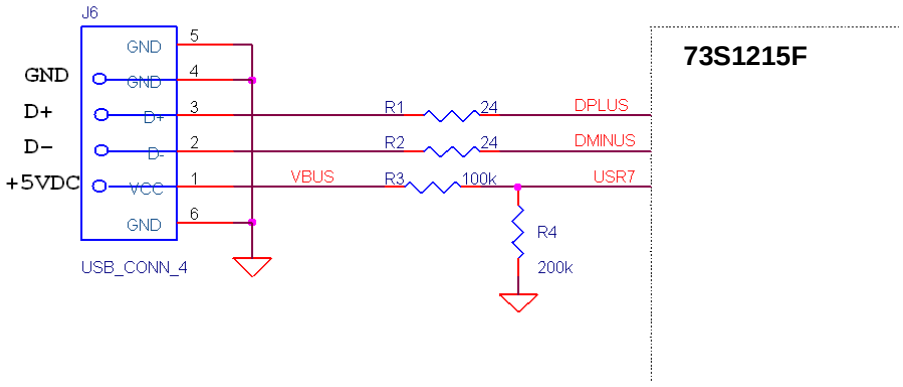

Figure 18: USB Connections

4.6.5 Smart Card Interface

The smart card interface on the 73S1215F requires few external components for proper operation. Figure 19 shows the recommended smart card interface connections.

- The RST and CLK signals should have 27 pF capacitors at the smart card connector.
- It is recommended that a 0 Ω resistor be added in series with the CLK signal. If necessary, in noisy environments, this resistor can be replaced with a small resistor to create a RC filter on the CLK signal to reduce CLK noise. This filter is used to soften the clock edges and provide a cleaner clock for those environments where this could be problematic.
- The VCC output must have a 1.0 μF capacitor at the smart card connector for proper operation.
- The VPC input is the power supply input for the smart card power. It is recommended that both a 10 μF and a 0.1 μF capacitor are connected to provide proper decoupling for this input.
- The PRES input on the 73S1215F contains a very weak pull down resistor. As a result, an additional external pull down resistor is recommended to prevent any system noise from triggering a false card event. The same holds true for the $\overline{\text{PRES}}$ input, except a pull up resistor is utilized as the logic is inverted from the PRES input.

The smart card interface layout is important. The following guidelines should be followed to provide the optimum smart card interface operation:

- Route auxiliary signals away from card interface signals
- Keep CLK signal as short as possible and with few bends in the trace. Keep route of the CLK trace to one layer (avoid vias to other plane). Keep CLK trace away from other traces especially RST and VCC. Filtering of the CLK trace is allowed for noise purpose. Up to 30 pF to ground is allowed at the CLK pin of the smart card connector. Also, the zero ohm series resistor, R7, can be replaced for additional filtering (no more than 100 Ω).
- Keep VCC trace as short as possible. Make trace a minimum of 0.5 mm thick. Also, keep VCC away from other traces especially RST and CLK.
- Keep CLK trace away from VCC and RST traces. Up to 30 pF to ground is allowed for filtering
- Keep 0.1 μF close to VDD pin of the device and directly take other end to ground
- Keep 10 μF and 0.1 μF capacitors close to VPC pin of the device and directly take other end to ground
- Keep 1.0 μF close to VCC pin of the smart card connector and directly take other end to ground

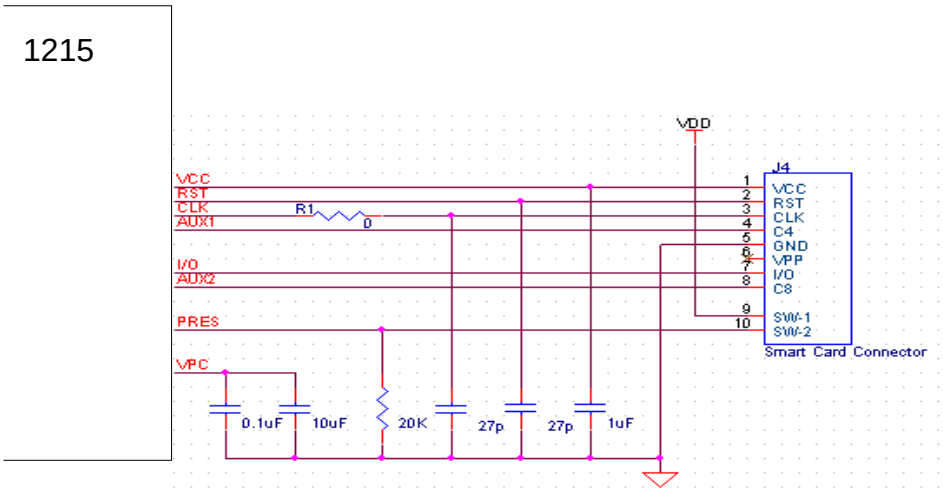

Figure 19: Smart Card Connections

5 Ordering Information

Part Description	Order Number
73S1215F 68-Pin QFN Evaluation Board	73S1215F-EB

6 Related Documentation

The following 73S1215F documents are available from Teridian Semiconductor Corporation:

73S1215F Data Sheet
73S1215F Evaluation Board Quick Start Guide
TSC Flash Programmer Model TFP2 User's Manual

7 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S1215F contact us at:

6440 Oak Canyon Road
Suite 100
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: scr.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
0.1	December 8, 2005	Document Created – Alpha version.
1.0	January 25, 2007	Added necessary rework instructions for proper board operation and API library compatibility.
1.1	April 17, 2007	Added 44 pin board.
1.2	June 9, 2007	Removed C36 and TP33 and added 20 pF capacitors to C38-C42 to the schematic and BOM.
1.3	November 9, 2007	Added emulator usage and schematic descriptions.
1.4	January 3, 2007	Removed capacitor and pull up resistors from the ICE interface.
1.5	March 5, 2007	Made BOM corrections.
1.6	March 27, 2007	Added new Rev C PWB for 64 pin device. Removed errata section. Fixed BOM for C6 and PJ1.
1.7	August 8, 2007	Modified incorrect part number for S1 in BOM.
1.8	August 17, 2009	Removed 44-pin board references. Added information from the Quick Start Guide. Miscellaneous editorial modifications.