FEATURES

- **700MHz min. count frequency**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **1000ps CLK to Q, $\overline{TC}$**
- **Internal, gated $\overline{TC}$ feedback**
- **8 bits wide**
- **Fully synchronous counting and $\overline{TC}$ generation**
- **Asynchronous Master Reset**
- **Fully compatible with industry standard 10KH, 100K I/O levels**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E016**
- **Available in 28-pin PLCC package**

DESCRIPTION

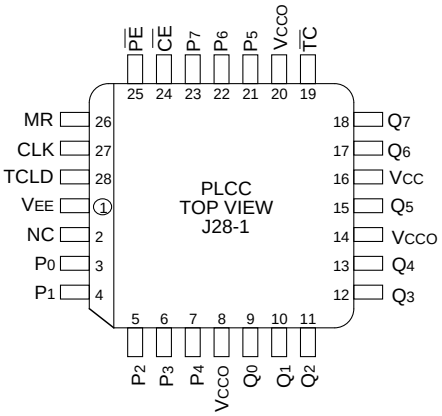
The SY10/100E016 are high-speed synchronous, presettable and cascadable 8-bit binary counters designed for use in new, high-performance ECL systems. Architecture and operation are the same as the Motorola MC10H016 in the MECL 10KH family, extended to 8 bits, as shown in the logic diagram.

The counters feature internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW, the $\overline{TC}$ feedback is disabled and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all-HIGH state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically reload upon $\overline{TC}$ = LOW, thus functioning as a programmable counter.

PIN NAMES

Pin	Function
P_0-P_7	Parallel Data (Preset) Inputs
Q_0-Q_7	Data outputs
$\overline{CE}$	Count Enable Control Input
$\overline{PE}$	Parallel Load Enable Control Input
MR	Master Reset
CLK	Clock
$\overline{TC}$	Terminal Count Output
TCLD	TC-Load Control Input
V_{CCO}	V_{CC} to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

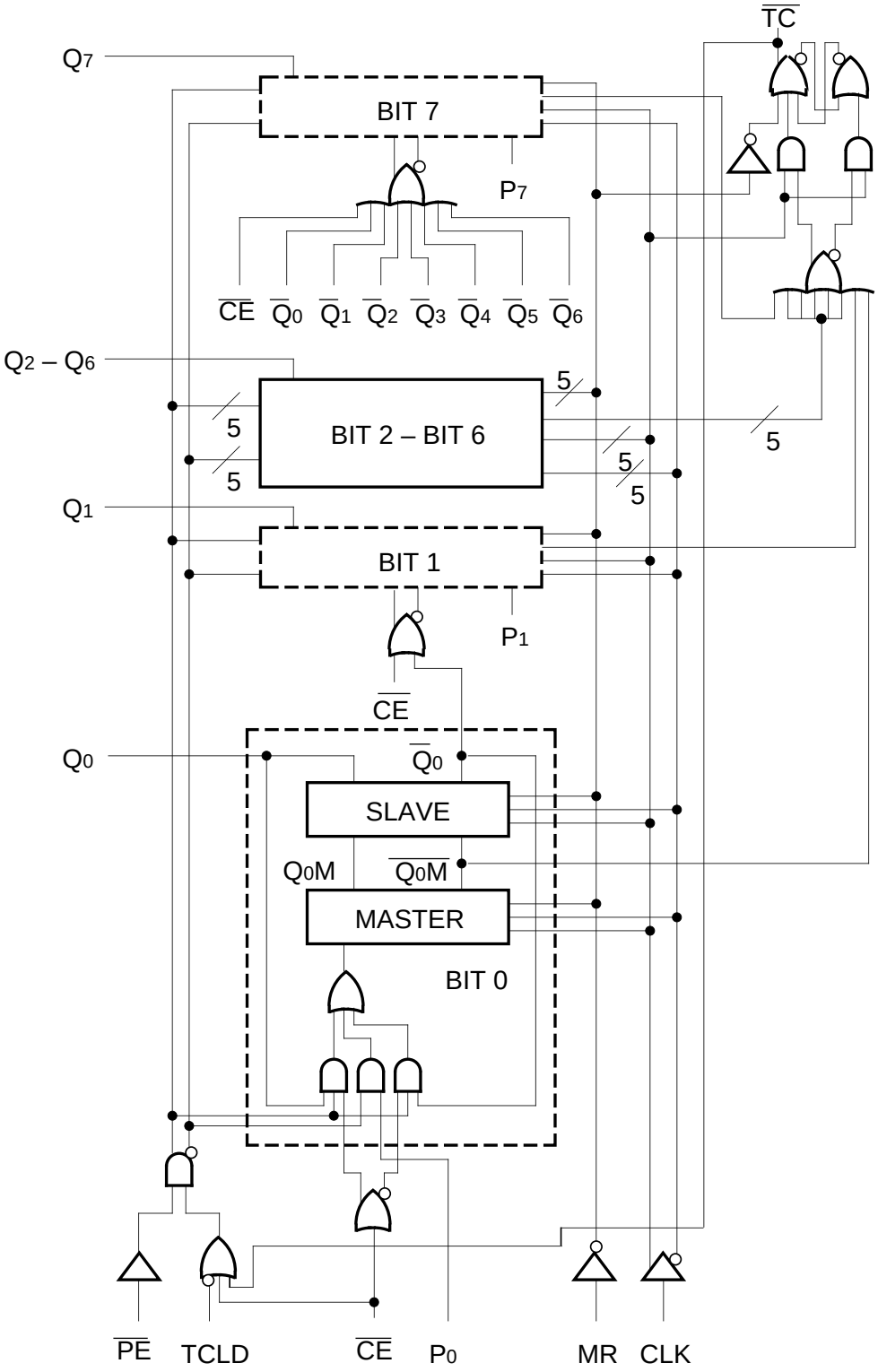
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E016JI	J28-1	Industrial	SY10E016JI	Sn-Pb
SY10E016JITR[2]	J28-1	Industrial	SY10E016JI	Sn-Pb
SY100E016JI	J28-1	Industrial	SY100E016JI	Sn-Pb
SY100E016JITR[2]	J28-1	Industrial	SY100E016JI	Sn-Pb
SY10E016JC	J28-1	Commercial	SY10E016JC	Sn-Pb
SY10E016JCTR[2]	J28-1	Commercial	SY10E016JC	Sn-Pb
SY100E016JC	J28-1	Commercial	SY100E016JC	Sn-Pb
SY100E016JCTR[2]	J28-1	Commercial	SY100E016JC	Sn-Pb
SY10E016JY[3]	J28-1	Industrial	SY10E016JY with Pb-Free bar-line indicator	Matte-Sn
SY10E016JYTR[2, 3]	J28-1	Industrial	SY10E016JYwith Pb-Free bar-line indicator	Matte-Sn
SY100E016JY[3]	J28-1	Industrial	SY100E016JY with Pb-Free bar-line indicator	Matte-Sn
SY100E016JYTR[2, 3]	J28-1	Industrial	SY100E016JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM



TRUTH TABLE[1]

$\overline{CE}$	$\overline{PE}$	TCLD	MR	CLK	Function
X	L	X	L	Z	Load Parallel (P_n to Q_n)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Master respond, Slaves Hold
X	X	X	H	Z	Reset (Q_n : = LOW, $\overline{TC}$: = HIGH)

NOTE:

1. Z = Clock Pulse (LOW-to-HIGH), ZZ = Clock Pulse (HIGH-to-LOW)

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{EE}	Power Supply Current													mA
	10E	—	151	181	—	151	181	—	151	181	—	151	181	
	100E	—	151	181	—	151	181	—	151	181	—	174	208	

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = –40°C			T_A = 0°C			T_A = 25°C			T_A = +85°C			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
f_{COUNT}	Max. Count Frequency	700	900	—	700	900	—	700	900	—	700	900	—	MHz
t_{PD}	Propagation Delay to Output													ps
	CLK to Q	600	725	1000	600	725	1000	600	725	1000	600	725	1000	
	MR to Q	600	775	1000	600	775	1000	600	775	1000	600	775	1000	
	CLK to TC (Qs loaded)[1]	550	775	1050	550	775	1050	550	775	1050	550	775	1050	
	CLK to TC (Qs unloaded)[1]	550	700	900	550	700	900	550	700	900	550	700	900	
	MR to TC	625	775	1000	625	775	1000	625	775	1000	625	775	1000	
t_S	Set-up Time													ps
	$\underline{Pn}$	150	–30	—	150	–30	—	150	–30	—	150	–30	—	
	$\overline{CE}$	600	400	—	600	400	—	600	400	—	600	400	—	
	$\overline{PE}$	600	400	—	600	400	—	600	400	—	600	400	—	
	TCLD	500	300	—	500	300	—	500	300	—	500	300	—	
t_H	Hold Time													ps
	$\underline{Pn}$	250	30	—	250	30	—	250	30	—	250	30	—	
	$\overline{CE}$	0	–400	—	0	–400	—	0	–400	—	0	–400	—	
	$\overline{PE}$	0	–400	—	0	–400	—	0	–400	—	0	–400	—	
	TCLD	100	–300	—	100	–300	—	100	–300	—	100	–300	—	
t_{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	900	700	—	ps
t_{WP}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	400	—	—	ps
t_r t_f	Rise/Fall Times 20% to 80%	300	510	800	300	510	800	300	510	800	300	510	800	ps

NOTE:

1. CLK to $\overline{TC}$ propagation delay is dependent on the loading of the Q outputs. With all of the Q outputs loaded, the noise generated in going from a IIII IIII state to a 0000 0000 state causes the CLk to $\overline{TC}$+ delay to increase.

FUNCTION TABLE

Function	$\overline{PE}$	$\overline{CE}$	MR	TCLD	CLK	P_7–P_4	P_3	P_2	P_1	P_0	Q_7–Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Count	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	L	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Hold	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
Load On	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H
Terminal	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H
Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	L	H
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	H	H
	H	L	L	H	Z	H	L	H	H	L	H	H	L	L	L	H
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H

APPLICATIONS INFORMATION

Cascading Multiple E016 Devices

For applications which call for larger than 8-bit counters, multiple E016s can be tied together to achieve very wide bit width counters. The active low terminal count ($\overline{TC}$) output and count enable input ($\overline{CE}$) greatly facilitate the cascading of E016 devices. Two E016s can be cascaded without the need for external gating; however, for counters wider than 16 bits, external OR gates are necessary for cascade implementations.

Figure 1, below, pictorially illustrates the cascading of 4 E016s to build a 32-bit high frequency counter. Note the E101 gates used to OR the terminal count outputs of the lower order E016s to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state), the more significant E016 is set in its count mode and will count one binary digit upon the next positive clock transition. In addition, the preceding devices will also count one bit, thus sending their terminal count outputs back to a high state, disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an E016 in the chain to count all of the lower order terminal count outputs, it must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting E016 devices from Figure 1 and maintaining the logic pattern illustrated in the same figure.

The maximum frequency of operation for the cascaded counter chain is set by the propagation delay of the $\overline{TC}$ output and the necessary set-up time of the $\overline{CE}$ input and the propagation delay through the OR gate controlling it (for 16-bit counters the limitation is only the $\overline{TC}$ propagation delay and the $\overline{CE}$ set-up time). Figure 1 shows E101 gates used to control the count enable inputs; however, if the frequency of operation is lower, a slower ECL OR gate can be used. Using the worst case guarantees for these parameters from the ECLinPS data book, the maximum count frequency for a greater than 16-bit counter is 475MHz and that for a 16-bit counter is 625MHz. Note that this assumes the trace delay between the $\overline{TC}$ outputs and the $\overline{CE}$ inputs are negligible. If this is not the case, estimates of these delays need to be added to the calculations.

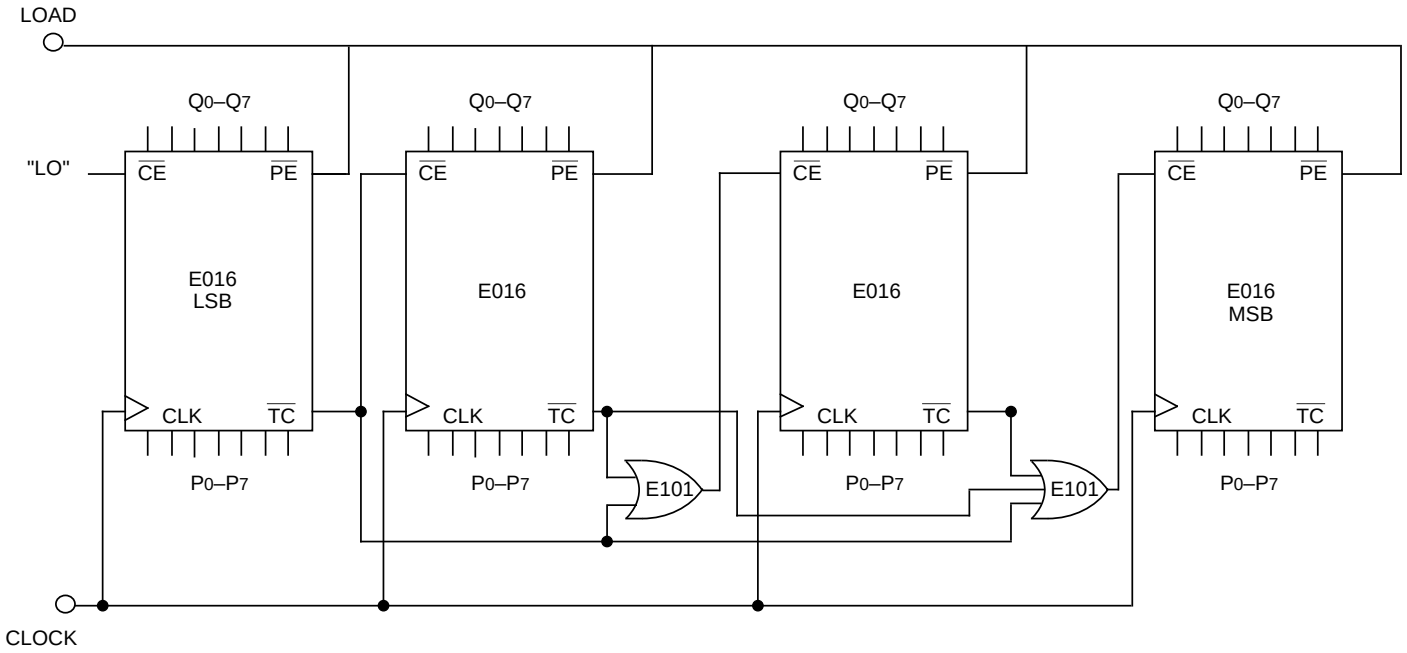


Figure 1. 32-Bit Cascaded E016 Counter

Programmable Divider

The E016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count), when asserted, reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 2 below illustrates the input conditions necessary for utilizing the E016 as a programmable divider set up to divide by 113.

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio for the binary value for 256. As an example for a divide ration of 113:

$PN's = 256 – 113 = 8F_{16} = 1000\ 1111$

where

P_0 = LSB and P_7 = MSB

Forcing this input condition, as per the set-up in Figure 2, will result in the waveforms of Figure 3. Note that the $\overline{TC}$ output

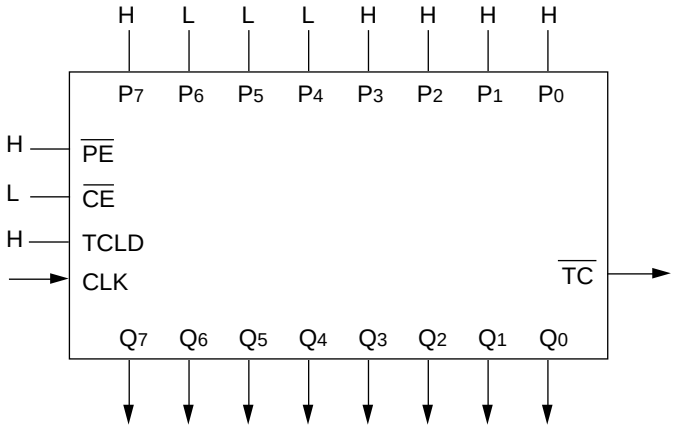


Figure 2. Mod 2 to 256 Programmable Divider

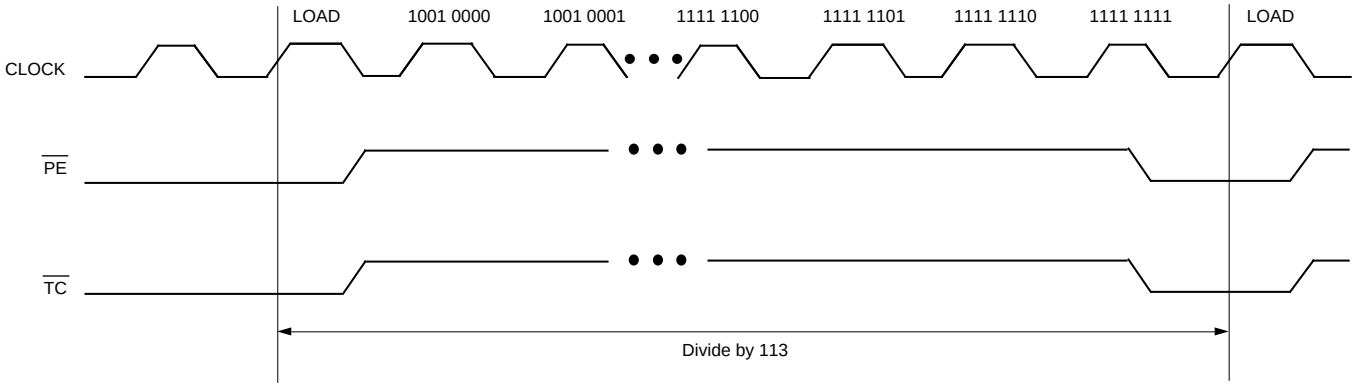


Figure 3. Divide by 113 E016 Programmable Divider Waveforms

Divide Ratio	Preset Data Inputs							
	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

Table 1. Preset Values for Various Divide Ratios

is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios twice the desired divide ratio can be loaded into the E016 and the $\overline{TC}$ output can feed the clock input of a toggle flip-flop to create a signal divided as desired with a 50% duty cycle.

A single E016 can be used to divide by any ratio from 2 to 256, inclusive. If divide ratios of greater than 256 are needed, multiple E016s can be cascaded in a manner similar to that already discussed. When E016s are cascaded to build larger dividers, the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple E016 divider chains.

Figure 4 on the following page shows a typical block diagram of a 32-bit divider chain. Once again, the maximize the frequency of operation, E101 OR gates were used. For lower frequency applications, a slower OR gate could replace the E101. Note that for a 16-bit divider, the OR function feeding the $\overline{PE}$ (program enable) input CANNOT be replaced by a wire OR tie as the $\overline{TC}$ output of the least significant E016 must also feed the CE input of the most significant E016. If the two $\overline{TC}$ outputs were OR tied, the cascaded count operation would not operate properly. Because in the cascaded form the $\overline{PE}$ feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

Maximizing E016 Count Frequency

The E016 device produces nine fast transitioning single-ended outputs; thus, V_{CC} noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This V_{CC} noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that, if the outputs are not going to be used in the rest of the system, they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system, only those outputs should be terminated. Not terminating the unused outputs will not only cut down the V_{CC} noise generated, but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs, or provide them

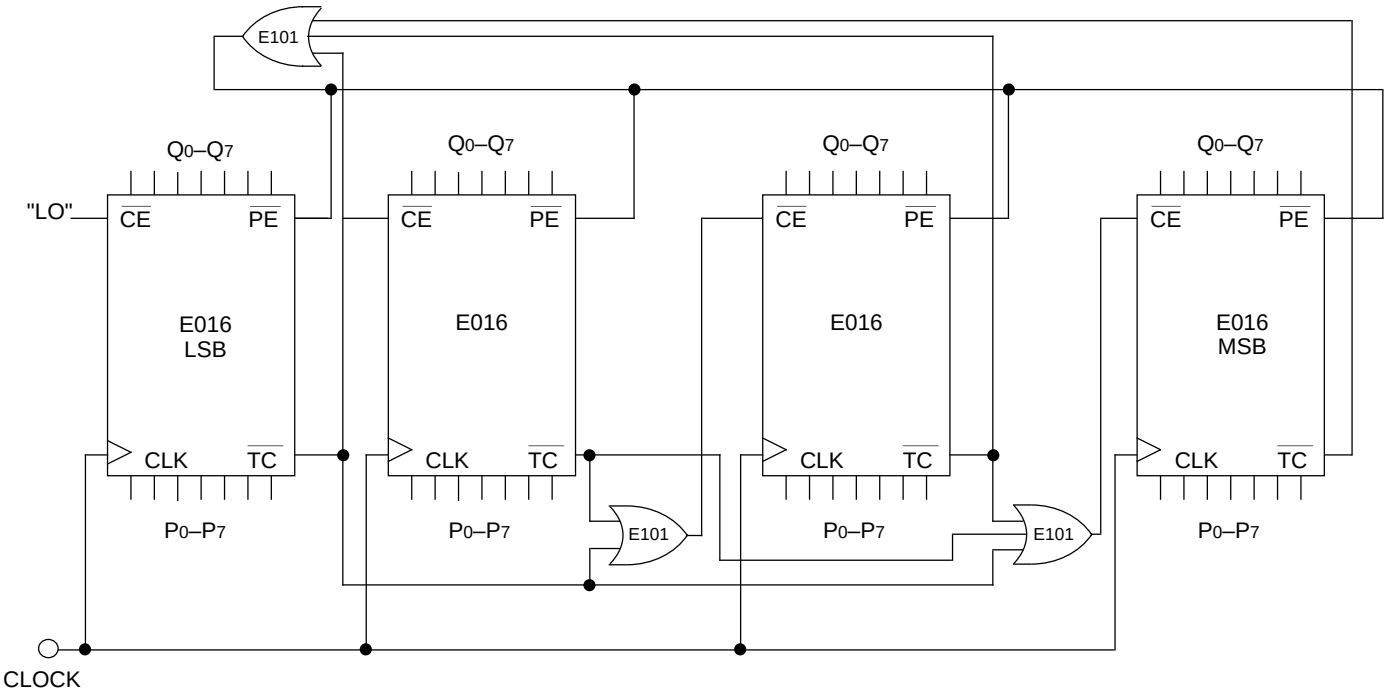
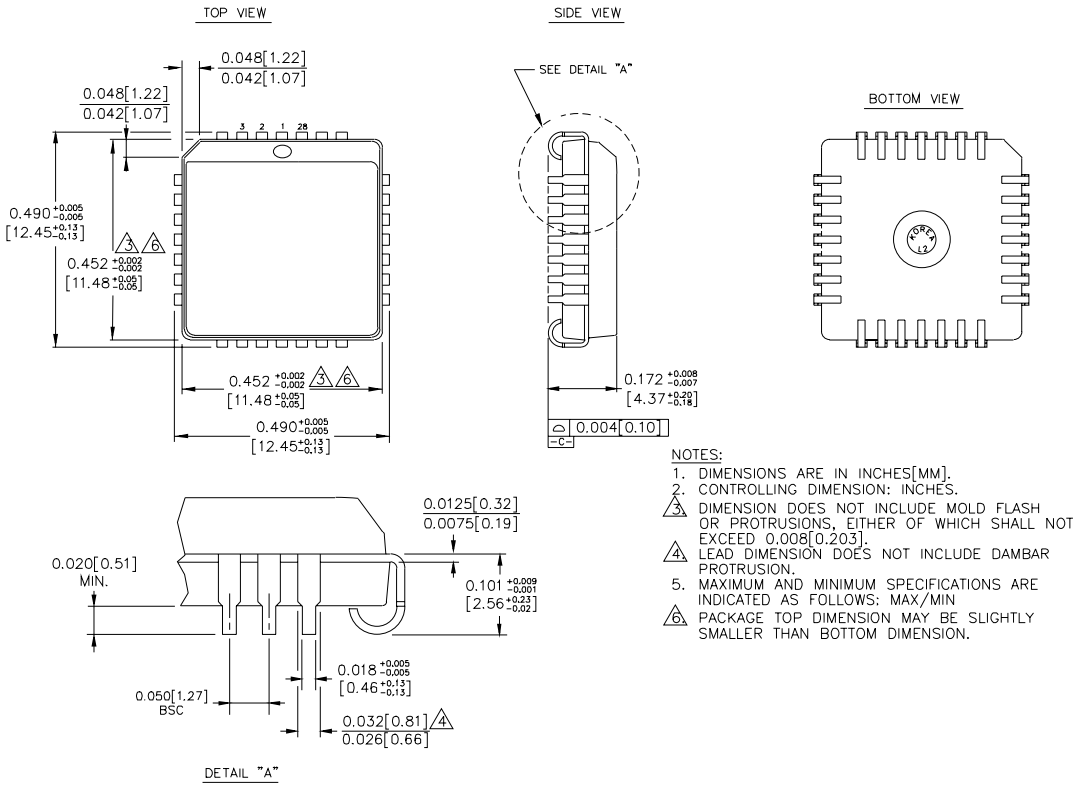


Figure 4. 32-Bit Cascaded E016 Programmable Divider

28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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