TOSHIBA Field-Effect Transistor Silicon N Channel MOS Type (U-MOSⅣ)

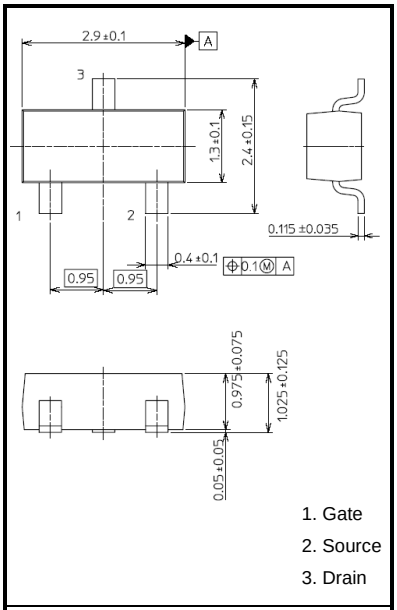
SSM3K7002BS

High-Speed Switching Applications

Analog Switch Applications

- Small package
- Low ON-resistance : $R_{DS(ON)}$ = 3.3 Ω (max) (@V_{GS} = 4.5 V)
  : $R_{DS(ON)}$ = 2.6 Ω (max) (@V_{GS} = 5 V)
  : $R_{DS(ON)}$ = 2.1 Ω (max) (@V_{GS} = 10 V)

Unit: mm



JEDEC	SOT-23
JEITA	-
TOSHIBA	2-3AA1A

Weight: 8.0 mg (typ.)

Absolute Maximum Ratings (Ta = 25℃)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	60	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	200	mA
	Pulse	I_{DP}	800	
Power dissipation		P_D (Note 1)	200	mW
Channel temperature		T_{ch}	150	℃
Storage temperature range		T_{stg}	−55 to 150	℃

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board. (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

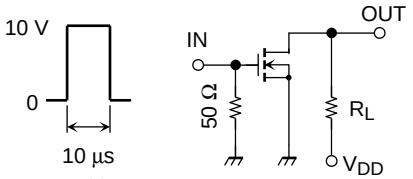
Electrical Characteristics (Ta = 25℃)

Characteristics		Symbol	Test Condition	Min	Typ	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0 V	—	—	±10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 0.1 mA, V_{GS} = 0 V	60	—	—	V
		$V_{(BR)\ DSX}$	I_D = 0.1 mA, V_{GS} = -10 V	45	—	—	
Drain cutoff current		I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 0.25 mA	1.0	—	2.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 200 mA (Note 2)	225	—	—	mS
Drain-source ON-resistance		$R_{DS\ (ON)}$	I_D = 500 mA, V_{GS} = 10 V (Note 2)	—	1.62	2.1	Ω
			I_D = 100 mA, V_{GS} = 5 V (Note 2)	—	1.77	2.6	
			I_D = 100 mA, V_{GS} = 4.5 V (Note 2)	—	1.81	3.3	
Input capacitance		C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	—	17.0	—	pF
Reverse transfer capacitance		C_{rss}		—	1.9	—	
Output capacitance		C_{oss}		—	3.6	—	
Switching time	Turn-on delay time	$td_{(on)}$	V_{DD} = 30 V, I_D = 200 mA, V_{GS} = 0 to 10 V	—	2.5	5.0	ns
	Turn-off delay time	$td_{(off)}$		—	18	55	
Drain-source forward voltage		V_{DSF}	I_D = -200 mA, V_{GS} = 0 V (Note 2)	—	-0.84	-1.2	V

Note2: Pulse test

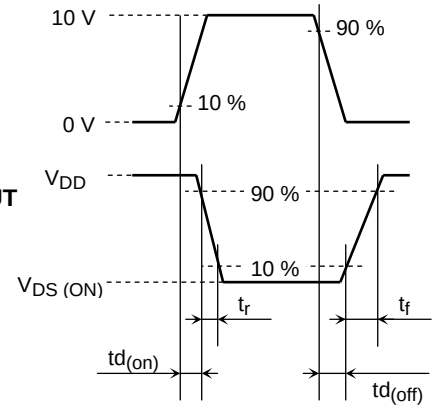
Switching Time Test Circuit

(a) Test circuit

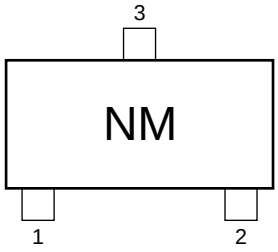


V_{DD} = 30 V
Duty ≦ 1%
V_{IN}: t_r, t_f < 2 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25 ℃

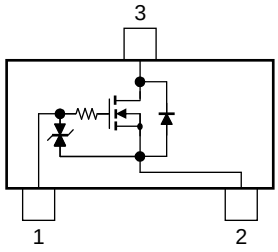
(b) V_{IN} and (c) V_{OUT}



Marking



Equivalent Circuit (top view)



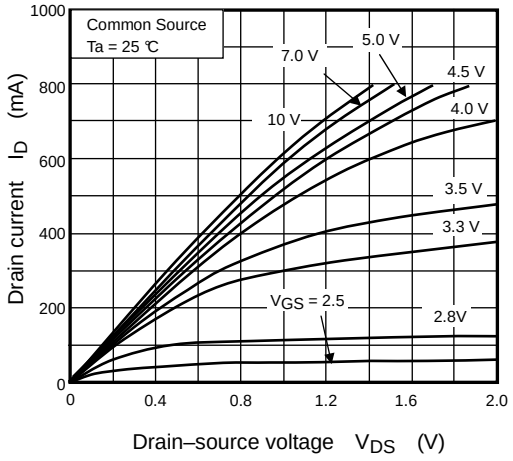
Precaution

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (0.25 mA for the SSM3K7002BS). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.
Take this into consideration when using the device.

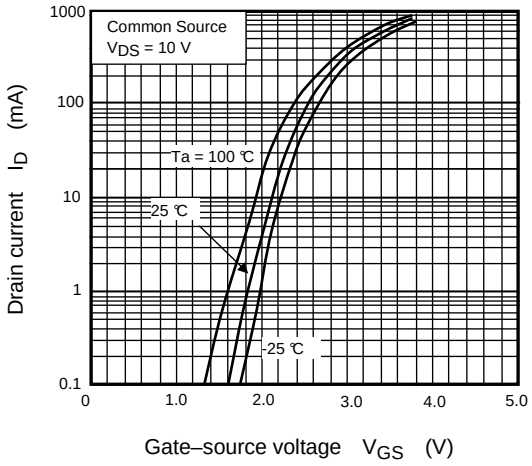
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

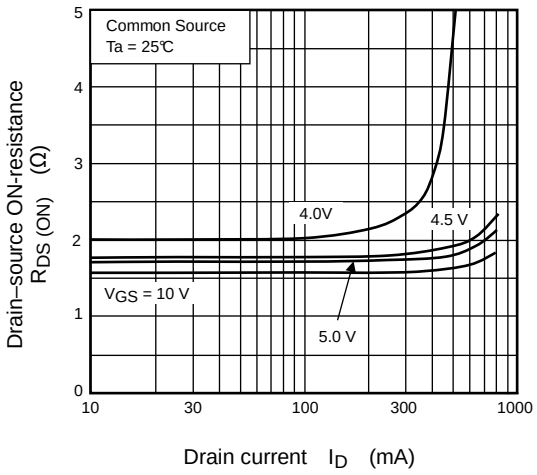
$I_D - V_{DS}$



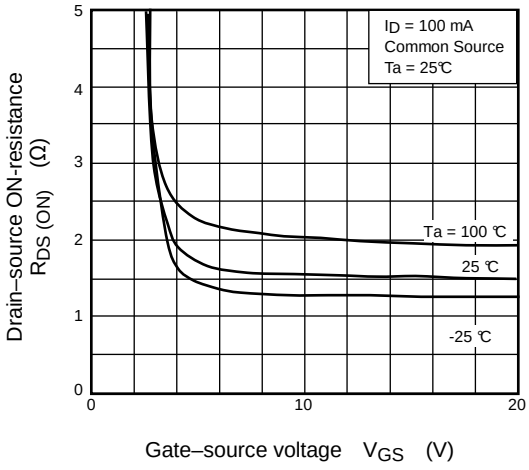
$I_D - V_{GS}$



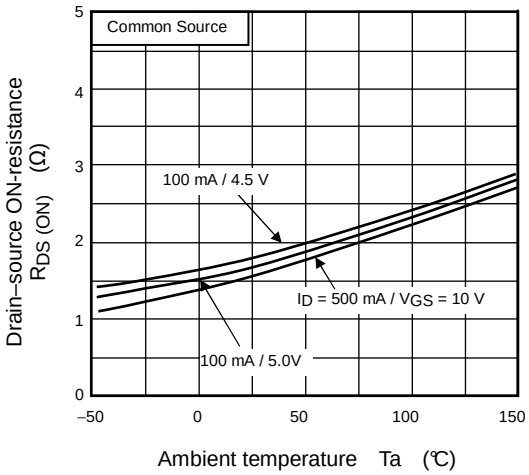
$R_{DS\ (ON)} - I_D$



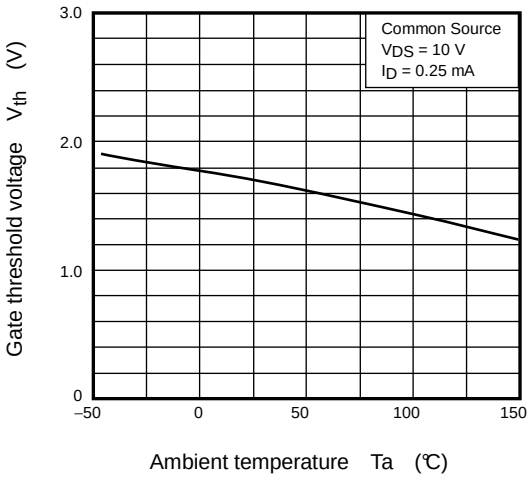
$R_{DS\ (ON)} - V_{GS}$

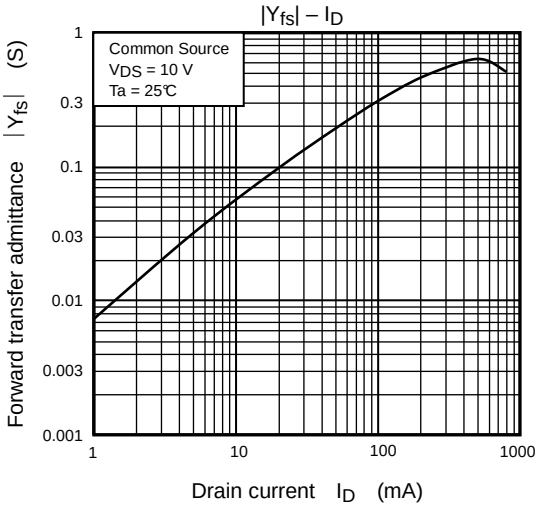


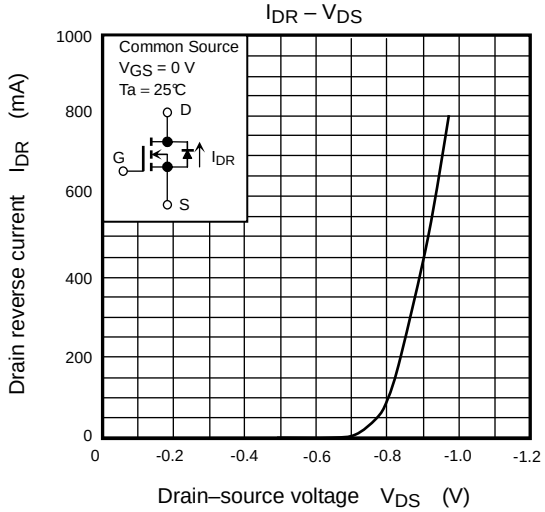
$R_{DS\ (ON)} - Ta$

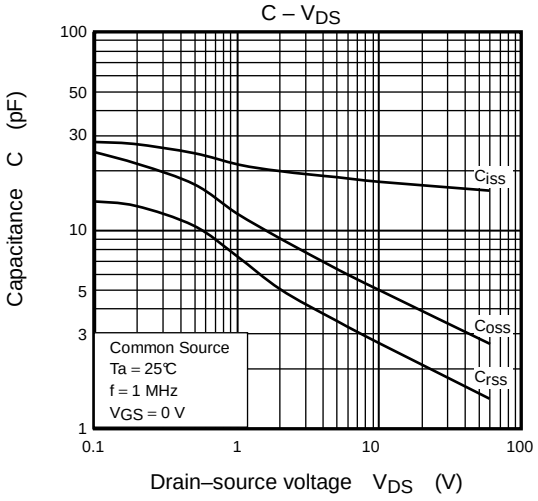


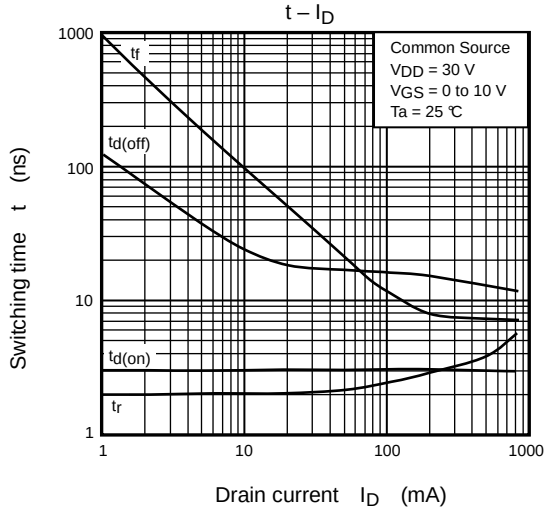
$V_{th} - Ta$

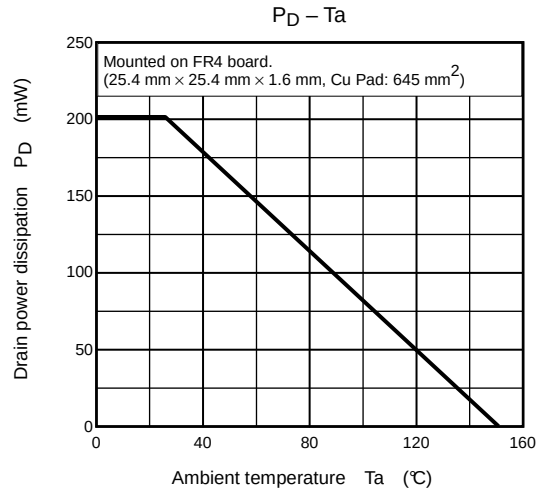



|Yfs| – ID
Common Source
VDS = 10 V
Ta = 25℃
Forward transfer admittance |Yfs| (S)
1
0.3
0.1
0.03
0.01
0.003
0.001
1
10
100
1000
Drain current ID (mA)


IDR – VDS
Common Source
VGS = 0 V
Ta = 25℃
D
G
IDR
S
Drain reverse current IDR (mA)
1000
800
600
400
200
0
0
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
Drain–source voltage VDS (V)


C – VDS
Capacitance C (pF)
100
50
30
10
5
3
1
Ciss
Coss
Crss
Common Source
Ta = 25℃
f = 1 MHz
VGS = 0 V
0.1
1
10
100
Drain–source voltage VDS (V)


t – ID
Common Source
VDD = 30 V
VGS = 0 to 10 V
Ta = 25 ℃
tf
td(off)
td(on)
tr
Switching time t (ns)
1000
100
10
1
1
10
100
1000
Drain current ID (mA)


PD – Ta
Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm2)
Drain power dissipation PD (mW)
250
200
150
100
50
0
0
40
80
120
160
Ambient temperature Ta (℃)

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