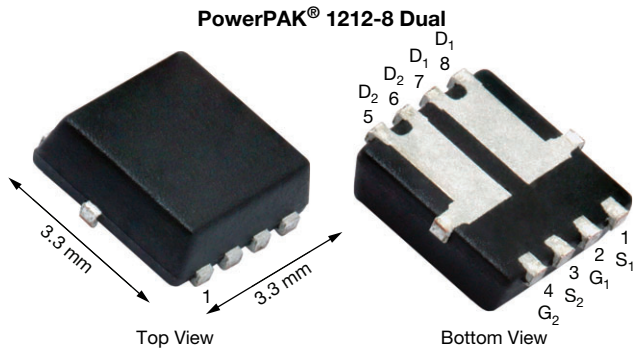


N-Channel 30 V (D-S) MOSFET



| PRODUCT SUMMARY | |
|--|-------------------|
| V_{DS} (V) | 30 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V | 0.022 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5$ V | 0.026 |
| Q_g typ. (nC) | 9.2 |
| I_D (A) | 6 ^{a, g} |
| Configuration | Dual |

FEATURES

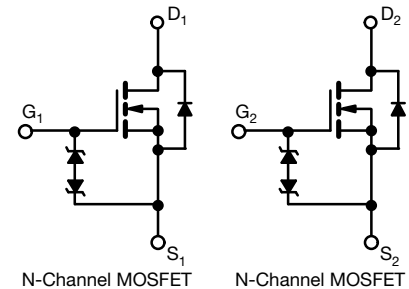
- TrenchFET® power MOSFET
- Typical ESD (HBM): 1900 V
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- DC/DC converters
- H-bridge
- Load switch
- Battery protection



| ORDERING INFORMATION | |
|---------------------------------|------------------|
| Package | PowerPAK 1212-8 |
| Lead (Pb)-free and halogen-free | SiS932EDN-T1-GE3 |

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted) | | | | |
|---|----------------|---------------|---------------------|---|
| PARAMETER | SYMBOL | LIMIT | UNIT | |
| Drain-source voltage | V_{DS} | 30 | V | |
| Gate-source voltage | V_{GS} | ± 12 | V | |
| Continuous drain current ($T_J = 150$ °C) | I_D | $T_C = 25$ °C | 6 ^a | A |
| | | $T_C = 70$ °C | 6 ^a | |
| | | $T_A = 25$ °C | 6 ^{b, c} | |
| | | $T_A = 70$ °C | 6 ^{b, c} | |
| Pulsed drain current ($t = 100$ μ s) | I_{DM} | 40 | A | |
| Continuous source-drain diode current | I_S | $T_C = 25$ °C | 6 ^a | A |
| | | $T_A = 25$ °C | 2.2 ^{b, c} | |
| Single pulse avalanche current | I_{AS} | 15 | A | |
| Single pulse avalanche energy | E_{AS} | 11.3 | mJ | |
| Maximum power dissipation | P_D | $T_C = 25$ °C | 23 | W |
| | | $T_C = 70$ °C | 14.8 | |
| | | $T_A = 25$ °C | 2.6 ^{b, c} | |
| | | $T_A = 70$ °C | 1.7 ^{b, c} | |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +150 | °C | |
| Soldering recommendations (peak temperature) ^c | | 260 | °C | |

| THERMAL RESISTANCE RATINGS | | | | |
|--|------------|---------|---------|------|
| PARAMETER | SYMBOL | TYPICAL | MAXIMUM | UNIT |
| Maximum junction-to-ambient ^b | R_{thJA} | 38 | 48 | °C/W |
| Maximum junction-to-case (drain) | R_{thJC} | 4.3 | 5.4 | |

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 94 °C/W
- $T_C = 25$ °C

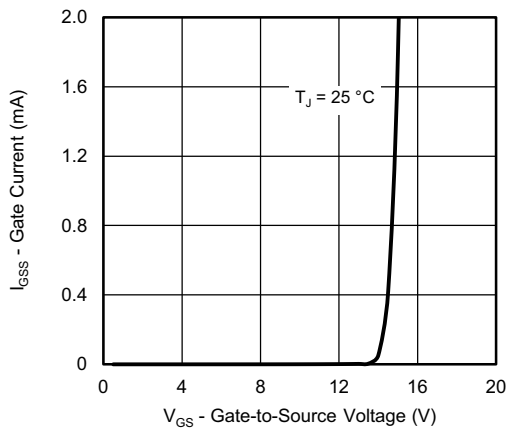
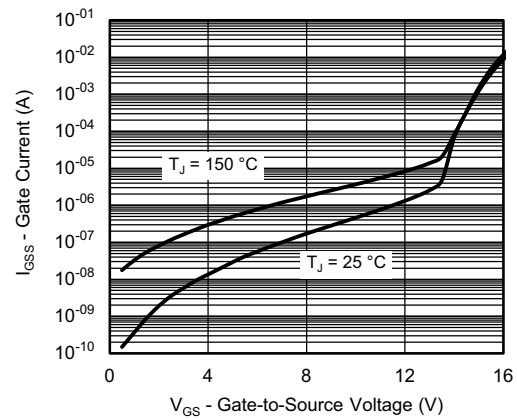
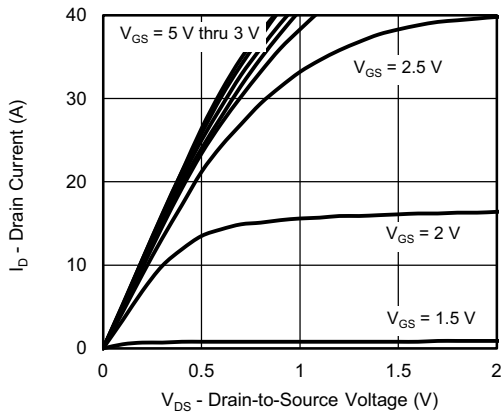
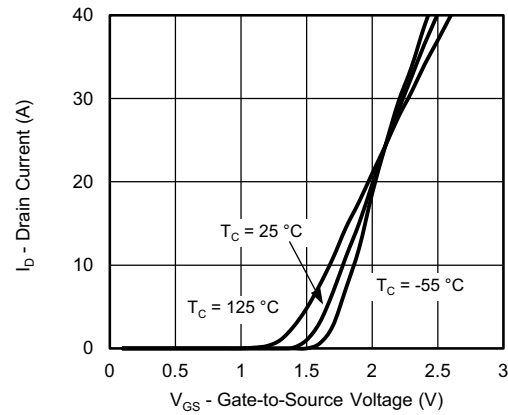
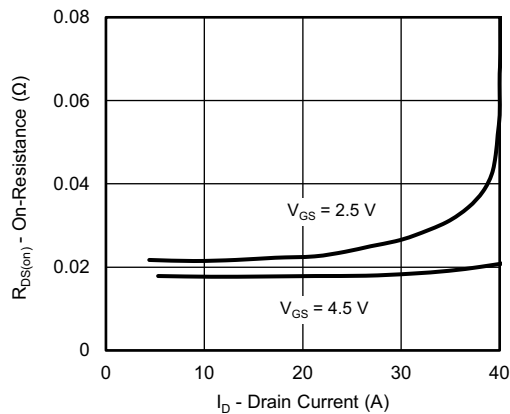
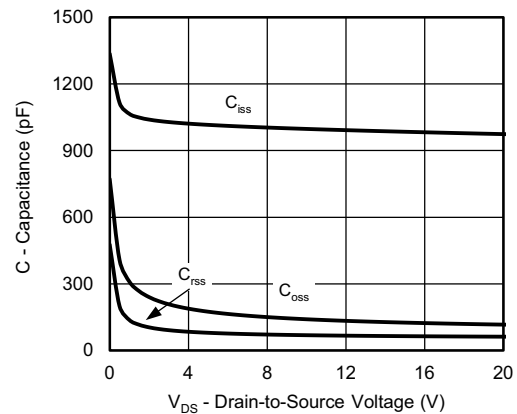


| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | |
|---|--------------------------------------|---|------|-------|-------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-source breakdown voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | 30 | - | - | V |
| V _{DS} temperature coefficient | ΔV _{DS} /T _J | I _D = 250 μA | - | 32 | - | mV/°C |
| V _{GS(th)} temperature coefficient | ΔV _{GS(th)} /T _J | I _D = 250 μA | - | -3.8 | - | |
| Gate-source threshold voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 0.6 | - | 1.4 | V |
| Gate-source leakage | I _{GSS} | V _{DS} = 0 V, V _{GS} = ± 12 | - | - | 15 | μA |
| Zero gate voltage drain current | I _{DSS} | V _{DS} = 30 V, V _{GS} = 0 V | - | - | 1 | |
| | | V _{DS} = 30 V, V _{GS} = 0 V, T _J = 70 °C | - | - | 10 | |
| On-state drain current ^a | I _{D(on)} | V _{DS} ≥ 5 V, V _{GS} = 4.5 V | 5 | - | - | A |
| Drain-source on-state resistance ^a | R _{DS(on)} | V _{GS} = 4.5 V, I _D = 10 A | - | 0.018 | 0.022 | Ω |
| | | V _{GS} = 2.5 V, I _D = 5 A | - | 0.021 | 0.026 | |
| Forward transconductance ^a | g _{fs} | V _{DS} = 5 V, I _D = 10 A | - | 45 | - | S |
| Dynamic ^b | | | | | | |
| Input capacitance | C _{ISS} | V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz | - | 1000 | - | pF |
| Output capacitance | C _{OSS} | | - | 125 | - | |
| Reverse transfer capacitance | C _{RSS} | | - | 66 | - | |
| Total gate charge | Q _g | V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 5 A | - | 9.2 | 14 | nC |
| Gate-source charge | Q _{gs} | | - | 1.9 | - | |
| Gate-drain charge | Q _{gd} | | - | 2 | - | |
| Gate resistance | R _g | f = 1 MHz | 0.6 | 3.1 | 6.2 | Ω |
| Turn-on delay time | t _{d(on)} | V _{DD} = 15 V, R _L = 3 Ω, I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω | - | 15 | 30 | ns |
| Rise time | t _r | | - | 35 | 70 | |
| Turn-off delay time | t _{d(off)} | | - | 32 | 60 | |
| Fall time | t _f | | - | 5 | 10 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous source-drain diode current | I _S | T _C = 25 °C | - | - | 6 | A |
| Pulse diode forward current | I _{SM} | | - | - | 40 | |
| Body diode voltage | V _{SD} | I _S = 5 A, V _{GS} = 0 V | - | 0.84 | 1.2 | V |
| Body diode reverse recovery time | t _{rr} | I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C | - | 15 | 30 | ns |
| Body diode reverse recovery charge | Q _{rr} | | - | 8 | 20 | nC |
| Reverse recovery fall time | t _a | | - | 10 | - | ns |
| Reverse recovery rise time | t _b | | - | 5 | - | |

Notes

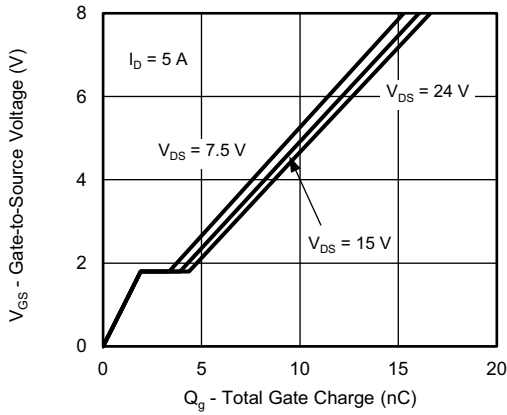
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

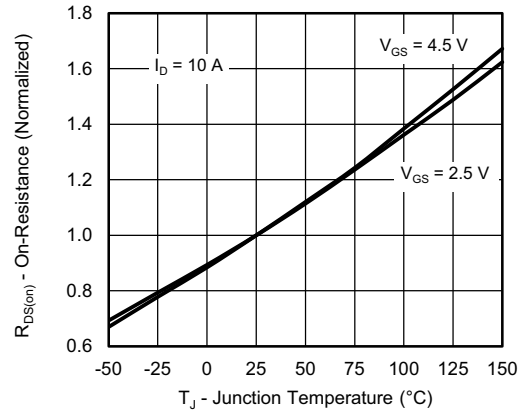
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Current vs. Gate-to-Source Voltage

Gate Current vs. Gate-to-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance



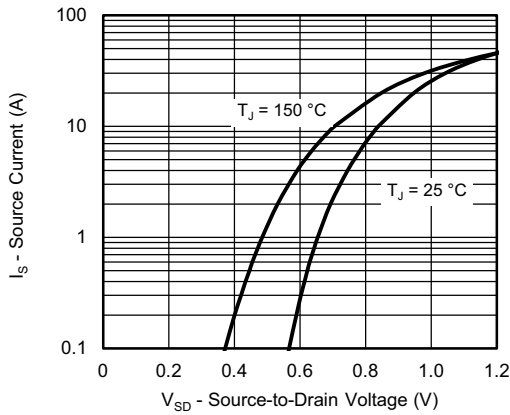
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



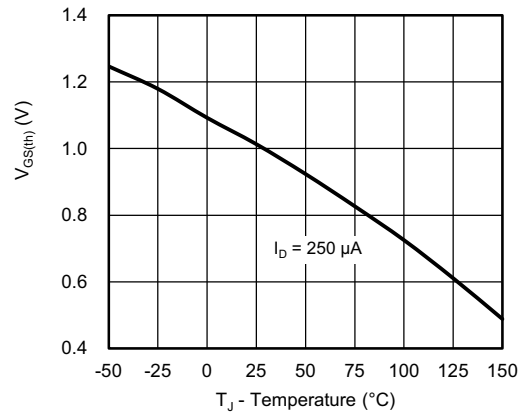
Gate Charge



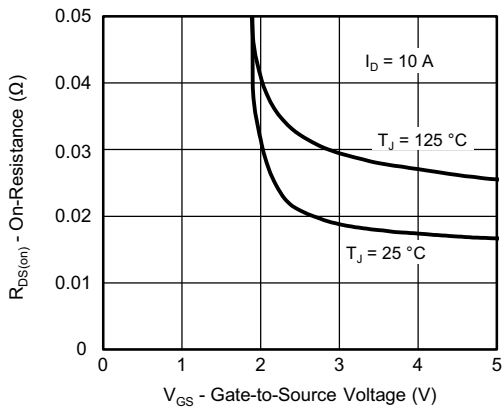
On-Resistance vs. Junction Temperature



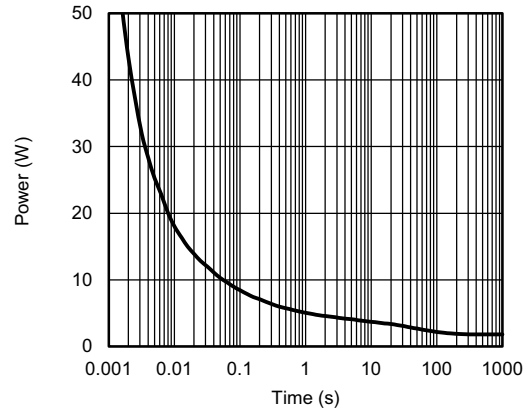
Source-Drain Diode Forward Voltage



Threshold Voltage



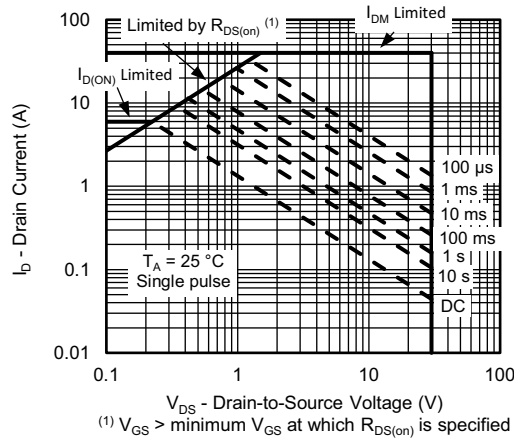
On-Resistance vs. Gate-to-Source Voltage



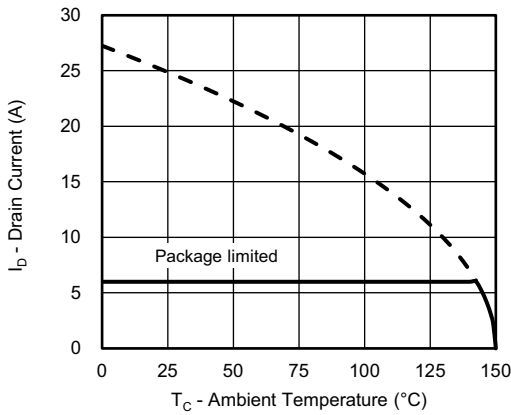
Single Pulse Power, Junction-to-Ambient



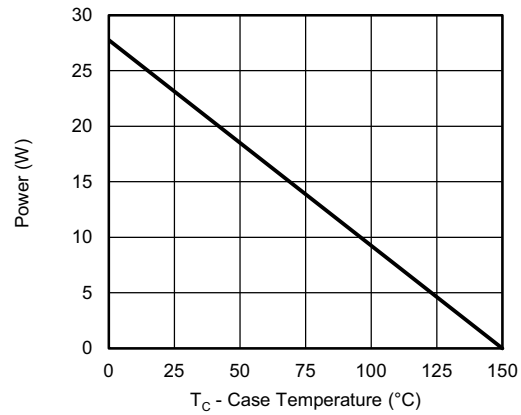
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating ^a



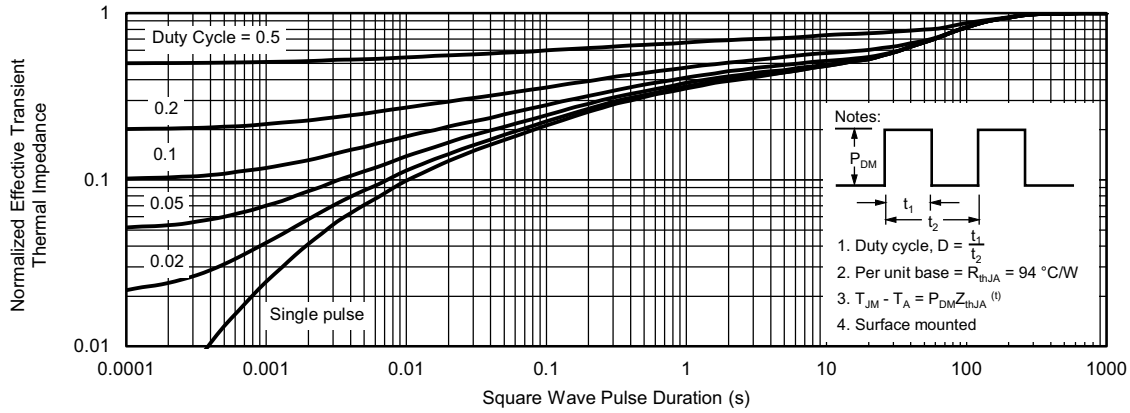
Power, Junction-to-Case

Note

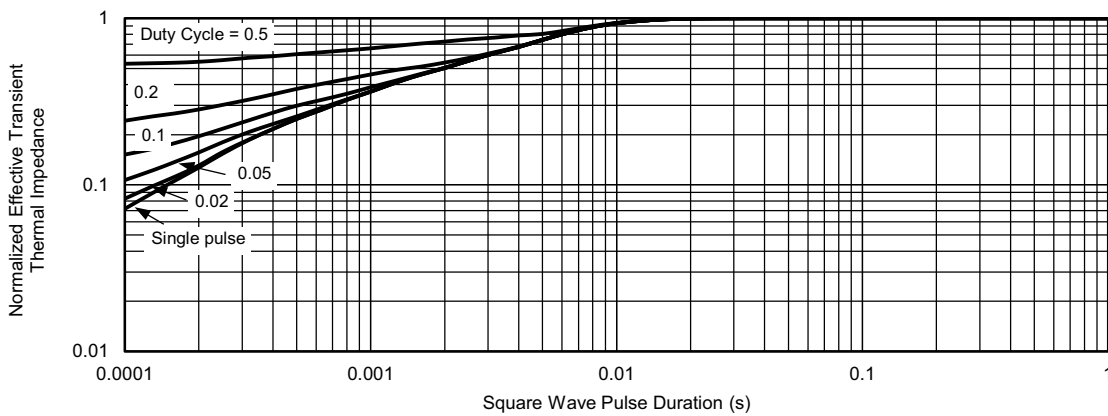
- a. The power dissipation P_D is based on $T_J \text{ max.} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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