SY88063AL

3.3V, 12.5Gbps Limiting Post Amplifier with Automatic Digital Offset Correction

General Description

The SY88063AL is a multi-rate limiting post amplifier designed for fiber-optic transceivers applications up to 12.5Gbps. It features an automatic digital offset correction function. The offset correction feature will automatically counteract any inherent offset present in the input signal and amplifier. The highly sensitive SY88063AL can amplify input signals as low as 20mVpp at 12.5Gbps or 10mVpp at 10.3Gbps to differential CML output levels.

The SY88063AL generates a loss-of-signal (LOS) open-collector TTL output. A programmable loss-of-signal level set pin (LOSLVL) sets the sensitivity of the input amplitude detection. LOS asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. The enable input (/EN) de-asserts the true output signal without removing the input signal. The LOS output can be fed back to the /EN input to implement the squelch function that maintains output stability under a loss-of-signal condition.

The SY88063AL operates from a single +3.3V power supply, over –40°C to +85°C, and is available in 3mm x 3mm 16-pin QFN package.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Up to 12.5Gbps operation
- Automatic Digital Offset Correction
- Programmable LOS level (LOSLVL)
- Squelching function to maintain output stability
- Low-noise CML data outputs
- TTL /EN input
- –40°C to +85°C Operation
- Small 3mm x 3mm QFN package

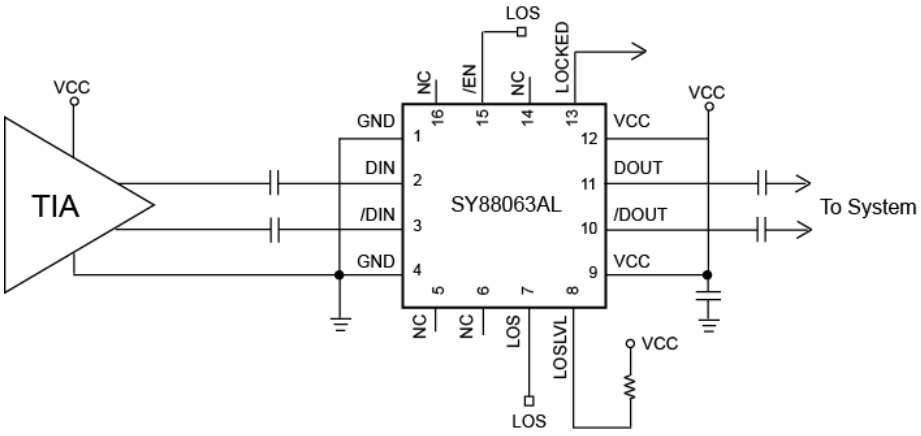
Applications

- 1x/2x/4x/8x Fibre Channel
- SR/LR SFP+ Optical Transceiver
- 10GPON ONU
- SONET/SDH:OC192 – STM64

Markets

- Datacom/telecom
- Optical transceiver

Typical Application



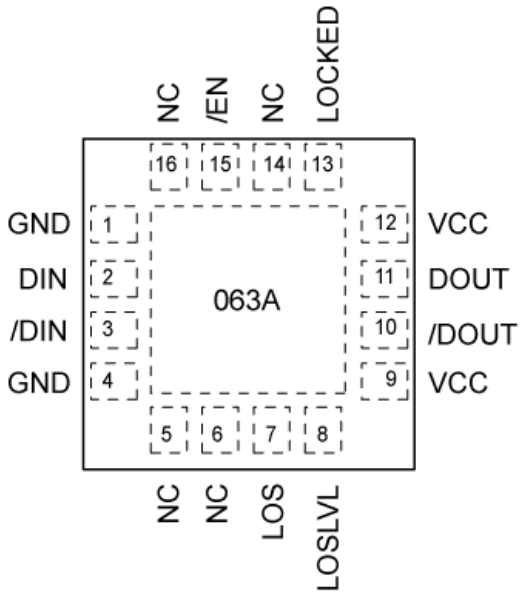
Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY88063ALMG	Lead-Free QFN-16	Industrial	063A with Pb-Free Bar Line Indicator
SY88063ALMG TR[(1)]	Lead-Free QFN-16	Industrial	063A with Pb-Free Bar Line Indicator

Note:

1. Tape and Reel.

Pin Configuration



3mm x 3mm QFN-16

Pin Description

Pin Number	Pin Name	Type	Pin Function
2, 3	DIN, /DIN	Data Input	Differential data inputs. Each input is internally terminated to approximately VCC – 1.3V by a 50Ω resistor. AC-Couple input signals.
5, 6, 14, 16	NC	No Connection	Unused Pins. Leave open.
7	LOS	Open-Collector TTL Output	Loss-of-Signal: Asserts HIGH when the data input amplitude falls below the threshold set by LOSLVL.
8	LOSLVL	DC Input	Loss-of-Signal Level Set. A resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which LOS will be asserted.
10, 11	/DOUT, DOUT	CML Output	Differential Data Outputs. Unused output should be terminated 50Ω-to-V_{CC}.

Pin Description (Continued)

Pin Number	Pin Name	Type	Pin Function
13	LOCKED	LVTTL Output	Once digital offset correction is locked based input signal, this pin will output a LVTTL HIGH.
15	/EN	LVTTL Input	/Enable: This input enables the outputs when it is LOW. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
1, 4	GND	Ground	Device Ground. Exposed pad must be soldered (or equivalent) to the same potential as the ground pins.
9, 12	V_{CC}	Power Supply	Positive Power Supply. Bypass with 0.1µF | | 0.01µF low ESR capacitors. 0.01µF capacitors should be as close as possible to V_{CC} pins.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... 0V to +4.0V
Input Voltage (DIN, /DIN) ..... 0 to V_{CC}
Output Current (I_{OUT}) ..... ±25mA
EN Voltage ..... 0 to V_{CC}
LOS_{LVL} Voltage ..... V_{CC}-1.3V to V_{CC}
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
QFN
(θ_{JA}) Still-air ..... 60°C/W
(ψ_{JB}) ..... 33°C/W

DC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power Supply Current	With 50Ω Output Load		53	72	mA
LOS_{LVL}	LOS_{LVL} Voltage		V_{CC} –1.3		V_{CC}	V
V_{OH}	DOUT, /DOUT HIGH Voltage		V_{CC} – 0.020	V_{CC} – 0.005	V_{CC}	V
V_{OL}	DOUT, /DOUT LOW Voltage		V_{CC} – 0.400	V_{CC} – 0.350	V_{CC} –0.300	V
Z_0	Single-Ended Output Impedance		45	50	55	Ω
Z_I	Single-Ended Input Impedance		45	50	55	Ω

TTL DC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	/EN Input HIGH Voltage		2.0			V
V_{IL}	/EN Input LOW Voltage				0.8	V
I_{IH}	/EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA
I_{IL}	/EN Input LOW Current	V_{IN} = 0.5V	–0.3			mA
V_{OH}	LOS Output HIGH Level	Sourcing 100µA	2.4			V
V_{OL}	LOS Output LOW Level	Sinking 2mA			0.5	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. ψ_{JB} uses a 4-layer and θ_{JA} in still air unless otherwise stated.

AC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; R_{Load} = 50Ω to V_{CC}; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{IN}	Input Data Rate	NRZ Data	1.25		12.5	Gbps
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 4		25	35	ps
t_{JITTER}	Deterministic Random	Note 5 Note 6		10 1		ps_{PP} ps_{RMS}
V_{ID}	Differential Input Voltage Swing	F_{IN} = 12.5Gbps	20		1800	mV_{PP}
		F_{IN} = 10.3Gbps	10			
V_{OD}	Differential Output Voltage Swing	Note 4	600	700	800	mV_{PP}
T_{OFF}	LOS Release Time	Note 9		100	500	ns
T_{ON}	LOS Assert Time	Note 9		100	500	ns
LOS_{AL}	Low LOS Assert Level	R_{LOSLVL} = 10kΩ, Note 7	9	11	13	mV_{PP}
LOS_{DL}	Low LOS De-Assert Level	R_{LOSLVL} = 10kΩ, Note 7	14	16	19	mV_{PP}
HSY_L	Low LOS Hysteresis	R_{LOSLVL} = 10kΩ, Note 8	2	3.5	4	dB
LOS_{AM}	Medium LOS Assert Level	R_{LOSLVL} = 5kΩ, Note 7	16	18	21	mV_{PP}
LOS_{DM}	Medium LOS De-Assert Level	R_{LOSLVL} = 5kΩ, Note 7	23	26	29	mV_{PP}
HSY_M	Medium LOS Hysteresis	R_{LOSLVL} = 5kΩ, Note 8	2	3	4	dB
LOS_{AH}	High LOS Assert Level	R_{LOSLVL} = 100Ω, Note 7	40	46	54	mV_{PP}
LOS_{DH}	High LOS De-Assert Level	R_{LOSLVL} = 100Ω, Note 7	61	68	74	mV_{PP}
HSY_H	High LOS Hysteresis	R_{LOSLVL} = 100Ω, Note 8	2	3	4	dB
B_{-3dB}	3dB Bandwidth			10		GHz
$A_{V(Diff)}$	Differential Voltage Gain			38		dB
S_{21}	Single-Ended Small-Signal Gain		26	32		dB

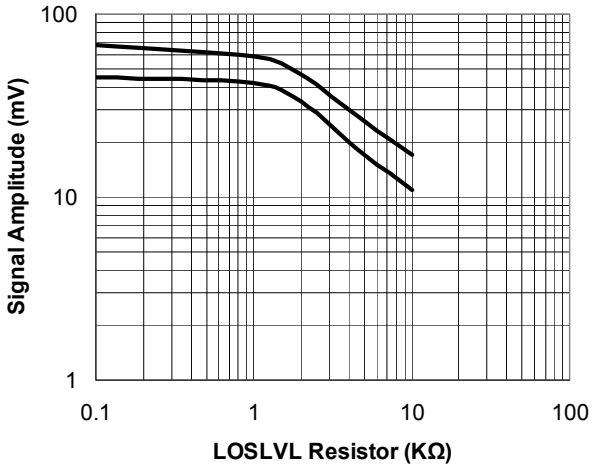
Notes:

4. Amplifier in limiting mode. Input is a 200MHz square wave.
5. Deterministic jitter measured using 10 Gbps K28.5 pattern, V_{ID} = 60mV_{PP}.
6. Random jitter measured using 10Gbps K28.7 pattern, V_{ID} = 60mV_{PP}.
7. See “Typical Operating Characteristics” for a graph showing how to choose a particular R_{LOSLVL} for a particular LOS assert and its associated de-assert amplitude.
8. This specification defines electrical hysteresis as 20log (LOS De-Assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based on that ratio, the optical hysteresis corresponding to the electrical hysteresis range 1dB-4.5 dB, shown in the AC characteristics table, will be 0.5dB-3dB Optical Hysteresis.
9. In real world applications, the LOS Release/Assert time can be strongly influenced by the RC time constant of the AC-coupling cap and the 50Ω input termination. To keep this time low, use a decoupling cap with the lowest value that is allowed by the data rate and the number of consecutive identical bits in the application (typical values are in the range of 0.001µF to 1.0µF).

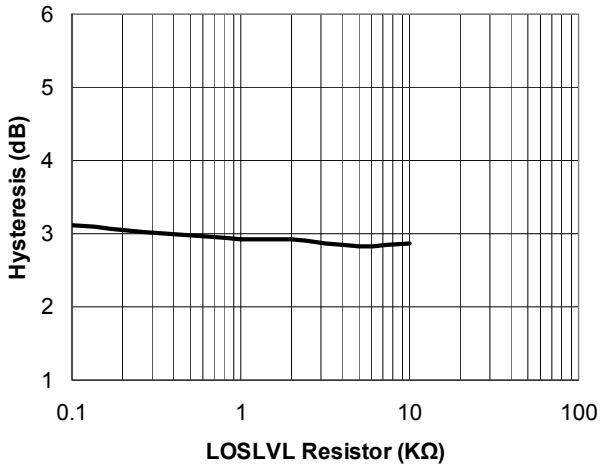
Typical Operating Characteristics

V_{CC} = 3.3V, T_A = 25°C, R_L = 50Ω to V_{CC}-2V, unless otherwise stated.

LOS Assert/De-Assert Levels



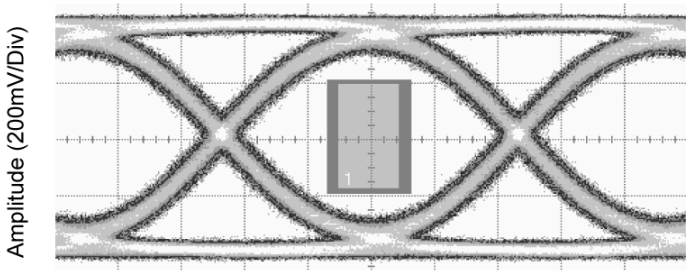
LOS Hysteresis



Typical Functional Characteristics

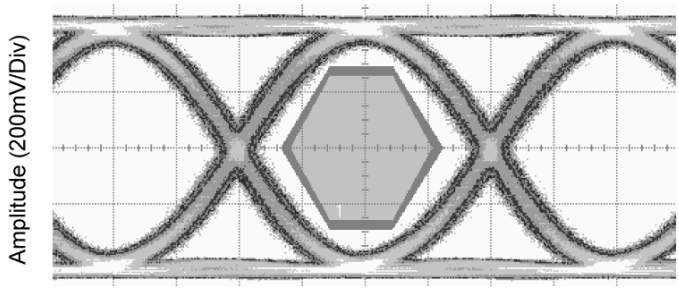
V_{CC} = 3.3V, T_A = 25°C, R_L = 50Ω to V_{CC}-2V, unless otherwise stated.

PRBS-23 Pattern @ 10.7Gbps, 10mVpp Input



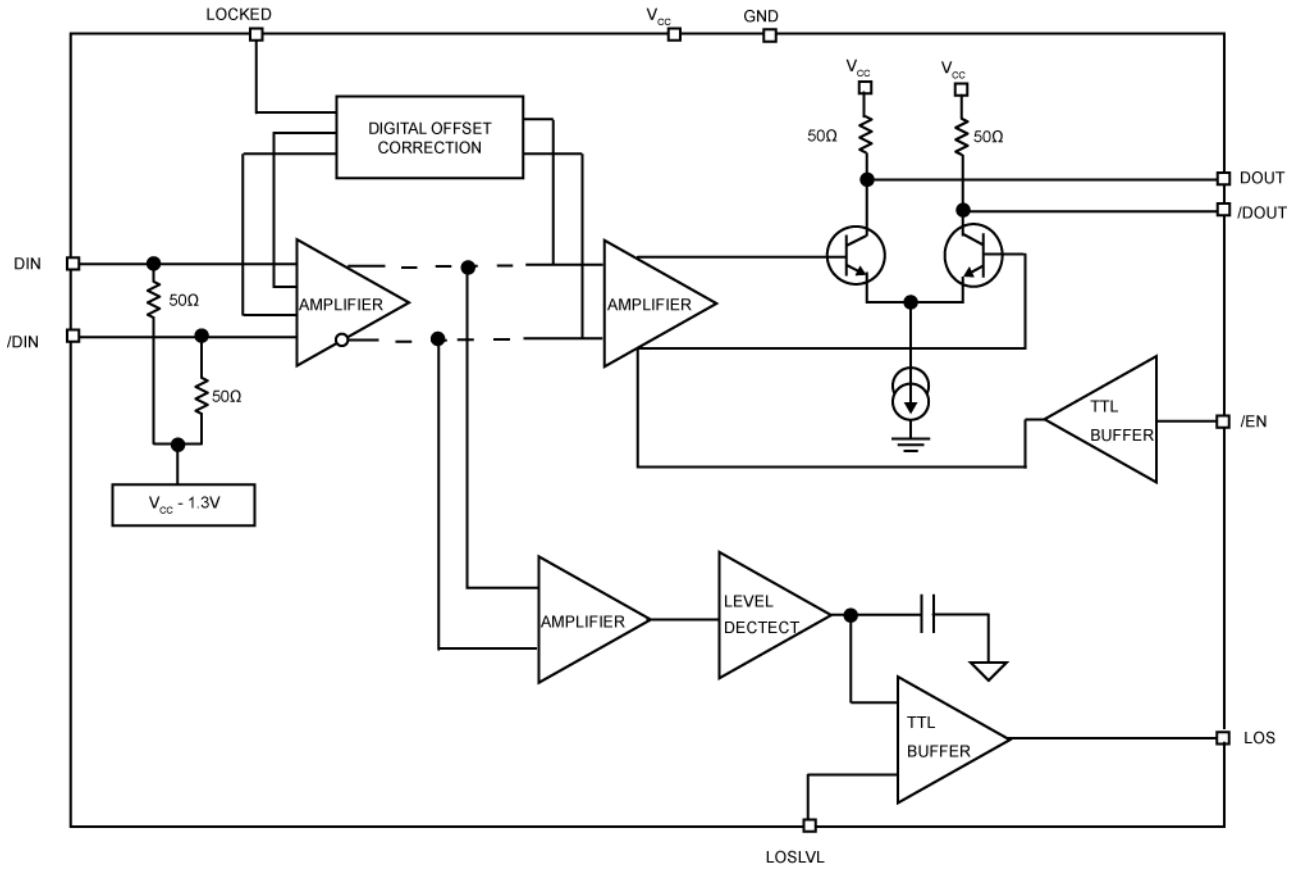
Time (20ps/Div)

PRBS-23 Pattern @ 12.5Gbps, 20mVpp Input



Time (20ps/Div)

Functional Block Diagram



Detailed Description

The SY88063AL is a high-sensitivity limiting post amplifier that operates from a single +3.3V power supply over temperatures from –40°C to +85°C. The SY88063AL can process input signals up to 12.5Gbps and as small as 20mV$_{pp}$. It can also process signals as small as 10mV$_{pp}$ with data rates as high as 10.7Gbps. Figure 1 shows the acceptable input ranges. The SY88063AL generates a LOS output signal that can be fed back to /EN for output stability in the absence of a signal at the input. LOSLVL sets the sensitivity of the input amplitude detection. By adjusting the voltage at the LOSLVL pin, either through an external voltage source or a resistor, the SY88063AL can trigger LOS on signals from 10mVpp to 70mVpp.

Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the input stage. The high-sensitivity of the input amplifier allows signals as small as 10mV$_{pp}$ to be detected and amplified. The input amplifier allows input signals as large as 1800mV$_{pp}$. Input signals are amplified with a typically 38dB differential voltage gain. Since it is a limiting amplifier, the SY88063AL outputs typically 700mV$_{pp}$ voltage-limited waveforms for input signals that are greater than 7mV$_{pp}$.

Output Buffer

The SY88063AL's CML output buffer is designed to drive 50Ω lines and is internally terminated with 50Ω to VCC. Figure 3 shows a schematic of the output stage.

Loss-of-Signal (LOS)

The SY88063AL generates a chatter-free loss-of-signal (LOS) open-collector TTL output as shown in Figure 4. LOS is used to determine if the input amplitude is too small to be considered as a valid input. LOS asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. LOS can be fed back to the enable (/EN) input to maintain output stability under a loss of signal condition. /EN de-asserts low the true output signal without removing the input signals. Typically, 3dB LOS hysteresis is provided to prevent chattering.

LOS-Level Set

A programmable LOS level set pin (LOSLVL) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and LOSLVL sets the voltage at LOSLVL. This voltage ranges from V_{CC} to V_{CC}-1.3V. The external resistor creates a voltage divider between V_{CC} and V_{CC}-1.3V, as shown in Figure 5.

Hysteresis

The SY88063AL provides typically 3dB LOS electrical hysteresis, which is defined as 20log (VINLOS-Assert / VINLOS-De-Assert). Since the relationship between the voltage out of the ROSA to optical power at its input is linear, the optical hysteresis will be typically half of the electrical hysteresis reported in the datasheet, but in practice the ratio between electrical and optical hysteresis is found to be within the range 1.5-1.8.

Digital Offset Correction

The SY88063AL features automatic digital offset correction function. The conventional analog offset correction is susceptible to offset drift from long input patterns of exclusively 0s or 1s. The SY88063AL is not limited by the input patterns. This feature will automatically detect any existing offset and lock the offset correction. The offset correction will not be applied to large input signals that place the outputs into limiting mode.

Timing Diagram

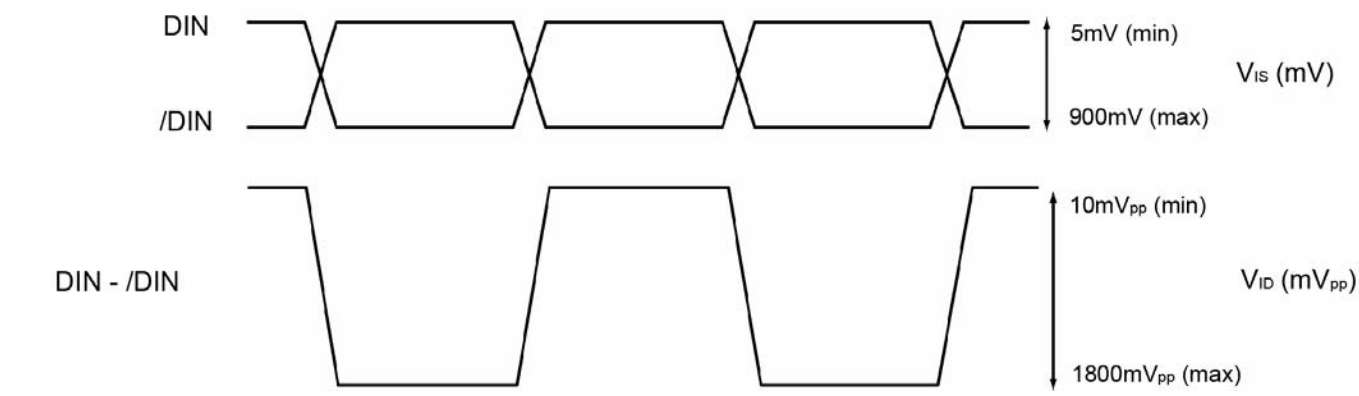


Figure 1. V_{IS} and V_{ID} Definition

Structure Recommendations

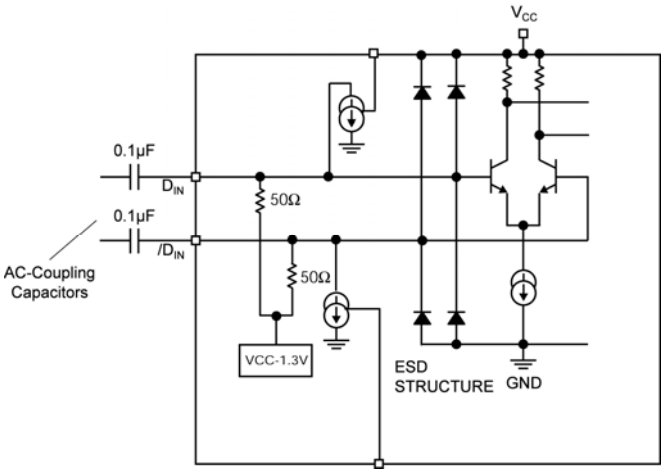


Figure 2. Simplified Input Structure

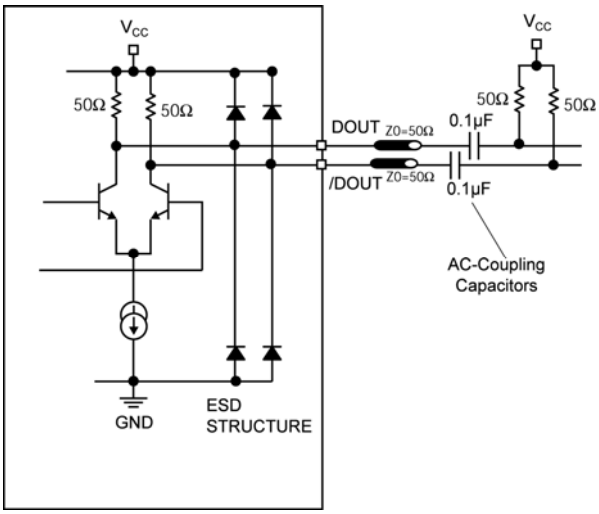


Figure 3. Simplified Output Structure

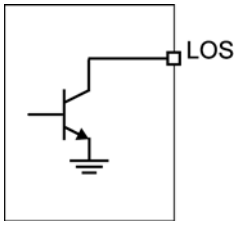


Figure 4. LOS Output Structure

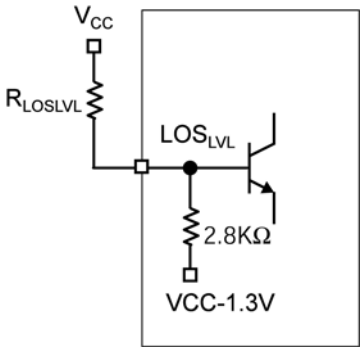
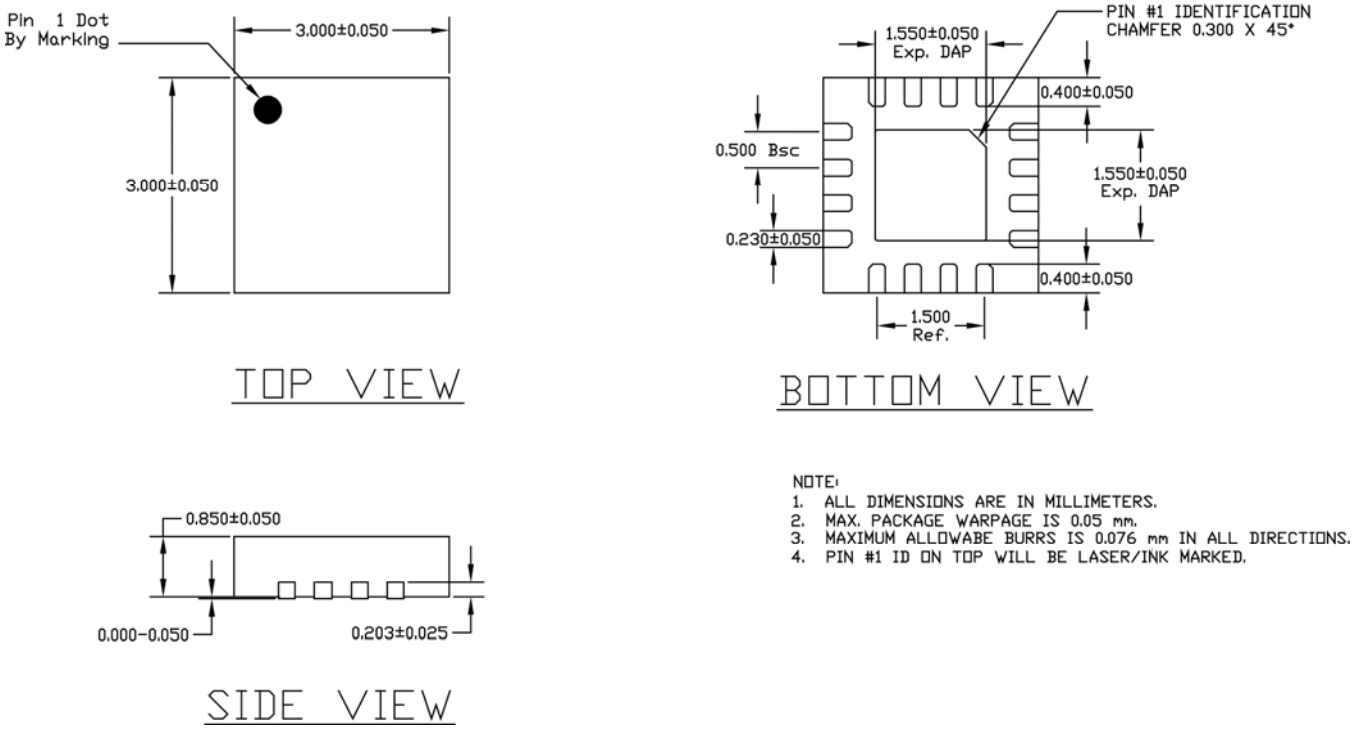


Figure 5. LOS_{LVL} Setting Circuit

Package Information



16-Pin (3mm × 3mm) QFN

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