SD56150

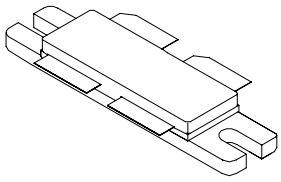
RF power transistor
the LdmoST family

Features

- Excellent thermal stability
- Common source configuration Push-pull
- P_{OUT} = 150W with 13dB gain @ 860MHz / 32V
- BeO free package
- Internal input matching
- In compliance with the 2002/95/EC european directive

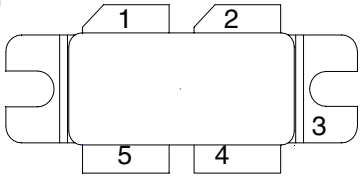
Description

The SD56150 is a common source N-channel enhancement-mode lateral Field-Effect RF power transistor designed for broadband commercial and industrial applications at frequencies up to 1.0 GHz. The SD56150 is designed for high gain and broadband performance operating in common source mode at 32 V. Its internal matching makes it ideal for TV broadcast applications requiring high linearity.



M252
Epoxy sealed

Figure 1. Pin connection



1. Drain
2. Drain
3. Source
4. Gate
5. Gate

Table 1. Device summary

Order code	Package	Branding
SD56150	M252	SD56150

Contents

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings (T_{CASE} = 25°C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Voltage	65	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current	17	A
P_{DISS}	Power Dissipation (@ Tc = 70°C)	236	W
Tj	Max. Operating Junction Temperature	200	°C
T_{STG}	Storage Temperature	-65 to +150	°C

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.55	°C/W

2 Electrical characteristics

T_{CASE} = +25 °C

2.1 Static

Table 4. Static (per section)

Symbol	Test conditions			Min	Typ	Max	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V	I_{DS} = 10 mA		65			V
I_{DSS}	V_{GS} = 0 V	V_{DS} = 28 V				1	µA
I_{GSS}	V_{GS} = 20 V	V_{DS} = 0 V				1	µA
$V_{GS(Q)}$	V_{DS} = 28 V	I_D = 100 mA		2.0		5.0	V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 3 A			0.5	0.8	V
G_{FS}	V_{DS} = 10 V	I_D = 3 A		2.5		4	mho
C_{ISS}(1)	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		255		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		50		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		2.9		pF

1. Includes Internal Input Moscap.

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions			Min	Typ	Max	Unit
P_{OUT}	V_{DD} = 32 V	I_{DQ} = 500 mA	f = 860MHz	150			W
G_{PS}	V_{DD} = 32 V	I_{DQ} = 500 mA	P_{OUT} = 150 W,f = 860MHz	13	16.5		dB
h_D	V_{DD} = 32 V	I_{DQ} = 500 mA	P_{OUT} = 150 W,f = 860MHz	50	60		%
Load mismatch	V_{DD} = 32 V All phase angles	I_{DQ} = 500 mA	P_{OUT} = 150 W,f = 860MHz	10:1			VSWR

3 Impedance

Figure 2. Current conventions

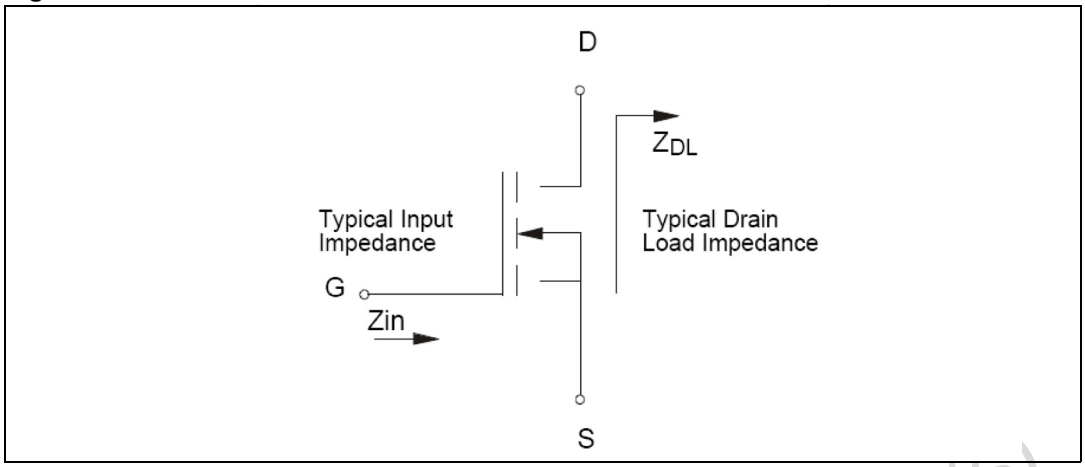


Table 6. Impedance data

Freq. (MHz)	Z_{IN} (Ω)	Z_{DL}(Ω)
860 MHz	4.7 - j 5.5	3.6 + j 6.5
880 MHz	4.3 - j 6.9	3.9 + j 7.4
900 MHz	4.5 - j 8.8	4.4 + j 7.8

Note: Measured drain to drain and gate to gate respectively.

4 Typical performance

Figure 3. Capacitance vs drain voltage

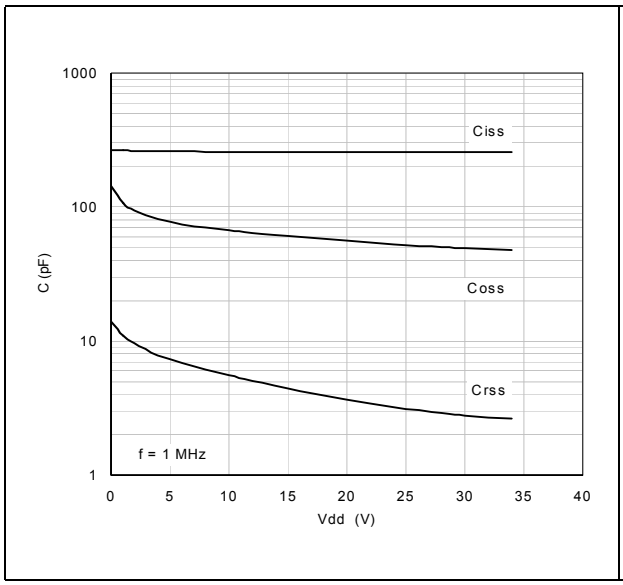


Figure 4. Gate-source voltage vs case temperature

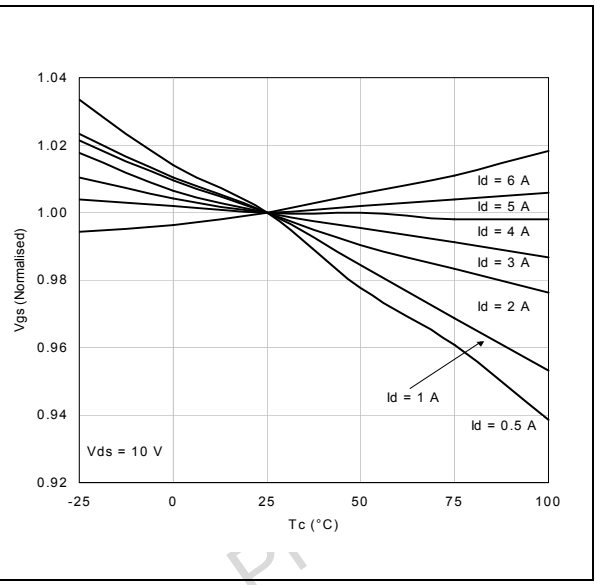


Figure 5. Drain current vs gate voltage

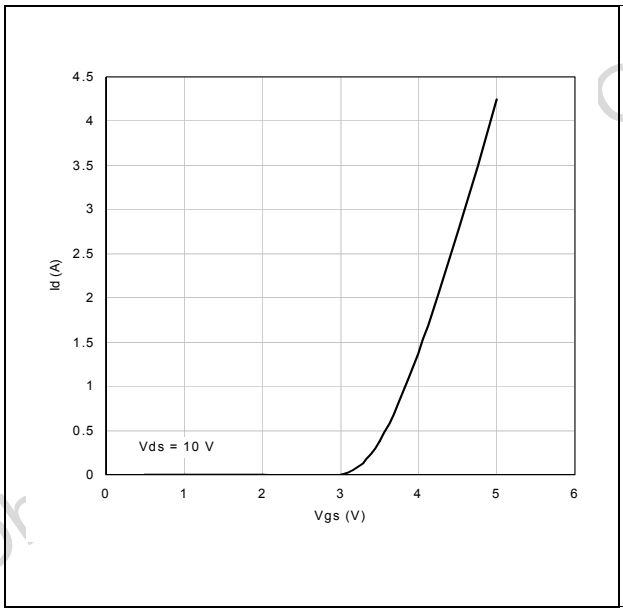


Figure 6. Output power vs input power

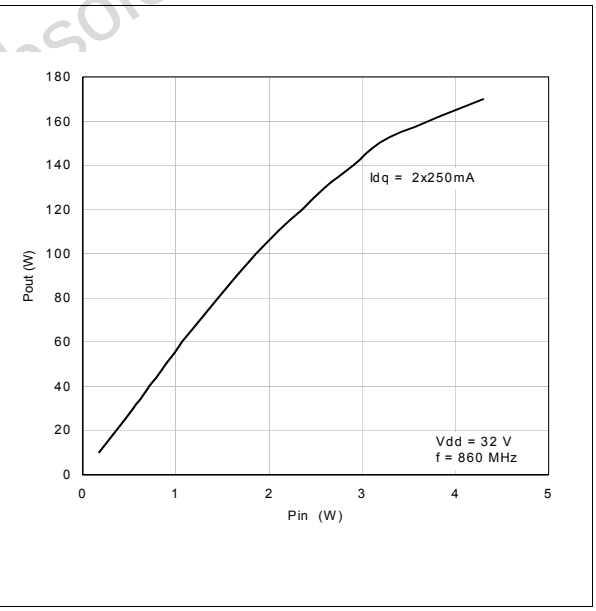


Figure 7. Power gain vs output power

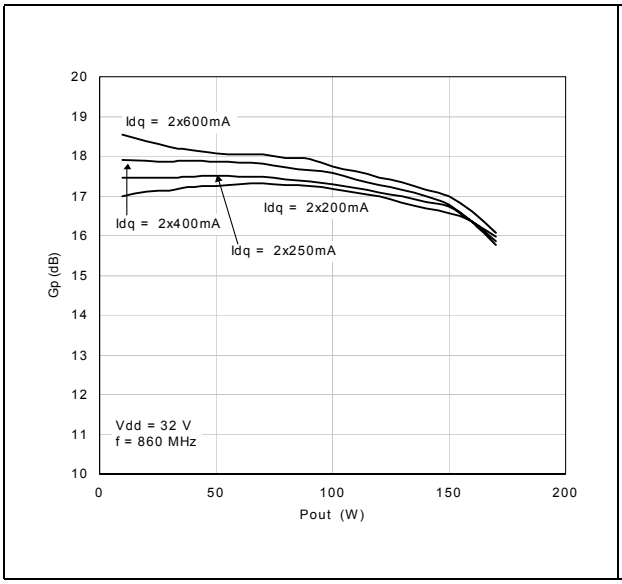


Figure 8. Efficiency vs output power

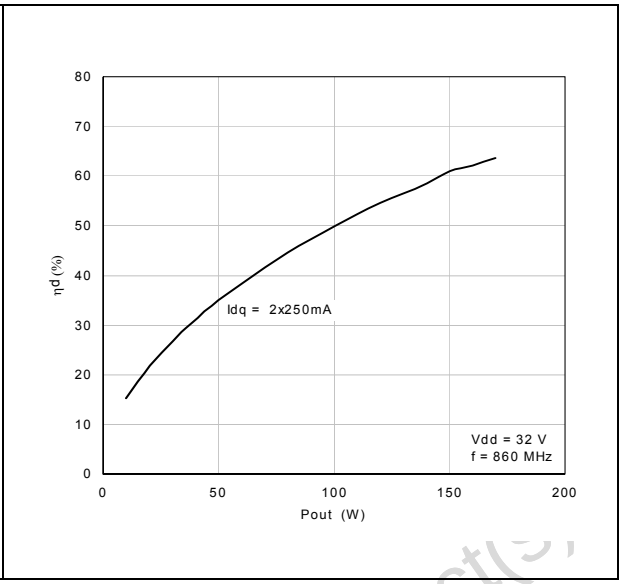


Figure 9. Output power vs supply voltage

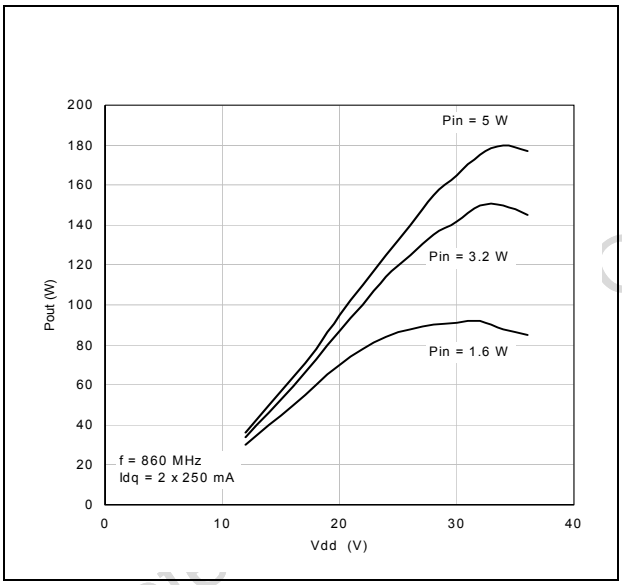


Figure 10. Efficiency vs supply voltage

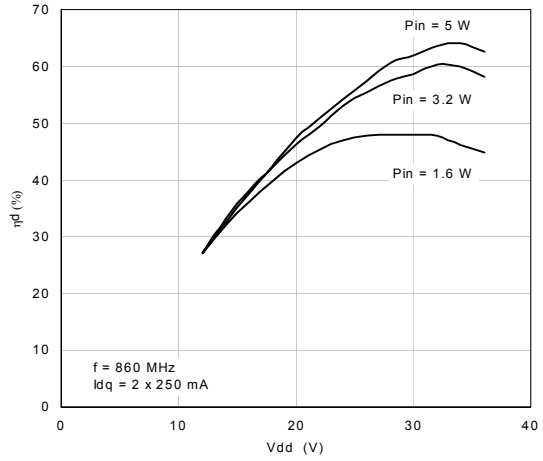


Figure 11. Intermodulation distorsion vs output power

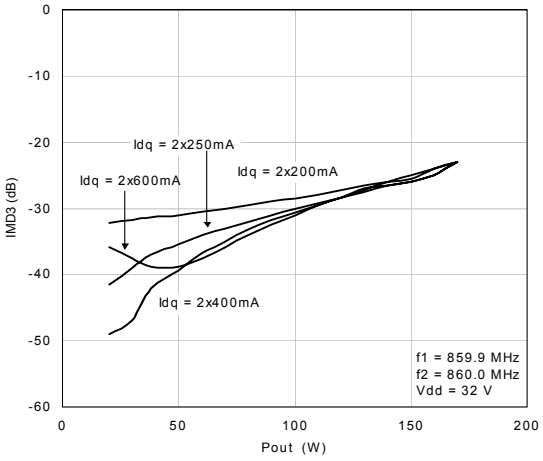
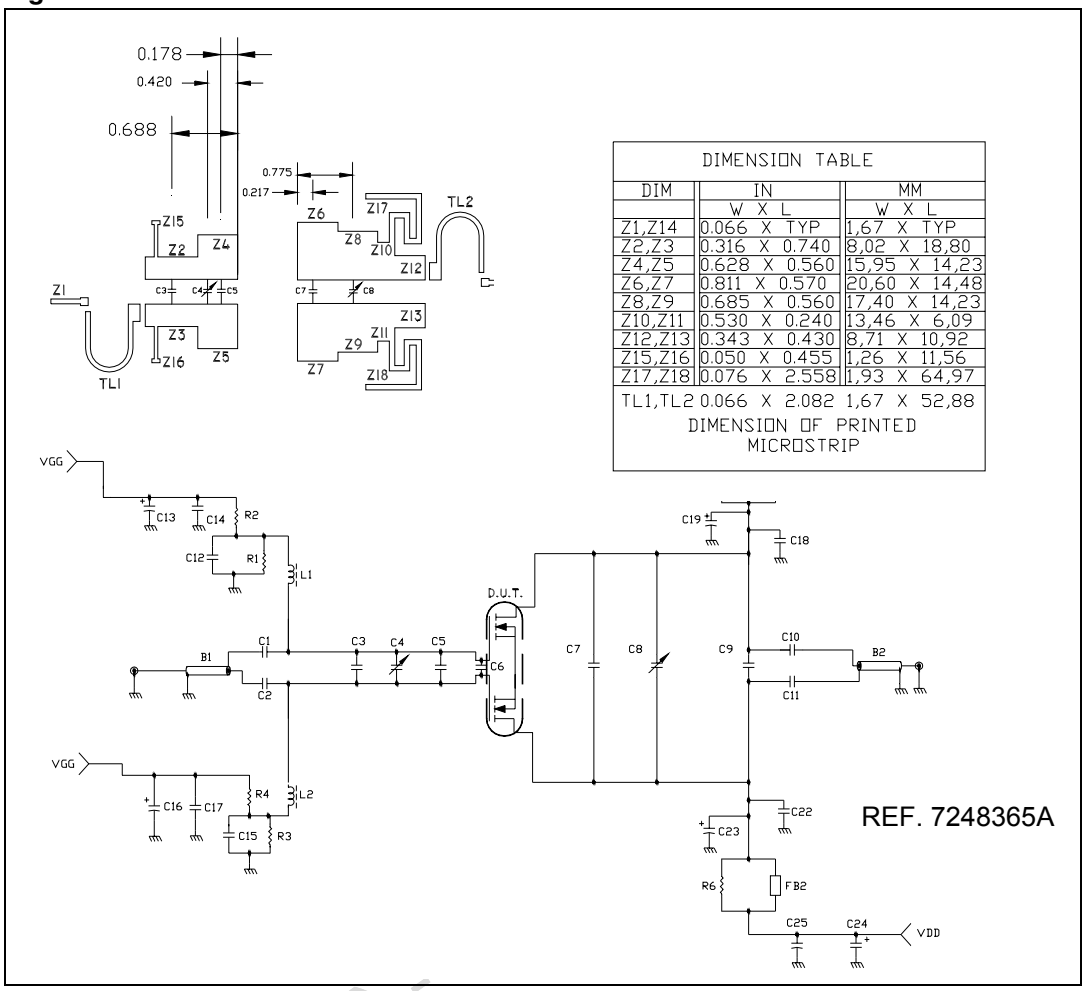


Figure 12. Test circuit schematic



1 *Gap between ground & transmission line = 0.056 [1.42] +0.002 [0.05] -0.000 [0.00] Typ.*

2 *2. C3 and C4 adjacent to each other*

Table 7. Test circuit component part list

Component	Description
C1,C2, C10, C11	51 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C3	9.1 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C4, C8	0.6 - 4.5 pF GIGATRIM VARIABLE CAPACITOR
C5	10 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C6	4.7 pF ATC 100A SURFACE MOUNT CERAMIC CHIP CAPACITOR
C7	13 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C9	6.2 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C12, C15, C18, C22	91 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C13, C16, C20, C24	10 μF 50V ALUMINUM ELECTROLYTIC RADIAL LEAD CAPACITOR
C14, C17, C21, C25	0.1 μF 500V SURFACE MOUNT CERAMIC CHIP CAPACITOR
C19, C23	100 μF 63V ALUMINUM ELECTROLYTIC RADIAL LEAD CAPACITOR
R1, R2, R3, R4	200 OHM 1/4 W SURFACE MOUNT CHIP RESISTOR
R5, R6	1.8 OHM 1/4 W SURFACE MOUNT CHIP RESISTOR
L1, L2	CHIP INDUCTOR 10 nH SURFACE MOUNT COIL
FB1, FB2	SURFACE MOUNT EMI SHIELD BEAD
B2, B1	BALUN, 25 OHM, SEMI-RIDGE OD 0.141 2.365 LG COAXIAL CABLE OR EQUIVALENT
PCB	WOVEN GLASS REINFORCED / CERAMIC FILLED 0.030” THK εr = 3.48, 2 Oz ED CU BOTH SIDES

Figure 13. Test fixture

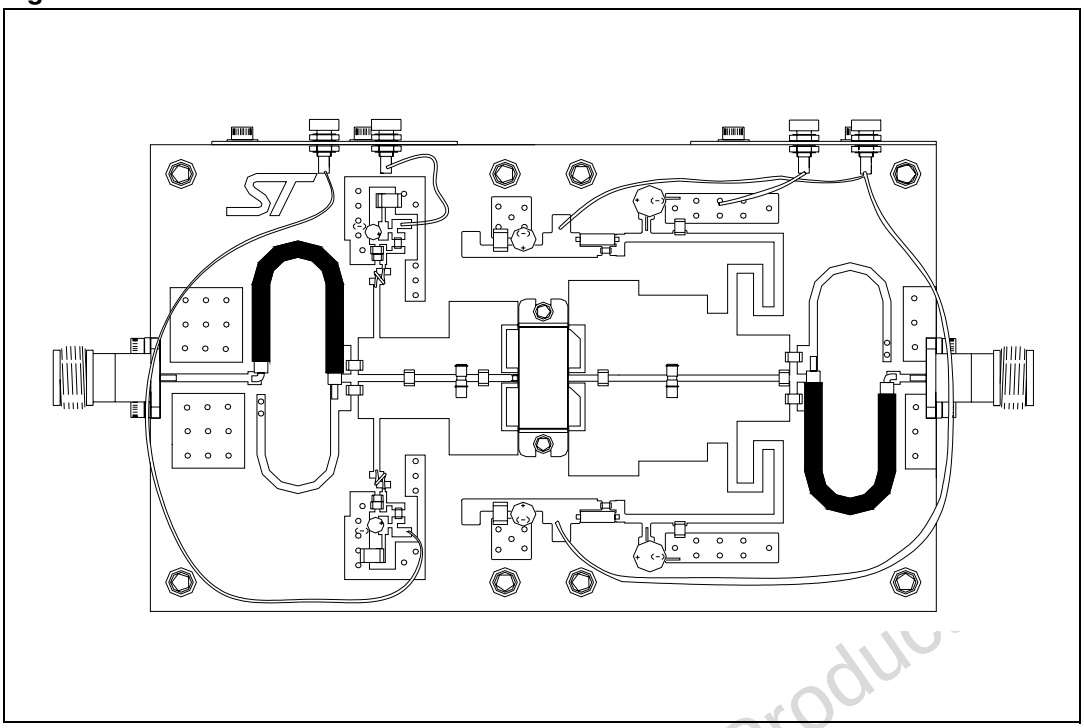
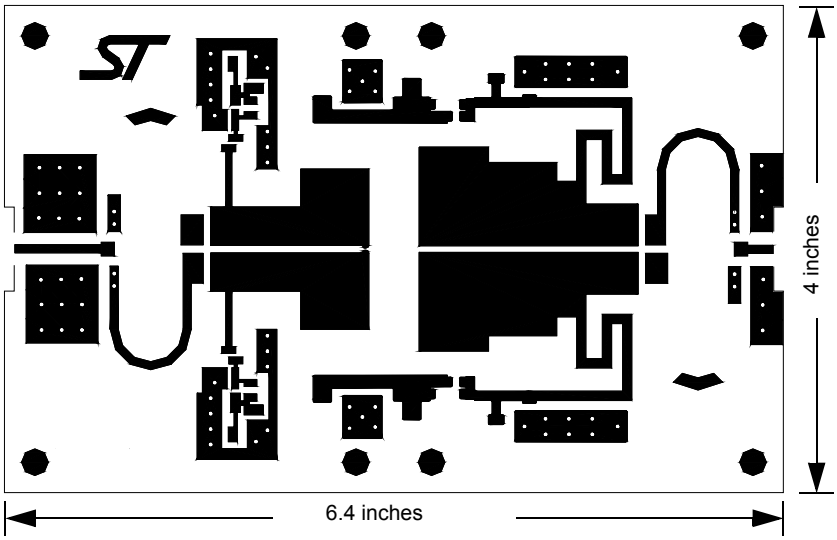


Figure 14. Test circuit photomaster

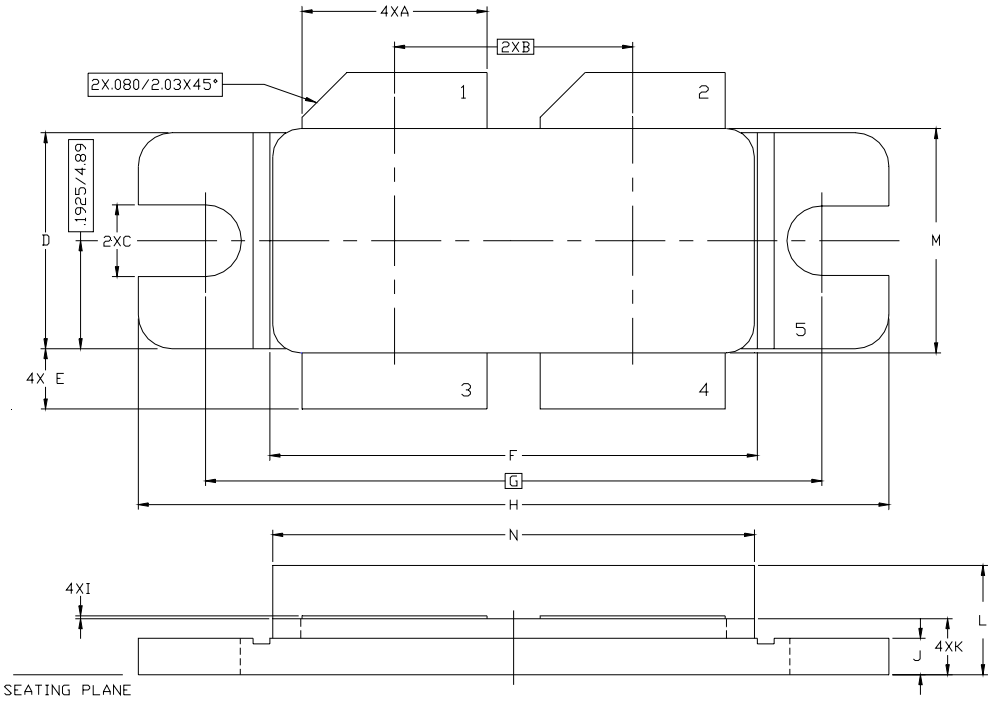


5 Package mechanical data

Table 8. M252 (.400 x .860 4L BAL N/HERM W/FLG) mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	8.13		8.64	.320		.340
B		10.80			.425	
C	3.00		3.30	.118		.130
D	9.65		9.91	.380		.390
E	2.16		2.92	.085		.115
F	21.97		22.23	.865		.875
G		27.94			1.100	
H	33.91		34.16	1.335		1.345
I	0.10		0.15	.004		.006
J	1.52		1.78	.060		.070
K	2.36		2.74	.093		.108
L	4.57		5.33	.180		.210
M	9.96		10.34	.392		.407
N	21.64		22.05	.852		.868

Figure 15. Package dimensions



Controlling dimension: Inches

Ref. 7145054A

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Sep-2003	5	First Issue
23-Jul-2007	6	Document reformatted, added lead free info
24-Aug-2007	7	Cover page title updated

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