SL23EP09

Low Jitter and Skew 10 to 220 MHz Zero Delay Buffer (ZDB)

Key Features

- 10 to 220 MHz operating frequency range
- Low output clock skew: 45ps-typ
- Low output clock jitter:
  - 50 ps-typ cycle-to-cycle jitter
  - 20 ps-typ period jitter
- Low part-to-part output skew: 90 ps-typ
- Wide 2.5 V to 3.3 V power supply range
- Low power dissipation:
  - 26 mA-max at 66 MHz and VDD=3.3 V
  - 24 mA-max at 66 MHz and VDD=2.5V
- One input drives 9 outputs organized as 4+4+1
- Select mode to bypass PLL or tri-state outputs
- SpreadThru™ PLL that allows use of SSCG
- Standard and High-Drive options
- Available in 16-pin SOIC and TSSOP packages
- Available in Commercial and Industrial grades

Applications

- Printers, MFPs and Digital Copiers
- PCs and Work Stations
- Routers, Switchers and Servers
- Digital Embeded Systems

Description

The SL23EP09 is a low skew, low jitter and low power Zero Delay Buffer (ZDB) designed to produce up to nine (9) clock outputs from one (1) reference input clock, for high speed clock distribution applications.

The product has an on-chip PLL which locks to the input clock at CLKIN and receives its feedback internally from the CLKOUT pin.

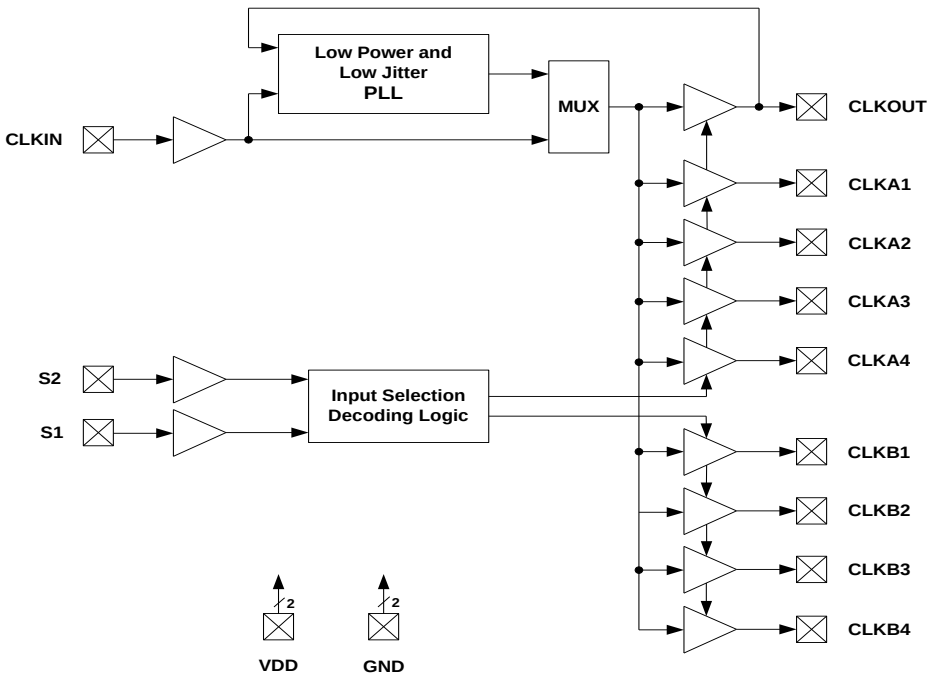
The SL23EP09 has two (2) clock driver banks each with four (4) clock outputs. These outputs are controlled by two (2) select input pins S1 and S2. When only four (4) outputs are needed, four (4) bank-B output clock buffers can be tri-stated to reduce power dissipation and jitter. The select inputs can also be used to tri-state both banks A and B or drive them directly from the input bypassing the PLL and making the product behave like a Non-Zero Delay Buffer (NZDB).

The high-drive version operates up to 220MHz and 200MHz at 3.3V and 2.5V power supplies respectively.

Benefits

- Up to nine (9) distribution of input clock
- Standard and High-Dirive levels to control impedance level, frequency range and EMI
- Low power dissipation, jitter and skew
- Low cost

Block Diagram



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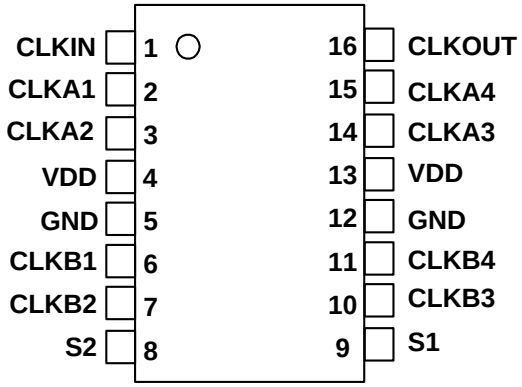
Pin Configuration



16-Pin SOIC and TSSOP

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Reference Frequency Clock Input. Weak pull-down (250kΩ).
2	CLKA1	Output	Buffered Clock Output, Bank A. Weak pull-down (250kΩ).
3	CLKA2	Output	Buffered Clock Output, Bank A. Weak pull-down (250kΩ).
4	VDD	Power	3.3V or 2.5V Power Supply.
5	GND	Power	Power Ground.
6	CLKB1	Output	Buffered Clock Output, Bank B. Weak pull-down (250kΩ).
7	CLKB2	Output	Buffered Clock Output, Bank B. Weak pull-down (250kΩ).
8	S2	Input	Select Input, select pin S2. Weak pull-up (250kΩ).
9	S1	Input	Select Input, select pin S1. Weak pull-up (250kΩ).
10	CLKB3	Output	Buffered Clock Output, Bank B. Weak pull-down (250kΩ).
11	CLKB4	Output	Buffered Clock Output, Bank B. Weak pull-down (250kΩ).
12	GND	Power	Power Ground.
13	VDD	Power	3.3V or 2.5V Power Supply.
14	CLKA3	Output	Buffered Clock Output, Bank A. Weak pull-down (250kΩ).
15	CLKA4	Output	Buffered Clock Output, Bank A. Weak pull-down (250kΩ).
16	CLKOUT	Output	Buffered Clock Output, PLL Internal Feedback Output. Weak pull-down (250kΩ).

General Description

The SL23EP09 is a low skew, low jitter Zero Delay Buffer with very low operating current.

The product includes an on-chip high performance PLL that locks into the input reference clock and produces nine (9) output clock drivers tracking the input reference clock for systems requiring clock distribution.

in addition to CLKOUT that is used for internal PLL feedback, there are two (2) banks with four (4) outputs in each bank, bringing the number of total available output clocks to nine (9).

Input and output Frequency Range

The input and output frequency range is the same. But, it depends on VDD and drive levels as given in the below Table 1.

VDD(V)	Drive	Min(MHz)	Max(MHz)
3.3	HIGH	10	220
3.3	STD	10	200
2.5	HIGH	10	180
2.5	STD	10	167

Table 1. Input/Output Frequency Range

If the input clock frequency is DC (GND to VDD), this is detected by an input frequency detection circuitry and all nine (9) clock outputs are forced to Hi-Z. The PLL is shutdown to save power. In this shutdown state, the product draws less than 12 µA supply current.

SpreadThru™ Feature

If a Spread Spectrum Clock (SSC) were to be used as an input clock, the SL23EP09 is designed to pass the modulated Spread Spectrum Clock (SSC) signal from its reference input to the output clocks. The same spread characteristics at the input are passed through the PLL and drivers without any degradation in spread percent (%), spread profile and modulation frequency

Select Input Control

The SL23EP09 provides two (2) input select control pins called S1 and S2. This feature enables users to selects various states of output clock banks-A and bank-B, output source and PLL shutdown features as shown in the Table 2.

The S1 (Pin-9) and S2 (Pin-8) inputs include 250 kΩ weak pull-up resistors to VDD.

PLL Bypass Mode

If the S2 and S1 pins are logic High(1) and Low(0) respectively, the on-chip PLL is shutdown and bypassed, and all the nine output clocks bank A, bank B and CLKOUT clocks are driven directly from the reference input clock. In this operation mode SL23EP09 works like a non-ZDB fanout buffer.

High and Low-Drive Product Options

The SL23EP09 is offered with High-Drive "-1H" and Standard-Drive "-1" options. These drive options enable the users to control load levels, frequency range and EMI control. Refer to the AC electrical tables for the details.

Skew and Zero Delay

All outputs should drive the similar load to achieve output-to-output skew and input-to-output specifications given in the AC electrical tables. However, Zero delay between input and outputs can be adjusted by changing the loading of CLKOUT relative to the banks A and B clocks since CLKOUT is the feedback to the PLL.

Power Supply Range (VDD)

The SL23EP09 is designed to operate in a wide power supply range from 2.3V (Min) to 3.6V (Max). An internal on-chip voltage regulator is used to supply PLL constant power supply of 1.8V, leading to a consistent and stable PLL electrical performance in terms of skew, jitter and power dissipation. Contact SLI for 1.8V power supply version ZDB called SL23EPL09.

S2	S1	Clock A1-A4	Clock B1-4	CLKOUT	Output Source	PLL Status
0	0	Tri-state	Tri-state	Driven	PLL	On
0	1	Driven	Tri-state	Driven	PLL	On
1	0	Driven	Driven	Driven	Reference	Off
1	1	Driven	Driven	Driven	PLL	On

Table 2. Select Input Decoding

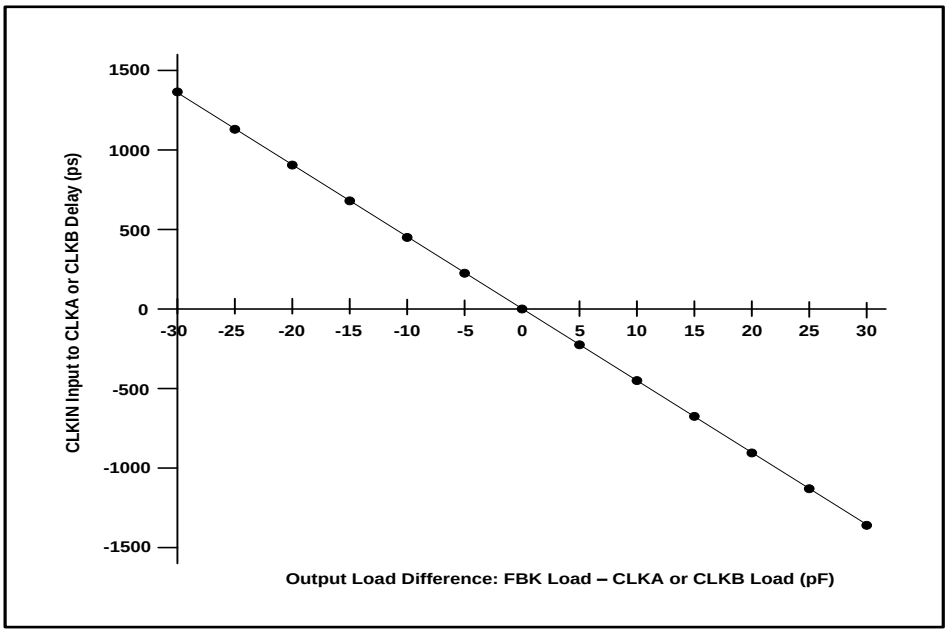


Figure 1. CLKIN Input to CLK A and B Delay
(In terms of load difference between CLKOUT and CLK A and B)

Absolute Maximum Ratings

Description	Condition	Min.	Max.	Unit
Supply voltage, VDD		– 0.5	4.6	V
All Inputs and Outputs		– 0.5	VDD+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	70	°C
Ambient Operating Temperature	In operation, I-Grade	– 40	85	°C
Storage Temperature	No power is applied	– 65	150	°C
Junction Temperature	In operation, power is applied	–	125	°C
Soldering Temperature		–	260	°C
ESD Rating (Human Body Model)	JEDECCC22-A114D	-4000	4000	V
ESD Rating (Change Device Model)	JEDECCC22-C101C	-1500	1500	V
ESD Rating (Machine Model)	JEDECCC22-A115D	-200	200	V

Operating Conditions: Unless Otherwise Stated VDD=2.3V to 3.6V and for Both C and I Grades

Symbol	Description	Condition	Min.	Max.	Unit
VDD3.3	3.3V Supply Voltage	3.3V+/-10%	3.0	3.6	V
VDD2.5	2.5V Supply Voltage	2.5V+/-10%	2.3	2.7	V
TA	Operating Temperature(Ambient)	Commercial	0	70	°C
		Industrial	–40	85	°C
CLOAD	Load Capacitance	<220 MHz, 3.3V with High Drive	–	15	pF
		<200 MHz, 3.3V with Standard drive	–	15	pF
		<180 MHz, 2.5V with High Drive	–	15	pF
		<167 MHz, 2.5V with Standard drive	–	15	pF
		<200 MHz, 3.3V with High Drive	–	22	pF
		<180 MHz, 3.3V with Standard drive	–	22	pF
		<167 MHz, 2.5V with High Drive	–	22	pF
		<134 MHz, 2.5V with Standard drive	–	22	pF
		<133 MHz, 3.3V with High Drive	–	30	pF
		<100 MHz, 3.3V with Standard drive	–	30	pF
		<80 MHz, 2.5V with High Drive	–	30	pF
		<67 MHz, 2.5V with Standard drive	–	30	pF
CIN	Input Capacitance	S1, S2 and CLKIN pins	–	5	pF
RPU/D	Pull-up and Pull-down Resistors	Pins-12/3/6/7/8/9/10/11/14/15/16 250kΩ-typ	175	325	kΩ
CLBW	Closed-loop bandwidth	3.3V, (typical)	1.2		MHz
		2.5V, (typical)	0.8		MHz
ZOUT	Output Impedance	3.3V, (typical), High drive	29		Ω
		3.3V, (typical), Standard drive	41		Ω
		2.5V, (typical), High drive	37		Ω
		2.5V, (typical), Standard drive	41		Ω

DC Electrical Specifications (VDD=3.3V): Unless Otherwise Stated for Both C and I Grades

Symbol	Description	Condition	Min	Max	Unit
VDD	Supply Voltage		3.0	3.6	V
VIL	Input LOW Voltage		–	0.8	V
VIH	Input HIGH Voltage		2.0	VDD+0.3	V
IIL	Input Leakage Current	0 < VIN < 0.8V	–	±10	µA
IIH	Input HIGH Current	VIN = VDD	–	100	µA
VOL	Output LOW Voltage	IOL = 8 mA (standard drive)	–	0.4	V
		IOL = 12 mA (high drive)	–	0.4	V
VOH	Output HIGH Voltage	IOH = –8 mA (standard drive)	2.4	–	V
		IOH = –12 mA (high drive)	2.4	–	V
IDDPD	Power Down Supply Current CLKIN<2.0MHz	Measured at CLKIN = 0 MHz (C-Grade)	–	12	µA
		Measured at CLKIN = 0 MHz (I-Grade)	–	25	µA
IDD1	Power Supply Current	All Outputs CL=0, 66 MHz CLKIN	–	26	mA
IDD2	Power Supply Current	All Outputs CL=0, 133 MHz CLKIN	–	42	mA

DC Electrical Specifications (VDD=2.5V): Unless Otherwise Stated for Both C and I Grades

Symbol	Description	Condition	Min	Max	Unit
VDD	Supply Voltage		2.3	2.7	V
VIL	Input LOW Voltage		–	0.7	V
VIH	Input HIGH Voltage		1.7	VDD+ 0.3	V
IIL	Input Leakage Current	0<VIN < 0.8V	–	10	µA
IIH	Input HIGH Current	VIN = VDD	–	100	µA
VOL	Output LOW Voltage	IOL = 8 mA (standard drive)	–	0.5	V
		IOL = 12 mA (high drive)	–	0.5	V
VOH	Output HIGH Voltage	IOH = –8 mA (standard drive)	VDD – 0.6	–	V
		IOH = –12 mA (high drive)	VDD – 0.6	–	V
IDDPD	Power Down Supply Current CLKIN<2MHz	Measured at CLKIN = 0 MHz (C-Grade)	–	12	µA
		Measured at CLKIN = 0 MHz (I-Grade)	–	25	µA
IDD1	Power Supply Current	All Outputs CL=0, 66 MHz CLKIN	–	24	mA
IDD2	Power Supply Current	All Outputs CL=0, 133 MHz CLKIN	–	40	mA

AC Electrical Specifications (VDD=3.3V and 2.5V)

Symbol	Description	Condition	Min	Typ	Max	Unit
FMAX	Maximum Frequency [1] (Input=Output)	3.3V High Drive	10	–	220	MHz
		3.3V Standard Drive	10	–	200	MHz
		2.5V High Drive	10	–	180	MHz
		2.5V Standard Drive	10	–	167	MHz
INDC	Input Duty Cycle	<135 MHz, VDD=3.3V	25	–	75	%
		<135 MHz, VDD=2.5V	40	–	60	%
OUTDC	Output Duty Cycle[2]	<135 MHz, VDD=3.3V	45	–	55	%
		<135 MHz, VDD=2.5V	40		60	%
tr/f3.3	Rise, Fall Time (3.3V) [2] (Measured at: 0.8 to 2.0V)	High drive, CL = 15 pF, <135 MHz	–	–	0.75	ns
		Std drive, CL = 15 pF, <170 MHz	–	–	1.5	ns
		High drive, CL = 22 pF, <135 MHz	–	–	1.2	ns
		Std drive, CL = 22 pF, <135 MHz	–	–	1.6	ns
		High drive, CL = 30 pF, <100 MHz	–	–	1.5	ns
		Std drive, CL = 30 pF, >100 MHz	–	–	2.5	ns
tr/f2.5	Rise, Fall Time (2.5) [2] (Measured at: 0.6 to 1.8V)	High drive, CL = 15 pF, <135 MHz	–	–	1.5	ns
		Std drive, CL = 15 pF, <135 MHz	–	–	2.5	ns
		High drive, CL = 22 pF, <135 MHz	–	–	1.3	ns
		High drive, CL = 30 pF, >100 MHz	–	–	2.5	ns
t1	Output-to-Output Skew [9] (Measured at VDD/2)	All outputs CL=0, 3.3V supply, 2.5 power supply, standard drive	–	45	100	ps
		All outputs CL=0, 2.5V power supply, high drive	–	–	110	ps
t2	Delay Time, CLKIN Rising Edge to CLKOUT Rising Edge[2] (Measured at VDD/2)	PLL Bypass mode	1.5	–	4.4	ns
		PLL enabled @ 3.3V	–100	–	100	ps
		PLL enabled @2.5V	–200	–	200	ps
t3	Part-to-Part Skew[2] (Measured at VDD/2)	Measured at VDD/2. Any output to any output, 3.3V supply	–	–	±150	ps
		Measured at VDD/2. Any output to any output, 2.5V supply	–	–	±300	ps

Notes:

1. For the given maximum loading conditions. See CL in Operating Conditions Table.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

AC Electrical Specifications (VDD=3.3V and 2.5V) (cont.)

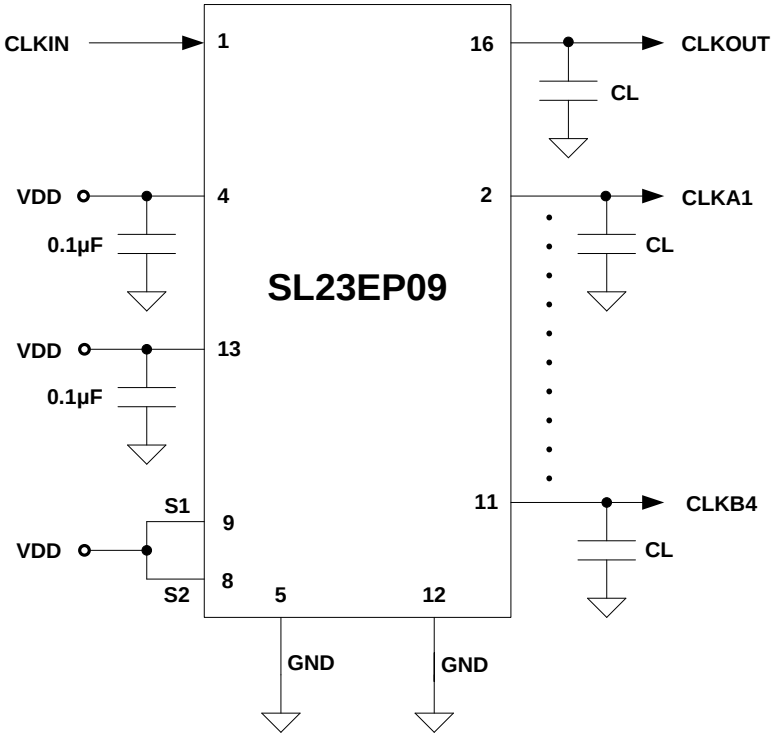
Symbol	Description	Condition	Min	Typ	Max	Unit
tPLLOCK	PLL Lock Time[9]	Time from 90% of VDD to valid clocks on all the output clocks	–	–	1.0	ms
CCJ [2,3]	Cycle-to-cycle Jitter	3.3V supply, >66 MHz, <15 pF, high drive	–	30	60	ps
		3.3V supply, >66 MHz, <15 pF, standard drive	–	50	185	ps
		2.5V supply, >66 MHz, <15 pF, high drive	–	70	150	ps
		2.5V supply, >66 MHz, <15 pF, standard drive	–	100	250	ps
		3.3V supply, >66 MHz, <30 pF, high drive	–	50	350	ps
		3.3V supply, >66 MHz, <30 pF, standard drive	–	65	250	ps
		2.5V supply, >66 MHz, <30 pF, high drive	–	75	430	ps
		S2:S1 = 1:0 mode, 3.3V, <15pF, high drive	–	15	40	ps
		S2:S1 = 1:0 mode, 3.3V, <15pF, standard drive	–	15	40	ps
		S2:S1 = 1:0 mode, 2.5V, <15pF, high drive	–	20	50	ps
		S2:S1 = 1:0 mode, 2.5V, <15pF, standard drive	–	20	50	ps
PPJ [2,3]	Peak Period Jitter	3.3V supply, >100 MHz, <15 pF, standard drive	–	40	90	ps
		3.3V supply, 66-100 MHz, <15 pF, standard drive	–	50	95	ps
		2.5V supply, 66-100 MHz, <15 pF, high drive	–	40	85	ps
		2.5V supply, >66 MHz, <15 pF, standard drive	–	75	180	ps
		2.5V supply, >100 MHz, <15 pF, high drive	–	15	45	ps
		S2:S1 = 1:0 mode, 3.3V, <15pF, standard drive	–	25	60	ps
		S2:S1 = 1:0 mode, 3.3V, <15pF, high drive	–	25	60	ps
		S2:S1 = 1:0 mode, 2.5V, <15pF, standard drive	–	40	80	ps
		S2:S1 = 1:0 mode, 2.5V, <15pF, high drive	–	40	80	ps

Notes:

3. Typical jitter is measured at 3.3V or 2.5V, 30°C with all outputs driven into the maximum specified load.

External Components & Design Considerations

Typical Application Schematic



Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD and VSS pins. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

Series Termination Resistor: A series termination resistor is recommended if the distance between the output clocks and the load is over 1 ½ inch. The nominal impedance of the clock outputs is given on the page 4. Place the series termination resistors as close to the clock outputs as possible.

Zero Delay and Skew Control: All outputs and CLKIN pins should be loaded with the same load to achieve “Zero Delay” between the CLKIN and the outputs. The CLKOUT pin is connected to CLKIN internally on-chip for feedback to PLL, and sees an additional 2 pF load with respect to Bank A and B clocks. For applications requiring zero input/output delay, the load at the all output pins including the CLKOUT pin must be the same. If any delay adjustment is required, the capacitance at the CLKOUT pin could be increased or decreased to increase or decrease the delay between Bank A and B clocks and CLKIN.

For minimum pin-to-pin skew, the external load at all the Bank A and B clocks must be the same.

Switching Waveforms

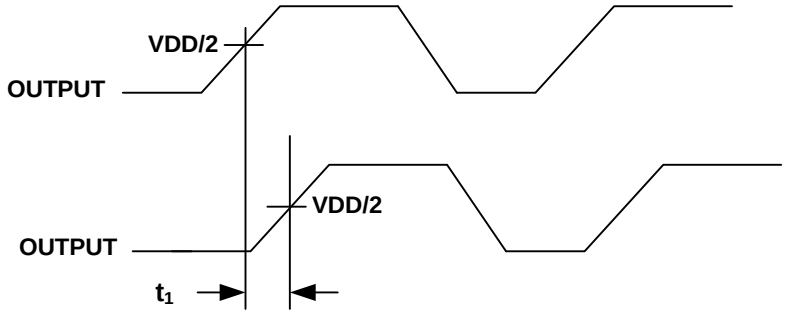


Figure 2. Output to Output Skew

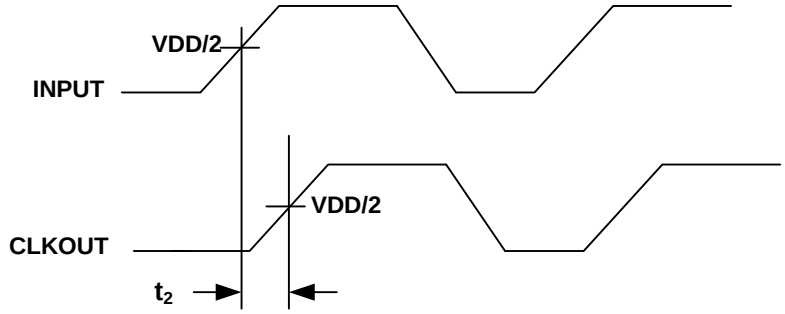


Figure 3. Input to Output Skew

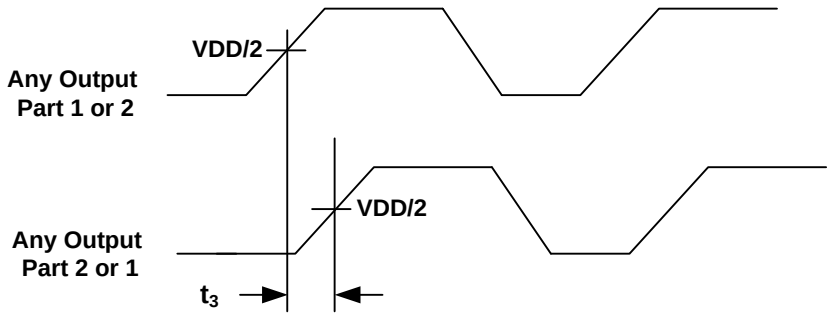
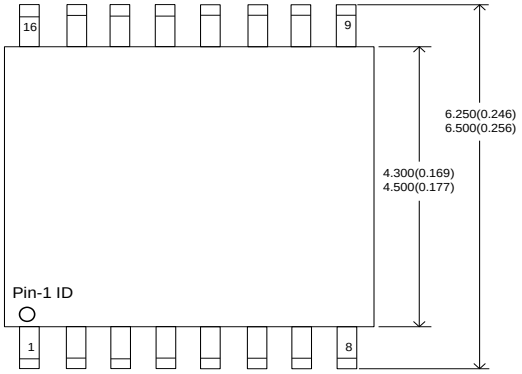


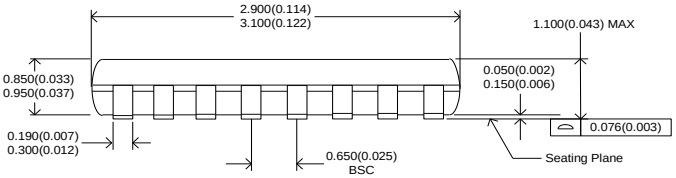
Figure 4. Part-to-Part Skew

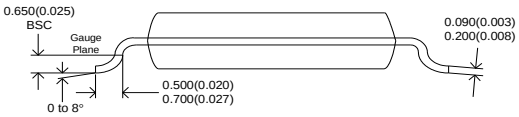
Package Drawing and Dimensions

16-Lead TSSOP (4.4mm)



Dimensions are in milimeters(inches).
Top line: (MIN) and Bottom line: (Max)





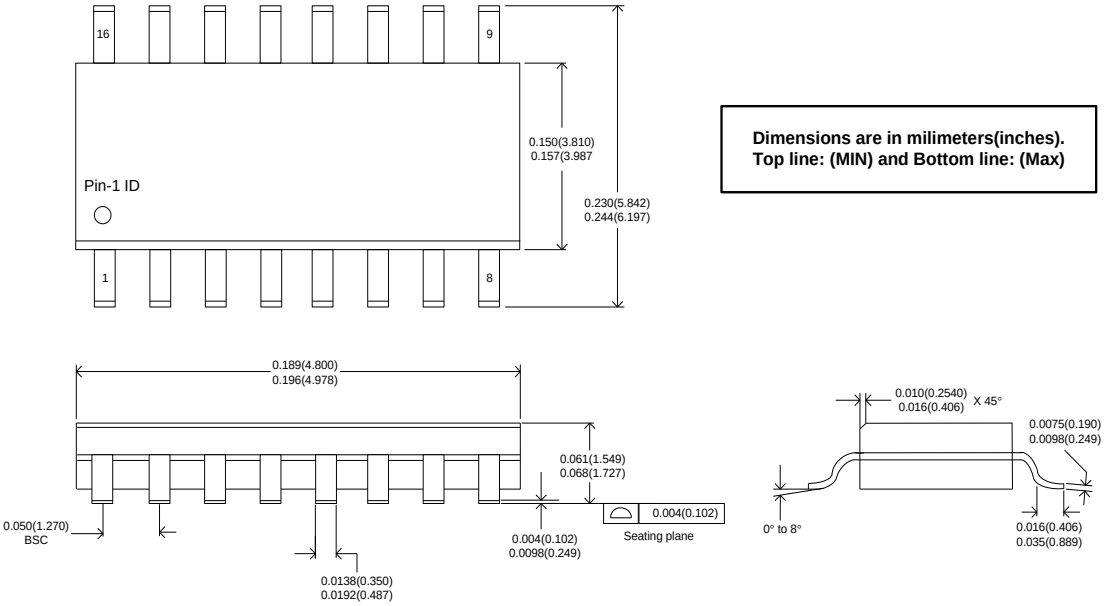
****Dimensions are in inches (millimeters)**

Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	Still air	-	105	-	°C/W
	θ JA	1m/s air flow	-	95	-	°C/W
	θ JA	3m/s air flow	-	90	-	°C/W
Thermal Resistance Junction to Case	θ JC	Independent of air flow	-	35	-	°C/W

Package Drawing and Dimensions (Cont.)

16-Lead SOIC (150 Mil)



****Dimensions are in inches (millimeters)**

Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	Still air	-	80	-	°C/W
	θ JA	1m/s air flow	-	74	-	°C/W
	θ JA	3m/s air flow	-	71	-	°C/W
Thermal Resistance Junction to Case	θ JC	Independent of air flow	-	44	-	°C/W

Ordering Information [4]

Ordering Number	Marking	Shipping Package	Package	Temperature
SL23EP09ZC-1	SL23EP09ZC-1	Tube	16-pin TSSOP	0 to 70°C
SL23EP09ZC-1T	SL23EP09ZC-1	Tape and Reel	16-pin TSSOP	0 to 70°C
SL23EP09ZC-1H	SL23EP09ZC-1H	Tube	16-pin TSSOP	0 to 70°C
SL23EP09ZC-1HT	SL23EP09ZC-1H	Tape and Reel	16-pin TSSOP	0 to 70°C
SL23EP09ZI-1	SL23EP09ZI-1	Tube	16-pin TSSOP	-40 to 85°C
SL23EP09ZI-1T	SL23EP09ZI-1	Tape and Reel	16-pin TSSOP	-40 to 85°C
SL23EP09ZI-1H	SL23EP09ZI-1H	Tube	16-pin TSSOP	-40 to 85°C
SL23EP09ZI-1HT	SL23EP09ZI-1H	Tape and Reel	16-pin TSSOP	-40 to 85°C
SL23EP09SC-1	SL23EP09SC-1	Tube	16-pin SOIC	0 to 70°C
SL23EP09SC-1T	SL23EP09SC-1	Tape and Reel	16-pin SOIC	0 to 70°C
SL23EP09SC-1H	SL23EP09SC-1H	Tube	16-pin SOIC	0 to 70°C
SL23EP09SC-1HT	SL23EP09SC-1H	Tape and Reel	16-pin SOIC	0 to 70°C
SL23EP09SI-1	SL23EP09SI-1	Tube	16-pin SOIC	-40 to 85°C
SL23EP09SI-1T	SL23EP09SI-1	Tape and Reel	16-pin SOIC	-40 to 85°C
SL23EP09SI-1H	SL23EP09SI-1H	Tube	16-pin SOIC	-40 to 85°C
SL23EP09SI-1HT	SL23EP09SI-1H	Tape and Reel	16-pin SOIC	-40 to 85°C

Notes:

4. The SL23EP09 products are RoHS compliant.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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